SGS-THOMSON MICROELECTRONICS

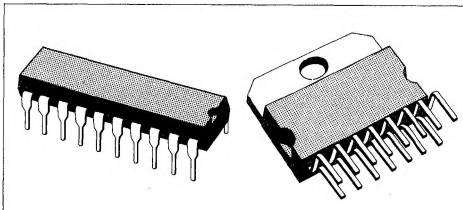
L6122
L6123

100 V DMOS SWITCHES

ADVANCE DATA

- OUTPUT VOLTAGE TO 100 V
- 0,5 Ω $R_{DS\ (on)}$
- SUPPLY VOLTAGE UP TO 60 V
- LOW INPUT CURRENT
- TTL/CMOS COMPATIBLE INPUTS
- HIGH SWITCHING FREQUENCY (200 KHz)

MultiPower BCD Technology



Powerdip 14+3+3 — **Multiwatt-15**

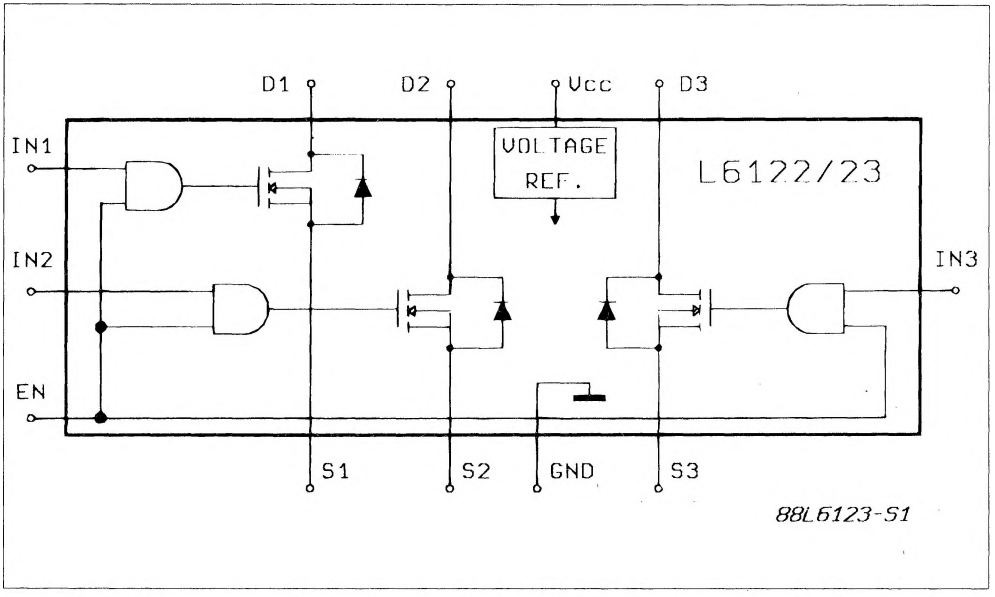
ORDER CODES : L6122, L6123

DESCRIPTION

Realized with the Multipower-BCD mixed bipolar/CMOS/DMOS process, the L6122/23 monolithic three DMOS switch is designed for high current, high voltage switching applications. Each of the three switches is controlled by a logic input and all three are controlled by a common enable input. All inputs are TTL/CMOS compatible for direct connection to logic circuits. Each source is available for the insertion of the sense resistors in current control applications.

Two versions are available : the L6122 mounted in a Powerdip 14 + 3 + 3 package and the L6123 in a 15-lead Multiwatt package.

BLOCK DIAGRAM

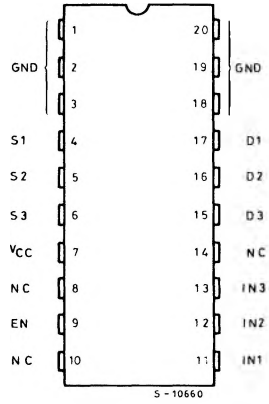


ABSOLUTE MAXIMUM RATINGS

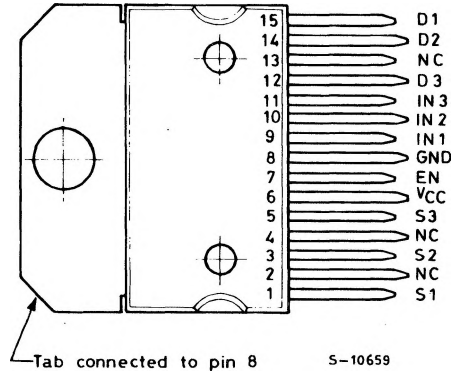
Symbol	Parameter		Value	Unit
V_{DS}	Drain-source Voltage		100	V
V_{CC}	Supply Voltage		60	V
I_D	Continuous Drain Current	@ T_{pins} = 90 °C Powerdip	1.5	A
		@ T_{case} = 90 °C Multiwatt –15	3	A
I_{DM} (*)	Pulsed Drain Current	Powerdip	5	A
		Multiwatt –15	8	A
I_{SD}	Continuous Source-drain Diode Current	@ T_{pins} = 90 °C Powerdip	1.5	A
		@ T_{case} = 90 °C Multiwatt –15	3	A
I_{SDM}	Pulsed Source Drain Diode Current	Powerdip	5	A
		Multiwatt –15	8	A
V_{IN}	Input Voltage		7	V
V_{EN}	Enable Voltage		7	V
V_S	Source Voltage		– 1 to + 4	V
P_{tot}	Total Power Dissipation	@ T_{pins} = 90 °C Powerdip	4.3	W
		@ T_{case} = 90 °C Multiwatt –15	20	W
		@ T_{amb} = 70 °C Powerdip	1.3	W
		@ T_{amb} = 70 °C Multiwatt –15	2.3	W
T_{stg}, T_j	Storage and Junction Temperature Range		– 40 to + 150	°C

(*) Pulse width ≤ 300 µs, duty cycle ≤ 10 %.
NOTE : I_D, I_{DM}, I_{SD}, I_{SDM} are given per channel.

CONNECTION DIAGRAMS (top view)



L6122 (Powerdip)



L6123 (Multiw. 15)

THERMAL DATA

			Powerdip	Multiwatt –15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	-
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	-	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	65 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_{CC} = 40 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		14		48	V
I_{CC}	Supply Current	All V_{IN} = H V_{EN} = Square Wave (200 KHz, 50 % DC)		9		mA
I_Q	Quiescent Current	V_{EN} = L		2	3	mA
BV_{DSS}	Drain Source Breakdown Voltage	I_D = 1 mA, V_{EN} = L	100			V
I_{DSS}	Output Leakage Current	V_{EN} = L, V_{DS} = 100 V			1	mA
		V_{EN} = L, V_{DS} = 80 V, T_j = 125 °C		1		mA
$R_{DS\ (on)}$ (*)	Static Drain-source on Resistance	$V_{CC} \geq$ 14 V, I_D = 1.5 A, V_{EN}, V_{IN} = H		0.7		Ω
V_{INL}, V_{ENL}	Input Low Voltage		– 0.3		0.8	V
V_{INH}, V_{ENH}	Input High Voltage		2		7	V
I_{INL}, I_{ENL}	Input Low Current	V_{IN}, V_{EN} = L			– 100	µA
I_{INH}, I_{ENH}	Input High Current	V_{IN}, V_{EN} = H			10	µA
$t_{d\ (on)}$	Turn on Delay Time	I_D = 1.5 A See Test Circuit and Waveforms		300		ns
t_r	Rise Time			100		ns
$t_{d\ (off)}$	Turn off Delay Time			400		ns
t_f	Fall Time			100		ns
V_{SD} (*)	Source Drain Diode Forward Voltage	I_{SD} = 1.5 A, V_{EN} = L			1.5	V
$V_{SD\ (on)}$ (*)	Source Drain Forward Voltage	I_{SD} = 1.5 A, V_{IN}, V_{EN} = H			1.2	V

(*) Pulse test : pulse width = 300 µs, duty cycle = 2 %.

SWITCHING TIMES RESISTIVE LOAD

Figure 1 : Test Circuit.

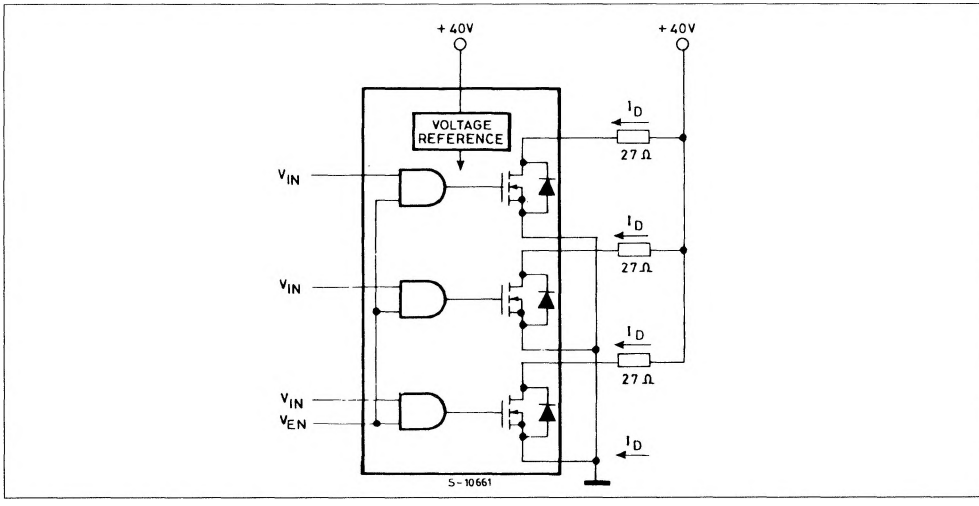


Figure 2 : Waveforms.

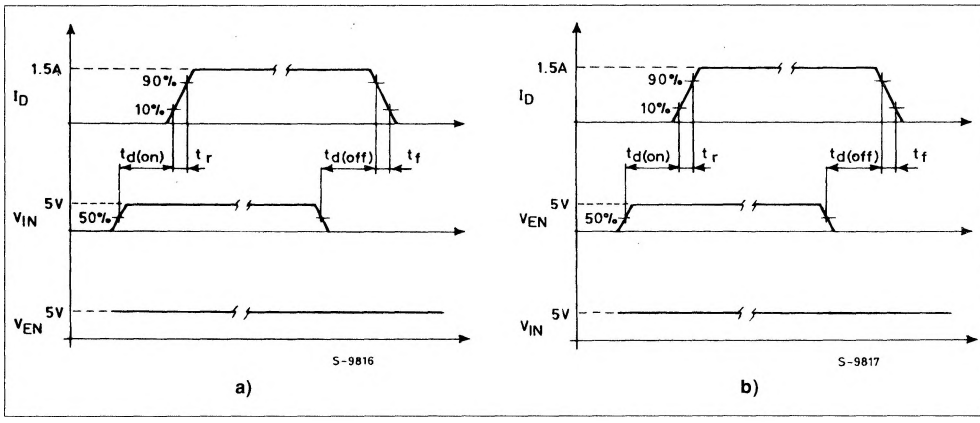


Figure 3 : Static Drain-source on Resistance.

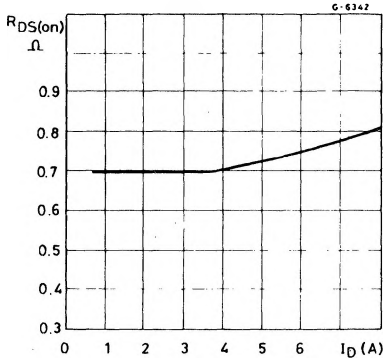


Figure 4 : Normalized Breakdown Voltage vs. Temperature.

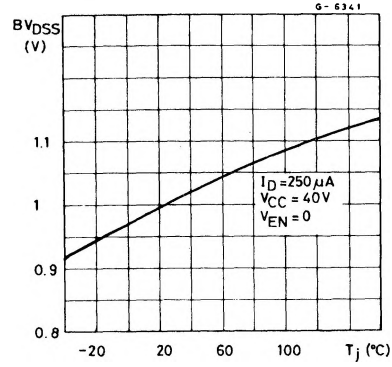


Figure 5 : Normalized on Resistance vs. Temperature.

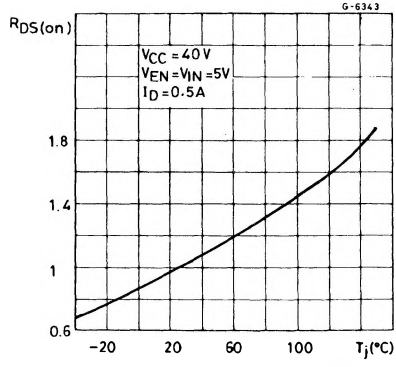


Figure 6 : Typical Source-drain Diode Forward Voltage.

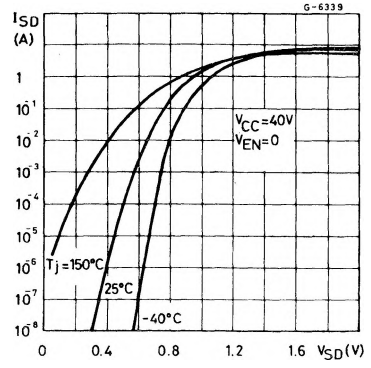
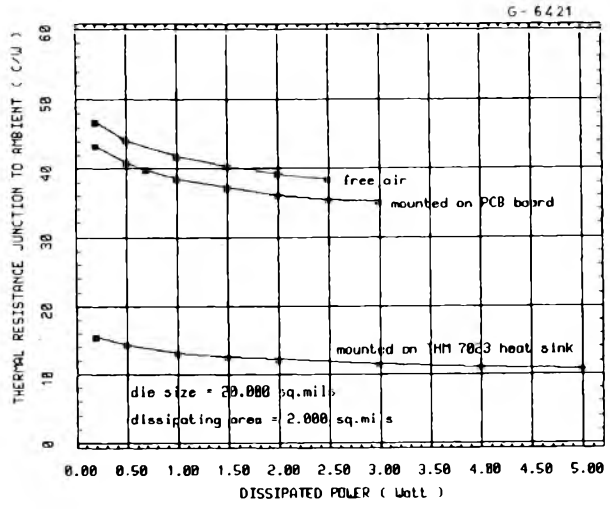


Figure 7 : $R_{th\ j\text{-}amb}$ vs. Dissipated Power (Multiwatt).



(*) Rth = 9°C/W

Figure 8 : Transient Thermal Resistance for Single Pulses (Multiwatt).

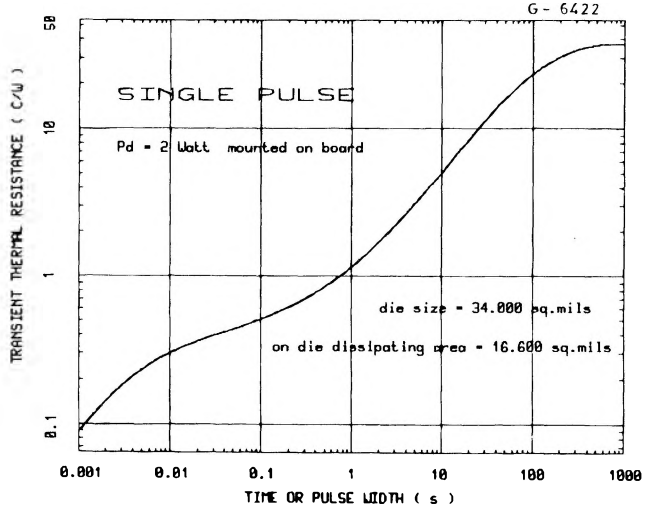


Figure 9 : Peak Transient Thermal Resistance vs. Pulse Width and Duty Cycle (Multiwatt).