SGS-THOMSON MICROELECTRONICS

L6201

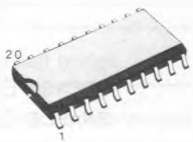
0.3Ω DMOS FULL BRIDGE DRIVER

ADVANCE DATA

- SUPPLY VOLTAGE UP TO 48V
- 2A MAX PEAK CURRENT
- TOTAL RMS CURRENT UP TO 1.0A
- $RD_{DS(ON)}$ 0.3Ω (TYPICAL VALUE AT 25°C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY (TYPICAL 90%)

The L6201 is a full bridge driver for motor control applications realised in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimise the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can deliver 1.0A RMS at motor supply voltages up to 48V and efficiently at high switching speeds. All the logic inputs are TTL, CMOS and μC compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The L6201 is mounted in an SO.20 package. Even at the full rated current and voltage no external heatsink is required at normal operating temperatures.

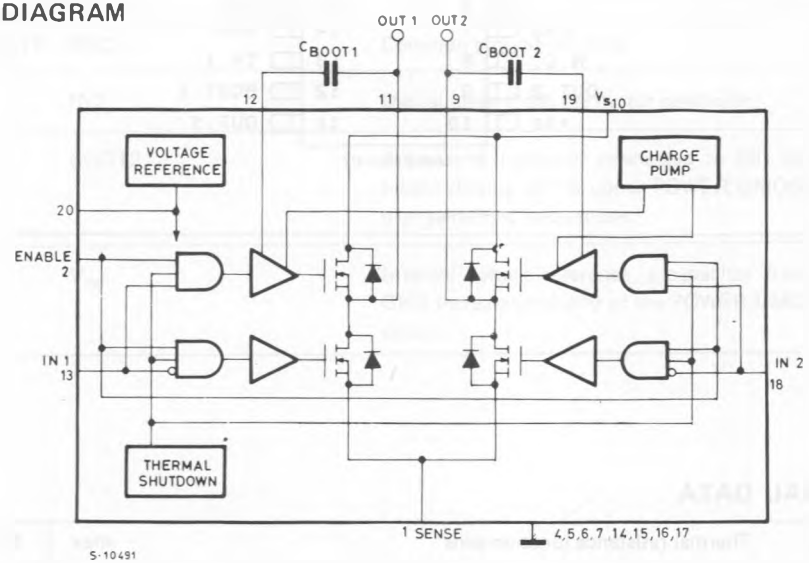
MultiPower BCD Technology



SO-20
(12 + 4 + 4)

ORDERING NUMBER: L6201

BLOCK DIAGRAM

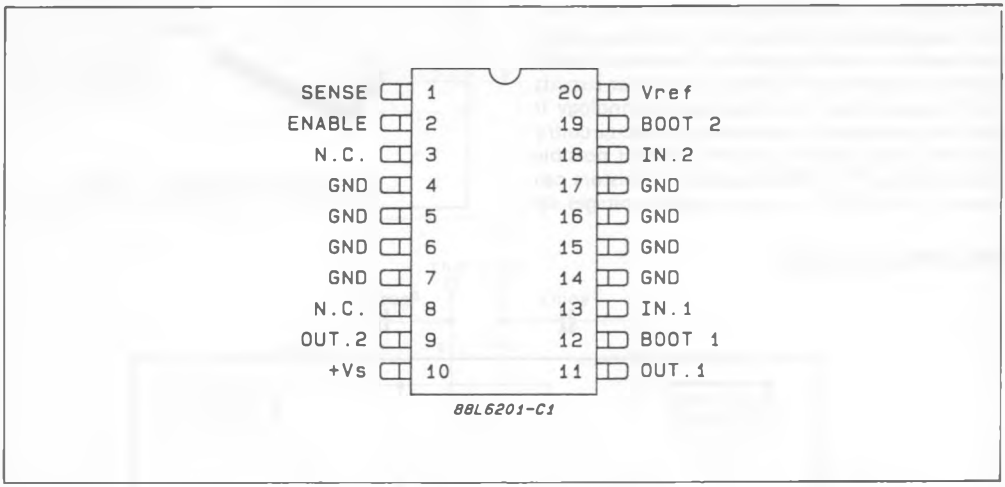


ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	52	V
V_{IN}, V_{EN}	Input or Enable voltage	-0.3 to 7	V
I_o	DC output current (note 1)	1	A
	- non repetitive (< 1ms)	5	A
V_{sense}	Sensing voltage	-1 to 4	V
V_b	Boostrap peak voltage	60	V
P_{tot}	Total power dissipation (T_{pins} = 90°C)	4	W
	(T_{amb} = 70°C no copper area on PCB)	0.9	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Note 1 : Pulse width limited only by junction temperature and the transient thermal impedance.

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	15	°C/W

PIN FUNCTIONS

PIN	NAME	FUNCTION
1	SENSE	A resistance R_{sense} connected to this pin provides feedback for motor current control
2	ENABLE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.
3	NO CONNECTION	
4, 5, 6, 7	GND	Common ground terminal.
8	NO CONNECTION	
9	OUT2	Output of the half bridge.
10	V_s	Supply voltage.
11	OUT1	Output of the half bridge.
12	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
13	IN1	Digital input from the motor controller.
14,15,16,17	GND	Common ground terminal.
18	IN2	Digital input from the motor controller.
19	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
20	V_{ref}	Internal voltage reference, a capacitor from this pin to GND increases stability of the POWER DMOS logic drive circuit.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits T_j = 25°C, V_s = 36V, unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		12	36	48	V
V_{ref}	Reference voltage			13.5		V
I_s	Quiescent supply current	EN = H V_{IN} = L EN = H V_{IN} = H I_L = 0 EN = L Fig. 10		10 10 8		mA mA mA
f_c	Commutation frequency			30	100	KHz
T_j	Thermal shutdown			150		°C
T_d	Dead time protection			100		ns
TRANSISTORS						
OFF						
I_{DSS}	Leakage current	Fig. 11		100		µA
ON						
R_{DS}	On resistance			0.3		Ω
$V_{DS(ON)}$	Drain source voltage	I_{DS} = 1.0A Fig. 9		0.36		V
V_{sens}	Sensing voltage		-1		4	V
SOURCE DRAIN DIODE						
V_{sd}	Forward ON voltage	I_{SD} = 1.0A EN = L		0.9		V
t_{rr}	Reverse recovery time	I_F = 1.0A $\frac{dif}{dt}$ = 25A/µs		300		ns
t_{fr}	Forward recovery time			200		ns
LOGIC LEVELS						
V_{INL}, V_{ENL}	Input Low voltage		-0.3		0.8	V
V_{INL}, V_{ENH}	Input High voltage		2		7	V
I_{INL}, I_{ENL}	Input Low current	V_{IN}, V_{EN} = L			-10	µA
I_{INH}, I_{ENH}	Input High current	V_{IN}, V_{EN} = H		30		µA
LOGIC CONTROL TO POWER DRIVE TIMING						
t_1 (V_i)	Source current turn-off delay	Fig. 12		300		ns
t_2 (V_i)	Source current fall time	Fig. 12		200		ns
t_3 (V_i)	Source current turn-on delay	Fig. 12		400		ns
t_4 (V_i)	Source current rise time	Fig. 12		200		ns
t_5 (V_i)	Sink current turn-off delay	Fig. 13		300		ns
t_6 (V_i)	Sink current fall time	Fig. 13		200		ns
t_7 (V_i)	Sink current turn-on delay	Fig. 13		400		ns
t_8 (V_i)	Sink current rise time	Fig. 13		200		ns

Fig. 1 - Typical I_s normalized vs. T_j

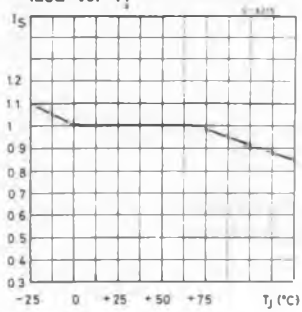


Fig. 2 - Quiescent current vs. frequency

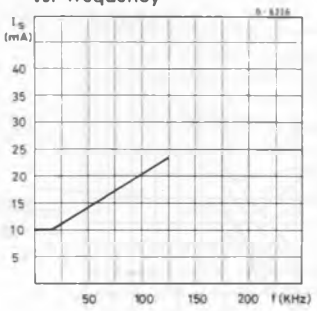


Fig. 3 - Typical I_s normalized vs. V_s

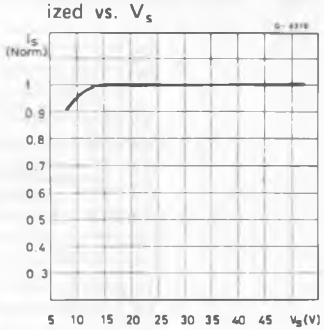


Fig. 4 - Typical diode behaviour in synchronous rectification

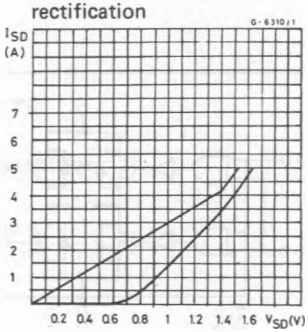


Fig. 5 - Typical $R_{DS\ (ON)}$ vs. $V_s \cong V_{ref}$

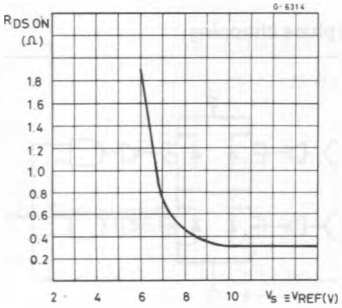


Fig. 6 - $R_{DS\ (ON)}$ normalized at 25°C vs. temperature typical values

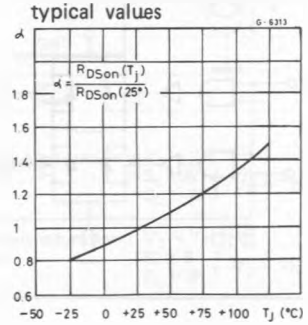


Fig. 7 - $R_{DS\ (ON)}$ vs. DMOS transistor current

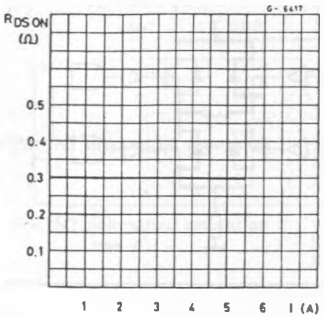


Fig. 8 - Typical power dissipation vs. I_L

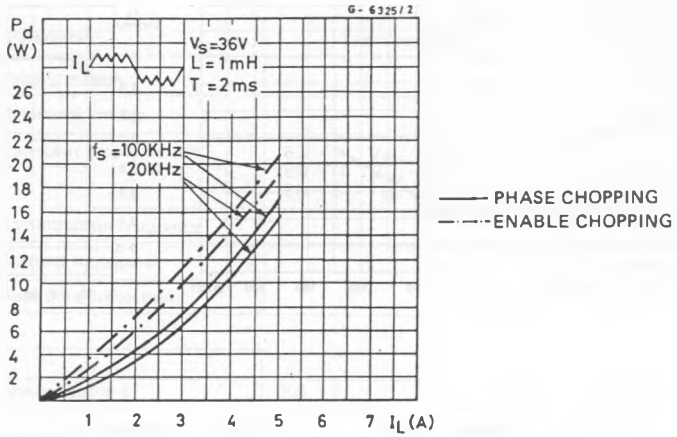


Fig. 8a - Two phase chopping

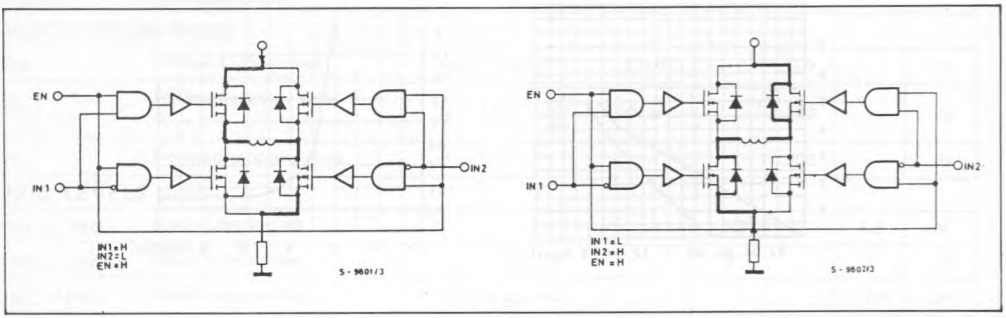


Fig. 8b - One phase chopping

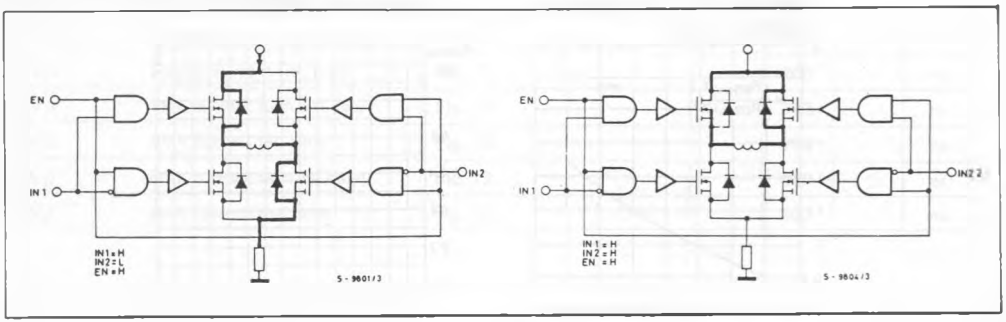
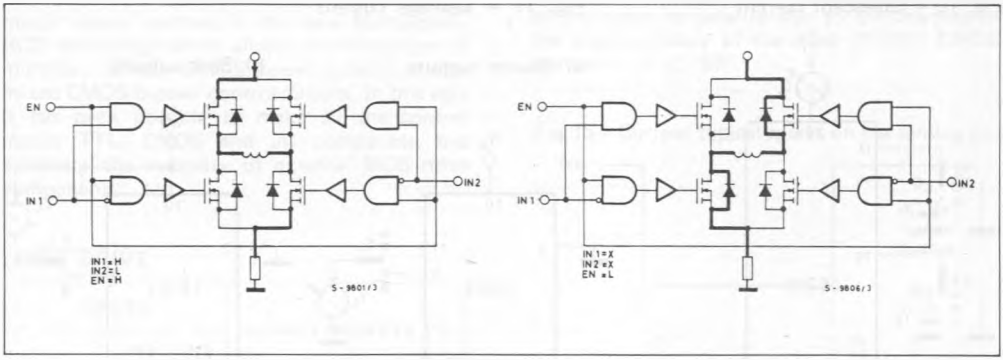


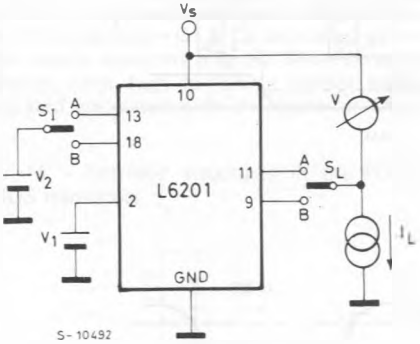
Fig. 8c - Enable chopping



TEST CIRCUITS

Fig. 9 - Saturation voltage

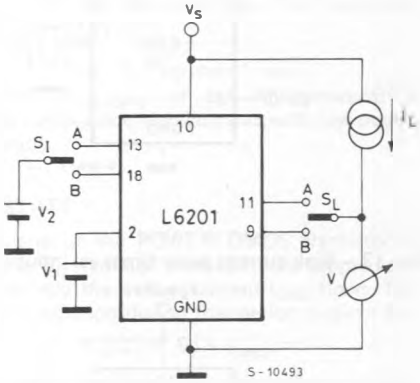
a) Source outputs



For IN1 source output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "H"

For IN2 source output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "H"

b) Sink outputs



For IN1 sink output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "L"

For IN2 sink output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "L"

TEST CIRCUITS (continued)

Fig. 10 - Quiescent current

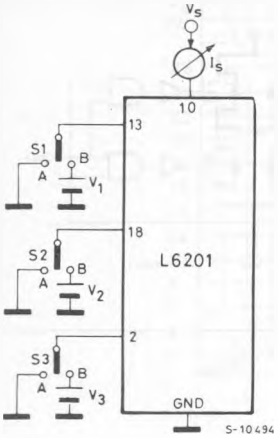
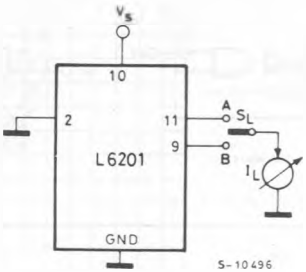
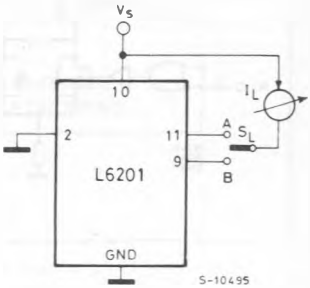


Fig. 11 - Leakage current

a) Source outputs

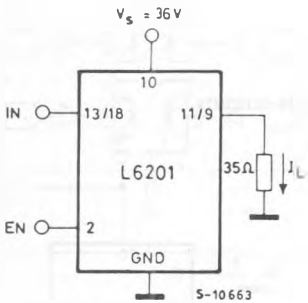


b) Sink outputs



SWITCHING TIMES

Fig. 12 - Source current delay times vs. input



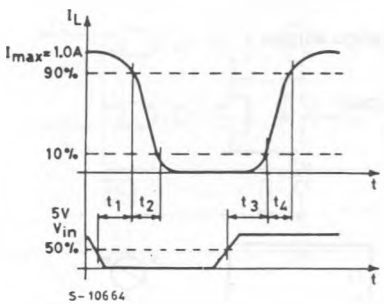
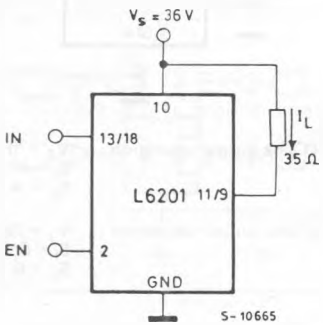
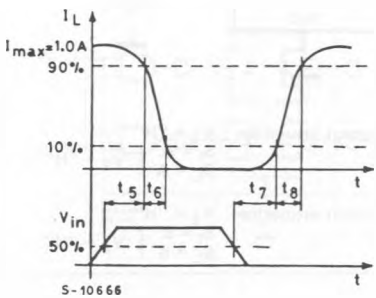


Fig. 13 - Sink current delay times vs. input





CIRCUIT DESCRIPTION

The L6201 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits. In this way it has been possible to make all the control inputs TTL, CMOS and μC compatible and eliminate the necessity of external MOS drive components.

LOGIC DRIVE

INPUTS			OUTPUT MOSFETS (*)
	IN1	IN2	
V_{EN} = H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
V_{EN} = L	X	X	All transistors turned oFF

L = Low H = High X = Don't care

(*) Numbers referred to INPUT 1 or INPUT2 controlled outputs stages

CROSS CONDUCTION

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (Fig. 14). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor. (Fig. 15)

Fig. 14 - Intrinsic structures in the POWER DMOS transistors

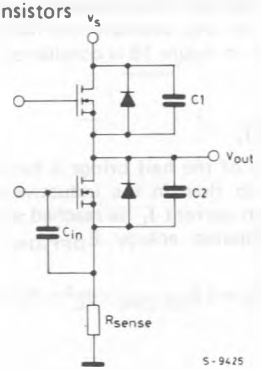
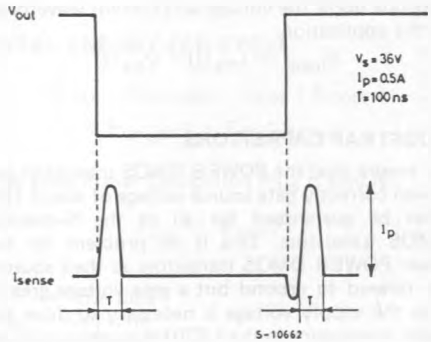


Fig. 15 - Current typical spikes on the sensing pin



TRANSISTOR OPERATION

ON STATE

When one of the POWER DMOS transistor is ON it can be considered as a resistor $R_{DS(ON)}$ (= 0.3Ω) throughout the recommended operating range. In this condition the dissipated power is given by:

$$P_{ON} = R_{DS(ON)} \cdot I_{DS}^2$$

The low $R_{DS(ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by:

$$P_{OFF} = V_s \cdot I_{DSS}$$

The power dissipation is in the order of pW and is negligible in comparison to that dissipated in the ON STATE.

TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have as intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode

applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_D$ and when the voltage reaches the diode voltage it is clamped to its characteristic. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans.} = I_{DS}(t) \cdot V_{DS}(t)$$

BOOSTRAP CAPACITORS

To ensure that the POWER DMOS transistors are driven correctly gate source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. This is no problem for the lower POWER DMOS transistors as their sources are refered to ground but a gate voltage greater than the supply voltage is necessary to drive the upper transistors. In the L6201 this achieved by an internal charge pump circuit that guarantees correct DC drive in combination with the boostrap circuit charges the external C_B capacitors when the source transistor is OFF and the sink transistor is ON giving lower commutation losses in switched mode operation. For efficient charging the value of the boostrap capacitor should be greater than the input capacitance of the power transistor which is around 1nF. It is recommended that a capacitance of at least 10nF is used for the bootstrap. If a smaller capacitor is used there is a risk that the POWER transistors will not be fully turned on and they will show a higher $R_{DS\,(ON)}$. On the other hand if a elevated value is used it is possible that a current spike may be produced in the sense resistor.

REFERENCE

To stabilise the internal drive circuit it is recommended that a capacitor be placed between this pin and ground. A value of 0.22μF should be sufficient for most applications.

This pin is also protected against a short circuit to ground.

DEAD TIME

To protect the device against simultaneous conduction in both arms of the bridge and the resulting rail to rail short, the logic control circuit provides a dead time greater than 40ns.

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature e reaches 150°C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problems because the voltage created across the sense resistor is usually much less than the peak value, although a small RC filter can be added if necessary.

POWER DISSIPATION

In order to achieve the high performance provided by the L6201 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat. The first stage of any thermal design is to calculate the dissipated power in the application, for this example the half step operation shown in figure 16 is considered.

RISE TIME T_r

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r. The dissipated energy $E_{OFF/ON}$ is in this case:

$$E_{OFF/ON} = [R_{DS\,(ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the commutation E_{COM}. As two of the POWER DMOS transistors are ON E_{ON} is given by:

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is:

$$E_{COM} = V_s \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where:

T_{COM} = Commutation Time and it is assumed that;
$T_{COM} = T_{TURN-ON} = T_{TURN-OFF} = 100ns$
f_{SWITCH} = Chopper frequency

FALL TIME T_f

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time:

$$E_{ON/OFF} = [R_{DS(ON)} \cdot I_L^2 \cdot T_f] \cdot 2/3$$

QUIESCENT ENERGY

The last contribution to the energy dissipation is due to the quiescent supply current and is given by:

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_s \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF} + E_{QUIESCENT}$$

The Total Power Dissipation P_{DIS} is simply:

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time
T_{ON} = ON time
T_f = Fall time
T_d = Dead time
T = Period

$$T = T_r + T_{ON} + T_f + T_d$$

Fig. 16 - Load current in half step operation

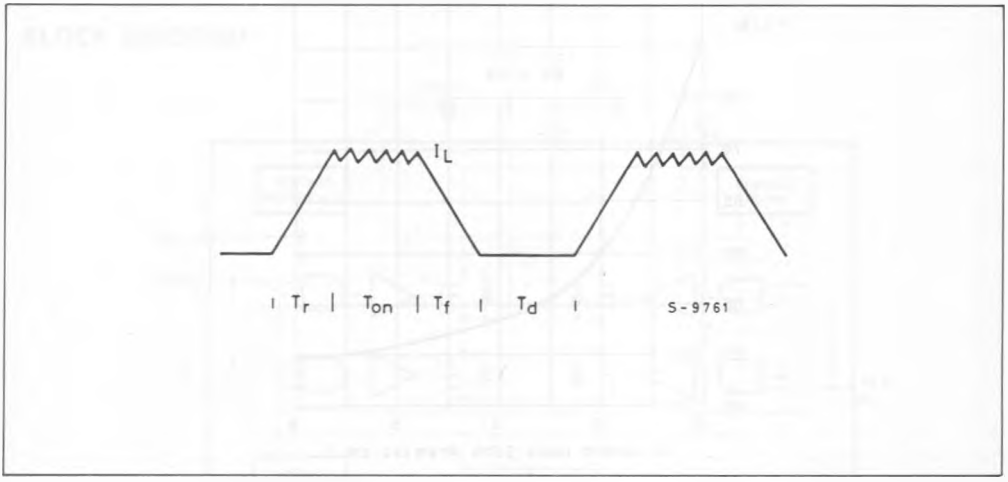


Fig. 17 - Two phase Bipolar stepper motor control circuit with chopper current control and translator

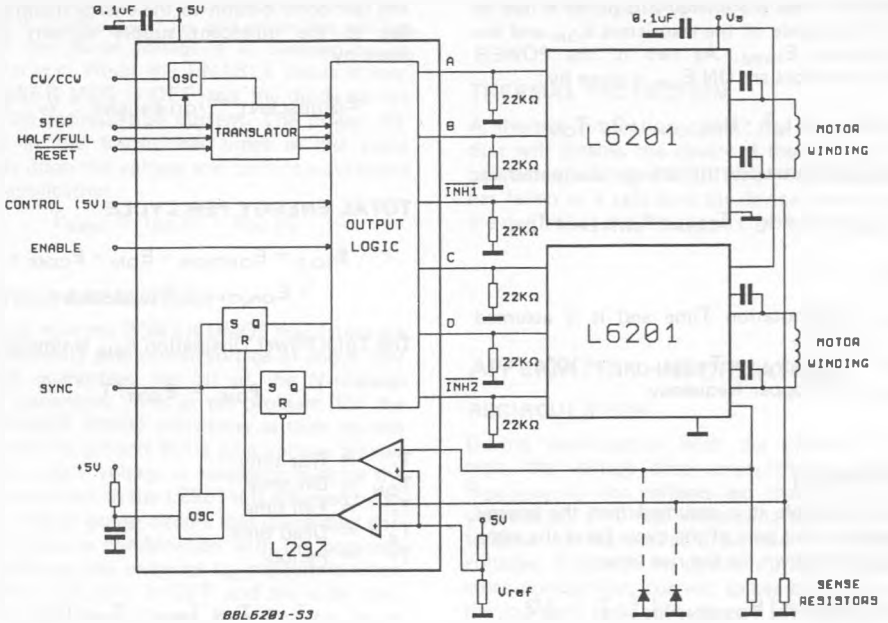


Fig. 18 - Rth junction to ambient vs. "on board" heat sink area