SGS-THOMSON MICROELECTRONICS

L6203

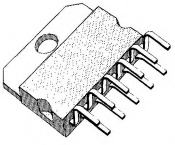
0.3Ω DMOS FULL BRIDGE DRIVER

PRELIMINARY DATA

- SUPPLY VOLTAGE UP TO 48V
- 5A MAX PEAK CURRENT
- TOTAL RMS CURRENT UP TO 4A
- $R_{DS(ON)}$ 0.3Ω (TYPICAL VALUE AT 25°C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY (TYPICAL 90%)

The L6203 is a full bridge driver for motor control applications realized in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can deliver 4A RMS at motor supply voltages up to 48V and efficiently at high switch speeds. All the logic inputs are TTL, CMOS and μC compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The L6203 is mounted in a 11-lead Multiwatt package.

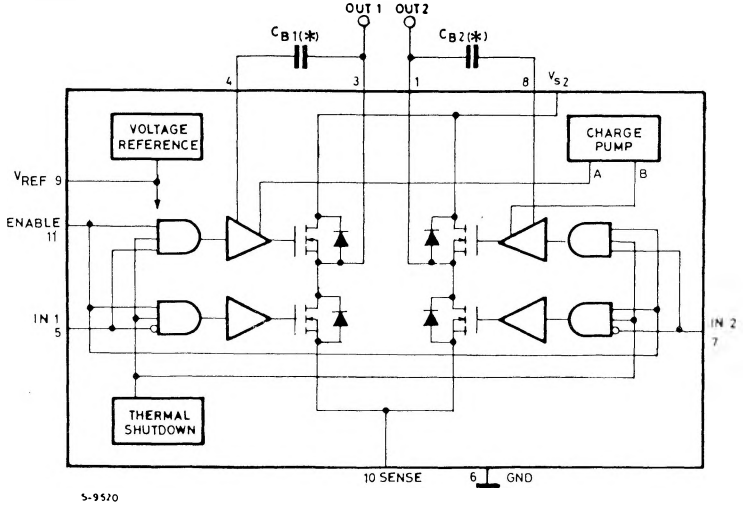
MultiPower BCD Technology



Multiwatt-11

ORDERING NUMBER: L6203

BLOCK DIAGRAM



(*) Suggested value for C_{BOOT1} and C_{BOOT2}: 10nF

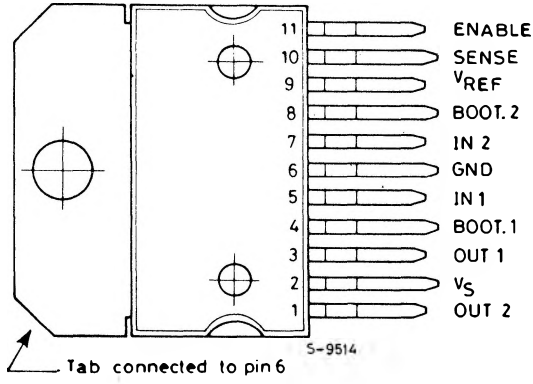
ABSOLUTE MAXIMUM RATINGS

V_S	Power supply	52	V
V_{OD}	Differential output voltage (Between pins 1 and 3)	60	V
V_{IN}, V_{EN}	Input or Enable voltage	-0.3 to 7	V
I_o	Pulsed output current (note 1)	5	A
	- non repetitive ($< 1ms$)	10	A
V_{sense}	Sensing voltage	-1 to 4	V
V_b	Boostrap peak voltage	60	V
P_{tot}	Total power dissipation (T_{case} = 90°C)	20	W
	(T_{amb} = 70°C free air)	2.3	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Note 1 : Pulse width limited only by junction temperature and the transient thermal impedance.

CONNECTION DIAGRAM

(Top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35	°C/W

PIN FUNCTIONS

PIN	NAME	FUNCTION
1	OUT2	Output of the half bridge.
2	V_s	Supply voltage.
3	OUT1	Output of the half bridge.
4	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
5	IN1	Digital input from the motor controller.
6	GND	Common ground terminal.
7	IN2	Digital input from the motor controller.
8	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
9	V_{ref}	Internal voltage reference, a capacitor from this pin to GND increases stability of the POWER DMOS logic drive cricuit.
10	SENSE	A resistance R_{sense} connected to this pin provides feedback for motor current control.
11	ENABLE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits T_j = 25°C, V_s = 42V, unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		12	36	48	V
V_{ref}	Reference voltage			13.5		V
I_{REF}	Output current				2	mA
I_s	Quiescent supply current	EN = H V_{IN} = L EN = H V_{IN} = H I_L = 0 EN = L Fig. 10		10 10 8		mA mA mA
f_c	Commutation frequency (*)			30	100	KHz
T_j	Thermal shutdown			150		°C
T_d	Dead time protection			100		ns
TRANSISTORS						
OFF						
I_{DSS}	Leakage current	Fig. 11 V_s = 52V			1	mA
ON						
R_{DS}	On resistance			0.3		Ω
$V_{DS\ (ON)}$	Drain source voltage	I_{DS} = 3A		0.9		V
V_{sens}	Sensing voltage		-1		4	V
SOURCE DRAIN DIODE						
V_{sd}	Forward ON voltage	I_{SD} = 3A EN = L		1,35(**)		V
t_{rr}	Reverse recovery time	I_F = 3A $\frac{dif}{dt}$ = 25A/μs		300		ns
t_{fr}	Forward recovery time			200		ns
LOGIC LEVELS						
$V_{IN\,L}$, $V_{EN\,L}$	Input Low voltage		-0.3		0.8	V
$V_{IN\,H}$, $V_{EN\,H}$	Input High voltage		2		7	V
$I_{IN\,L}$, $I_{EN\,L}$	Input Low current	V_{IN}, V_{EN} = L			-10	μA
$I_{IN\,H}$, $I_{EN\,H}$	Input High current	V_{IN}, V_{EN} = H		30		μA
LOGIC CONTROL TO POWER DRIVE TIMING						
t_1 (V_i)	Source current turn-off delay	Fig. 12		300		ns
t_2 (V_i)	Source current fall time	Fig. 12		200		ns
t_3 (V_i)	Source current turn-on delay	Fig. 12		400		ns
t_4 (V_i)	Source current rise time	Fig. 12		200		ns
t_5 (V_i)	Sink current turn-off delay	Fig. 13		300		ns
t_6 (V_i)	Sink current fall time	Fig. 13		200		ns
t_7 (V_i)	Sink current turn-on delay	Fig. 13		400		ns
t_8 (V_i)	Sink current rise time	Fig. 13		200		ns

(*) Limited by power dissipation

(**) In synchronous rectification the drain-source voltage drops V_{DS} is shown in Fig. 4.

Fig. 1 - Typical I_s normalized vs. T_j

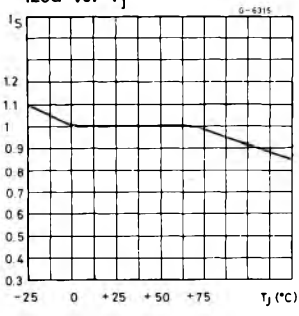


Fig. 2 - Quiescent current vs. frequency

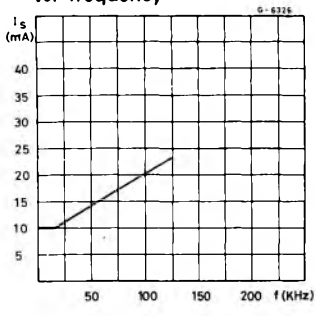


Fig. 3 - Typical I_s normalized vs. V_s

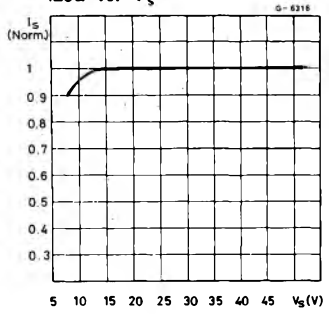


Fig. 4 - Typical diode behaviour in synchronous rectification

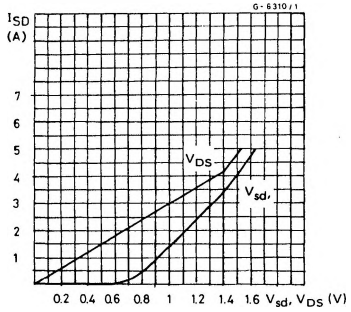


Fig. 5 - Typical $R_{DS\ (ON)}$ vs. $V_s \cong V_{ref}$

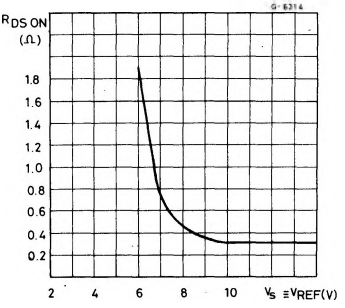


Fig. 6 - $R_{DS\ (ON)}$ normalized at 25°C vs. temperature typical values

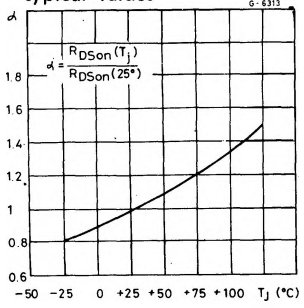


Fig. 7 - $R_{DS\ (ON)}$ vs. DMOS transistor current

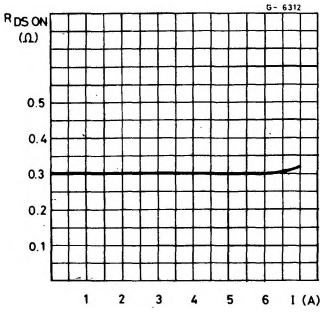


Fig. 8 - Typical power dissipation vs. I_L

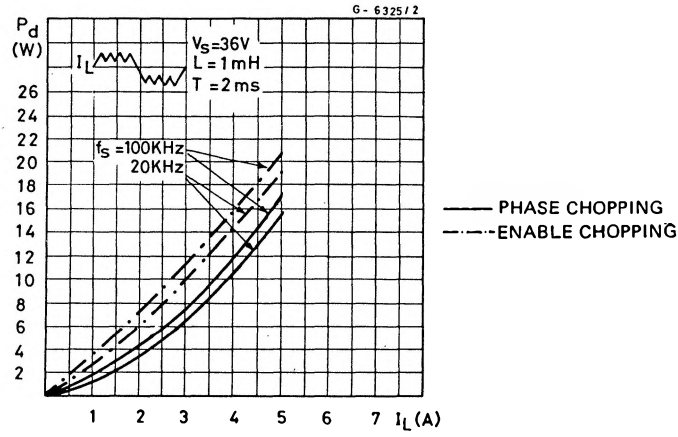


Fig. 8a - Two phase chopping

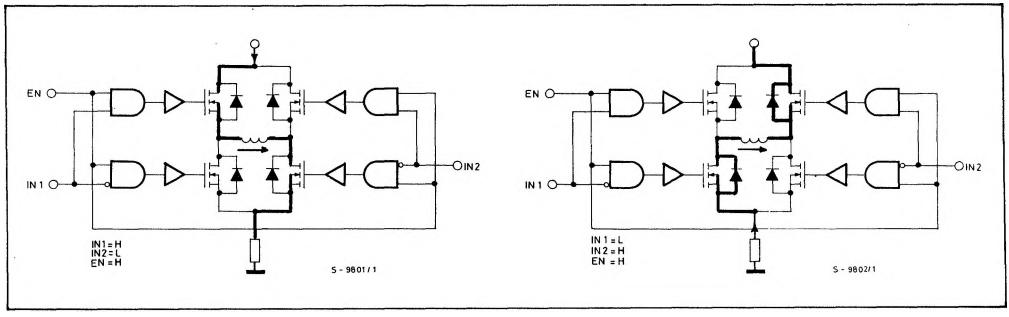


Fig. 8b - One phase chopping

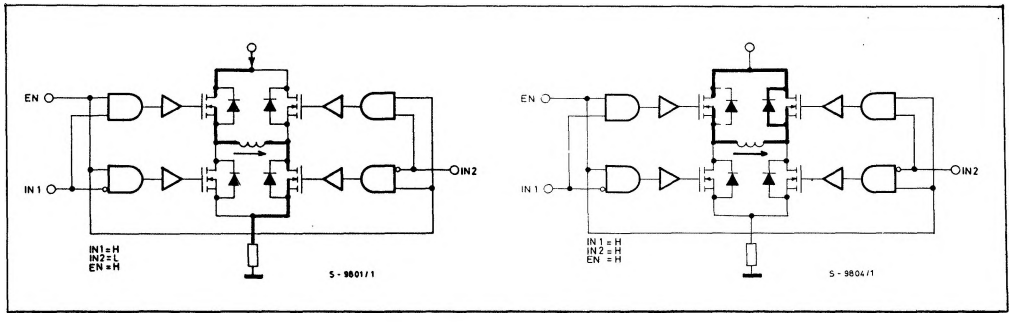
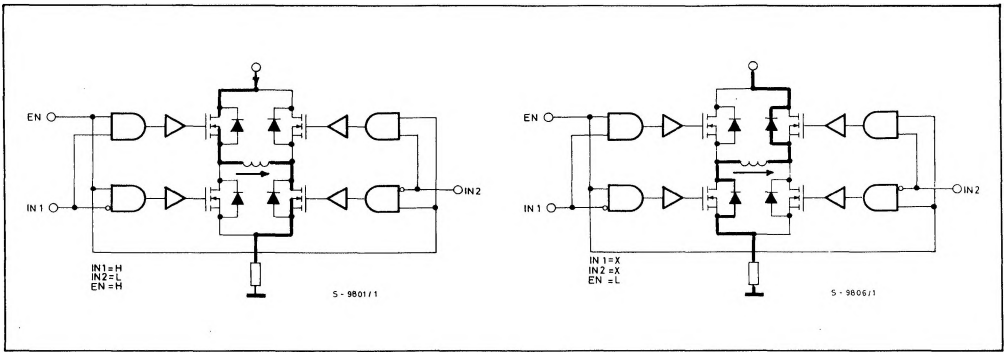


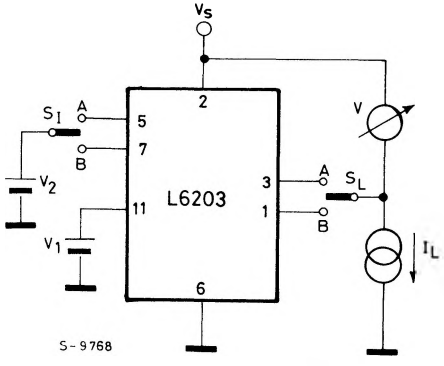
Fig. 8c - Enable chopping



TEST CIRCUITS

Fig. 9 - Saturation voltage

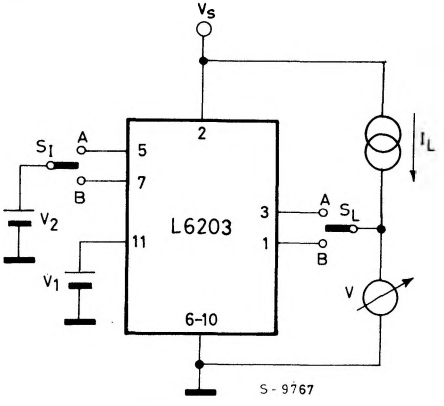
a) Source outputs



For IN1 source output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "H"

For IN2 source output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "H"

b) Sink outputs



For IN1 sink output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "L"

For IN2 sink output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "L"

TEST CIRCUITS (continued)

Fig. 10 - Quiescent current

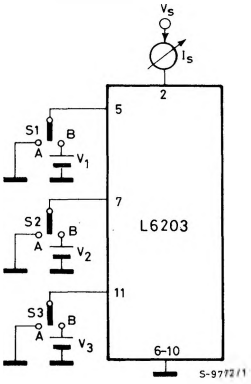
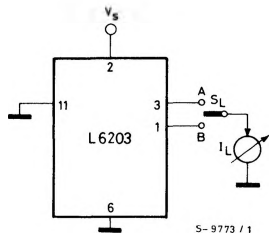
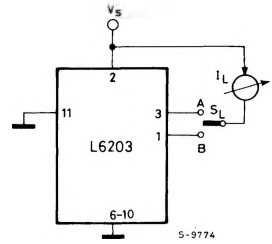


Fig. 11 - Leakage current

a) Source outputs



b) Sink outputs



SWITCHING TIMES

Fig. 12 - Source current delay times vs. input chopper

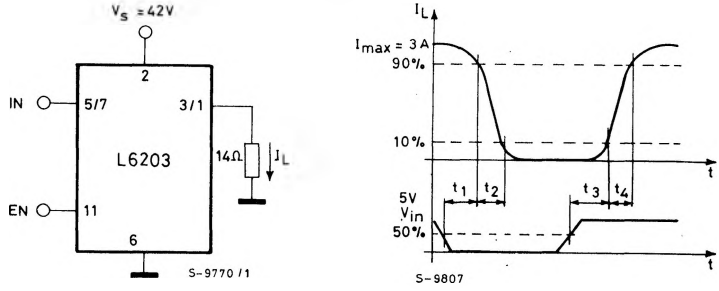
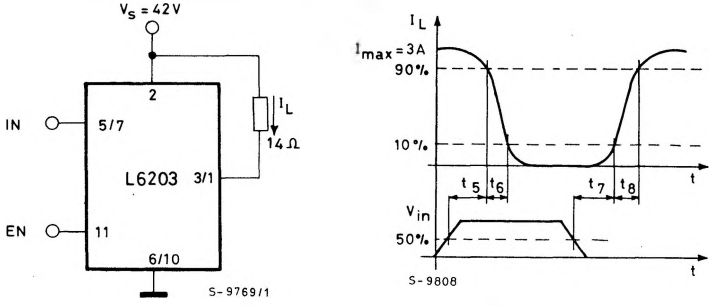


Fig. 13 - Sink current delay times vs. input chopper



CIRCUIT DESCRIPTION

The L6203 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits. In this way it has been possible to make all the control inputs TTL, CMOS and μC compatible and eliminate the necessity of external MOS drive components.

LOGIC DRIVE

INPUTS			OUTPUT MOSFETS (*)
	IN1	IN2	
V_{EN} = H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
V_{EN} = L	X	X	All transistors turned OFF

L = Low H = High X = Don't care

(*) Members referred to INPUT 1 or INPUT2 controlled outputs stages

CROSS CONDUCTION

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (Fig. 14). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor. (Fig. 15)

Fig. 14 - Intrinsic structures in the POWER MOS transistors

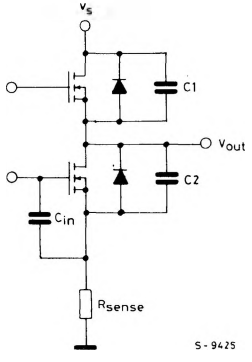
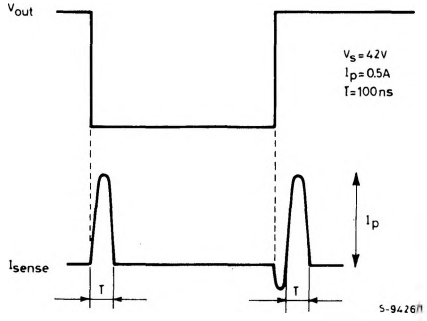


Fig. 15 - Current typical spikes on the sensing pin



TRANSISTOR OPERATION

ON STATE

When one of the POWER DMOS transistor is ON it can be considered as a resistor $R_{DS(ON)}$ (= 0.3Ω) throughout the recommended operating range. In this condition the dissipated power is given by:

$$P_{ON} = R_{DS(ON)} \cdot I_{DS}^2$$

The low $R_{DS(ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by:

$$P_{OFF} = V_s \cdot I_{DSS}$$

The power dissipation is in the order of pW and is negligible in comparison to that dissipated in the ON STATE.

TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have as intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode

applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\ (ON)}\ I_D$ and when the voltage reaches the diode voltage it is clamped to its characteristic. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans.} = I_{DS}(t) \cdot V_{DS}(t)$$

BOOSTRAP CAPACITORS

To ensure that the POWER DMOS transistors are driven correctly gate source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. This is no problem for the lower POWER DMOS transistors as their sources are refered to ground but a gate voltage greater than the supply voltage is necessary to drive the upper transistors. In the L6203 this achieved by an internal charge pump circuit that guarantees correct DC drive in combination with the boostrap circuit charges the external C_B capacitors when the source transistor is OFF and the sink transistor is ON giving lower commutation losses in switched mode operation. For efficient charging the value of the boostrap capacitor should be greater than the input capacitance of the power transistor which is around 1nF. It is recommended that a capacitance of at least 10nF is used for the bootstrap. If a smaller capacitor is used there is a risk that the POWER transistors will not be fully turned on and they will show a higher $R_{DS\ (ON)}$. On the other hand if a elevated value is used it is possible that a current spike may be produced in the sense resistor.

REFERENCE

To stabilise the internal drive circuit it is recommended that a capacitor be placed between this pin and ground. A value of 0.22μF should be sufficient for most applications.

This pin is also protected against a short circuit to ground.

DEAD TIME

To protect the device against simultaneous conduction in both arms of the bridge and the resulting rail to rail short, the logic control circuit provides a dead time greater than 40ns.

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature e reaches 150°C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\ (ON)} \cdot I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problems because the voltage created across the sense resistor is usually much less than the peak value, although a small RC filter can be added if necessary.

POWER DISSIPATION

In order to achieve the high performance provided by the L6203 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat. The first stage of any thermal design is to calculate the dissipated power in the application, for this example the half step operation shown in figure 16 is considered.

RISE TIME T_r

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r. The dissipated energy $E_{OFF/ON}$ is in this case:

$$E_{OFF/ON} = [R_{DS\ (ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the commutation E_{COM}. As two of the POWER DMOS transistors are ON E_{ON} is given by:

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is:

$$E_{COM} = V_s \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where:

T_{COM} = Commutation Time and it is assumed that;
$T_{COM} = T_{TURN-ON} = T_{TURN-OFF} = 100ns$
f_{SWITCH} = Chopper frequency

FALL TIME T_f

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time:

$$E_{ON/OFF} = [R_{DS(ON)} \cdot I_L^2 \cdot T_f] \cdot 2/3$$

QUIESCENT ENERGY

The last contribution to the energy dissipation is due to the quiescent supply current and is given by:

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_s \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF} + E_{QUIESCENT}$$

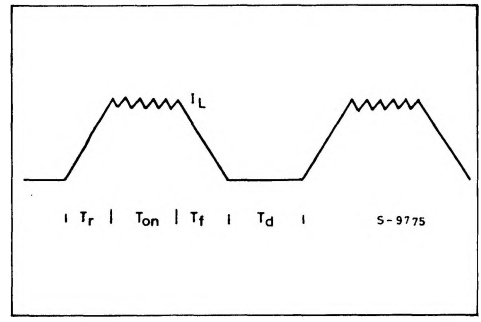
The Total Power Dissipation P_{DIS} is simply:

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time
T_{ON} = ON time
T_f = Fall time
T_d = Dead time
T = Period

$$T = T_r + T_{ON} + T_f + T_d$$

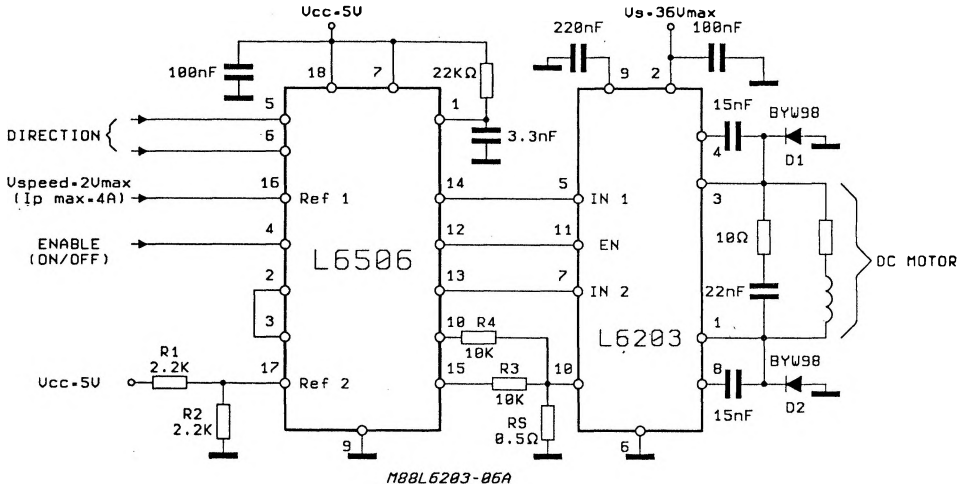
Fig. 16



DC MOTOR SPEED CONTROL

Since the L6203 integrates a full H-Bridge in a single package it si idealy suited for controlling small DC motors. When used for DC motor control the L6203 provides the power stage required for both speed and direction control. The L6203 can be combined with a current regulator like the L6506 to implement a transconductance amplifier for speed control, as shown in figure 17.
In this configuration the L6506 sense the voltage across the sense resistor, R_{SENSE}, to monitor the motor current. The L6506 then compares the sensed voltage to control the speed or during the input signals to the L6203.
Between the sense resistor and each sense input of the L6506 a resistor must be foreseen; if the connections between the outputs of the L6506 and the inputs of the L6202 need a long path, a resistor must be connected between each input of the L6202 and ground.
A snubber network made by the series of R and C must be foreseen very near to the outputs pins of the L6203.
The following formulas can be used :
$R \cong V_s/I_p$
$C = I_p/(dv/dt)$ where
V_s is the max supply voltage foreseen on the application;
I_p is the peak of the load current;
dv/dt is the needed rise time of the output voltage (200V/μsec is generally used).
A diode (BYW98) is connected between each power output pin and ground as well.
If the power supply cannot sink current, a suitable large capacitance must be used and connected near the supply pin of the L6202.
Sometimes a capacitor at pin 17 of the L6506 let application better work.

Fig. 17 - Bidirectional DC motor control



BIPOLAR STEPPER MOTORS APPLICATIONS

Bipolar stepper motors can be driven with an L297 or L6506, two L6203 bridge BCD drivers and very few external components. Together these three chips form a complete microprocessor-to-stepper motor interface.

As shown in Fig. 18 and Fig. 19, the controller connect directly to the two bridge BCD drivers. External component requirements are minimal: an RC network to set the chopper frequency, a resistive divider to establish the comparator reference voltage (pin 15 for L297, pin 10 and 15 for L6506) and a snubber network made by R and C in series.

The following formulas can be used :

$R \simeq V_s/I_p$

$C = I_p/(dv/dt)$ where V_s is the max. Supply Voltage foreseen on the application;

I_p is the peak of the load current;

dv/dt is the needed rise time of the output voltage (200V/μs is generally used). Depending on the Printed Circuit Board design, a resistor between each input of the L6203 and ground could be requested. These solutions have a very high efficiency because of low power dissipation.

HIGH CURRENT MICROSTEP DRIVE FOR STEPPER MOTORS

The L6203 can be used in conjunction with the L6217 to (figure 20) implement a high current microstepping controller for stepper motors.

In this application the L6217 is used as a control circuit and its outputs are used only to drive the inputs of the L6203. The application allows easy interface to a microprocessor since the L6217 may be connected directly to the microprocessor bus.

In the circuit shown in Figure 20, the L6217 senses the motor current by monitoring the voltage across the sense resistors, R_{SENSE}, and compares this value to the output of a 6 bit (7 bit if the L6217A is used) D to A Converter. The L6217 controls the current using a frequency modulated, constant off time, switching controller. The off time of each coil may be set using and external resistor and capacitor connected to PTA and PTB.

In this configuration the microprocessor simply loads the appropriate value for the direction of current flow through the coil and the data for the DAC into the L6217. The L6217 and L6203 then forms the complete interface between the micro and the motor.

When the pins 3 and 4 of the L6217 (Test A and B) are low, the bridges must be in tri-state condition.

For this reason two LM339 comparators must be used. The outputs of the comparators act on the enable inputs of the L6203 ICs.

A bilevel operation can be used for decreasing the minimum controllable load current. The mi-

nimum current that can be controlled is given by the following expression :

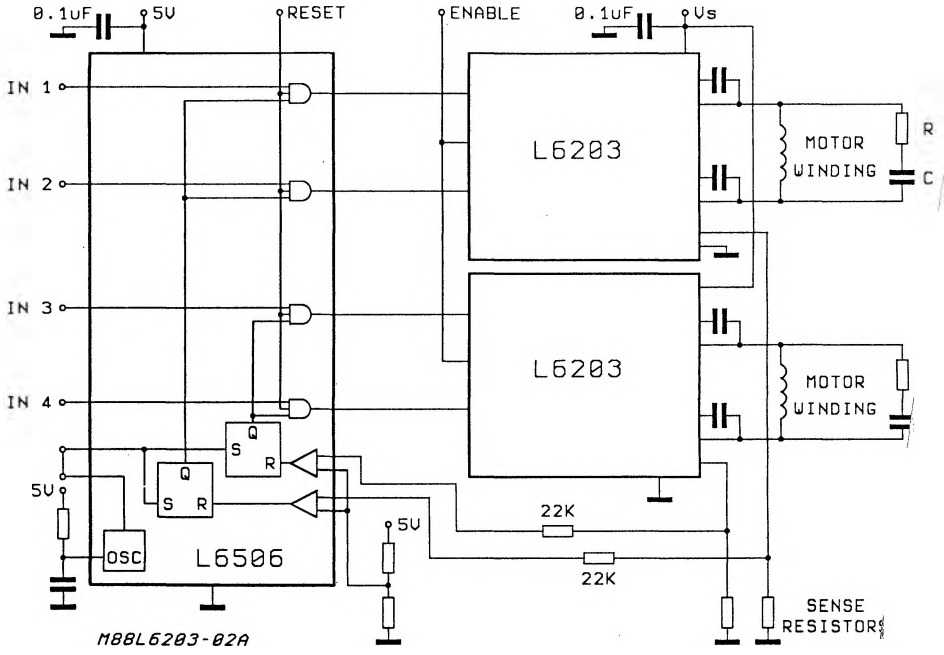
$$I_L \text{ (avg.)} = \frac{V_s}{R_{sense} + (2R_{DSon} + R_{LOAD})/DC}$$

where R_{LOAD} is the equivalent resistance of the load DC is the duty cycle given by

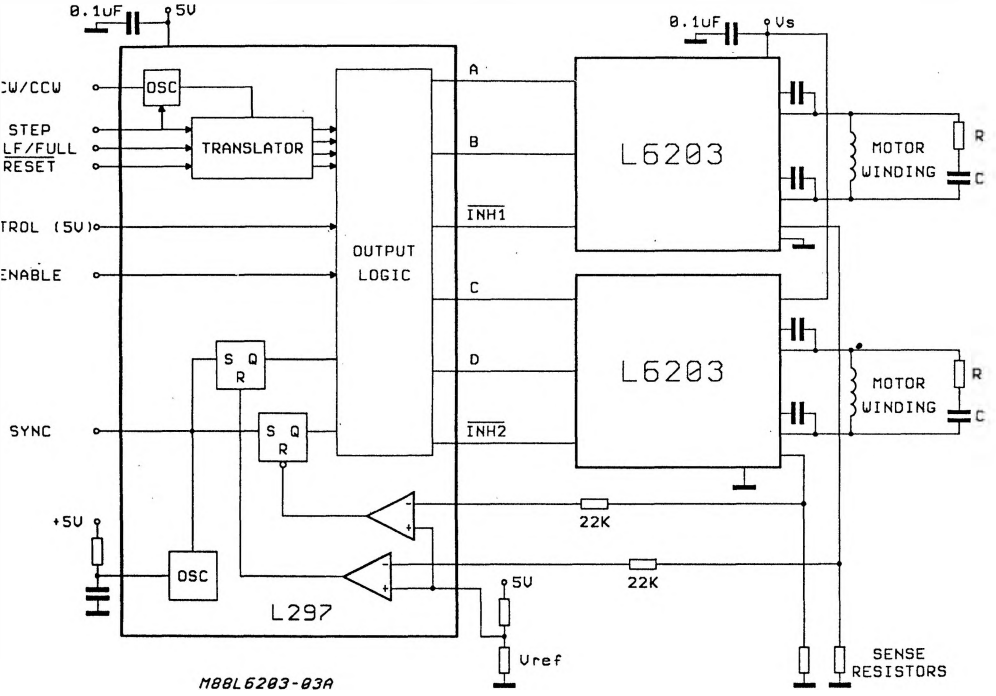
$$\frac{T_{on}}{T_{on} + T_{off}}$$

If 12V is forced on pin (Reference voltage) a the supply voltage V_s is reduced below 12V t on resistance tends to increase above the norm guaranteed 0.3ohm.
Consequently the minimum current will also reduced, as given in the above expression. Wher minimum current operation is required, a high gnal at point (A) can disable the pnp transisto in fig. 20. So it's possible to operate at a V_s (7V - V_{BE}).

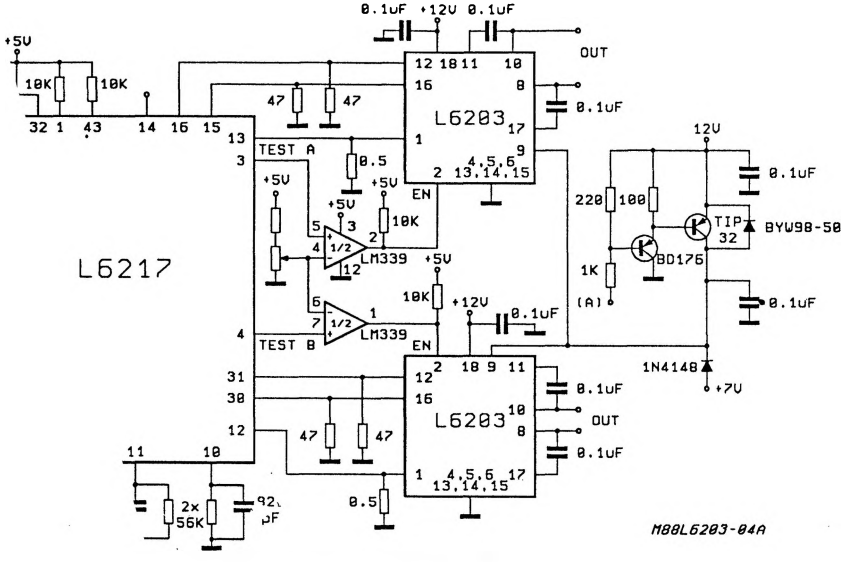
Fig. 18 - Two phase Bipolar stepper motor control circuit with chopper current control



g. 19 - Two phase Bipolar stepper motor control circuit with chopper current control and translator



gh current microstepping controller for stepper motors



THERMAL CHARACTERISTICS

Fig. 21 - $R_{th\ j\text{-}amb}$ of Multiwatt package vs. dissipated power

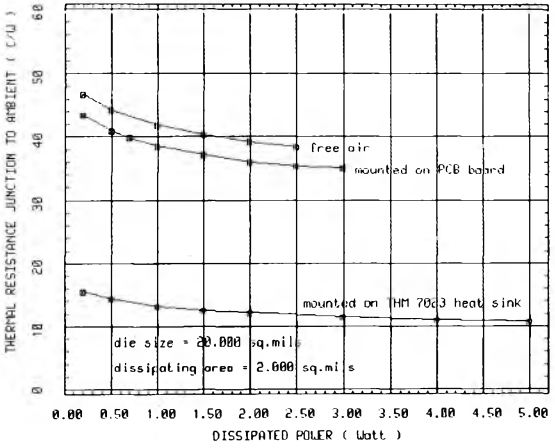
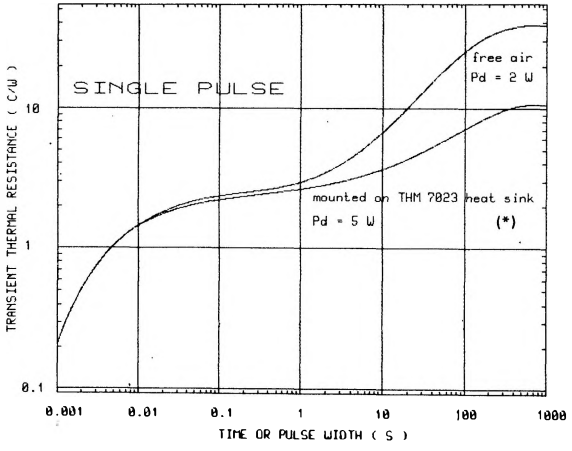


Fig. 22 - Comparison of transient R_{th} for single pulses with and without heatsink



(*) $R_{th} \cong 9°C/W$

g. 23 - Peak transient R_{th} vs. pulse width and duty cycle