SGS-THOMSON
MICROELECTRONICS

L6221A
L6221N

QUAD DARLINGTON SWITCH

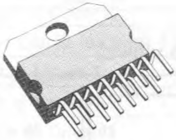
- FOUR NON INVERTING INPUTS WITH ENABLE
- OUTPUT VOLTAGE UP TO 50 V
- OUTPUT CURRENT UP TO 1.8 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

DESCRIPTION

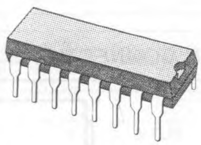
The L6221 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive device loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available : the L6221A mounted in a Powerdip 12 + 2 + 2 package and the L6221N mounted in a 15--lead Multiwatt package.



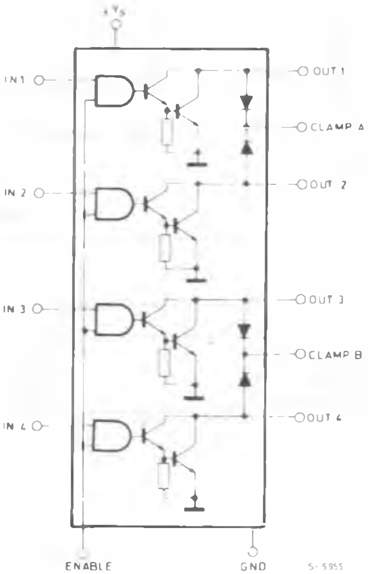
Multiwatt 15



Powerdip 12 + 2 + 2

ORDER CODES : L6221A
L6221N

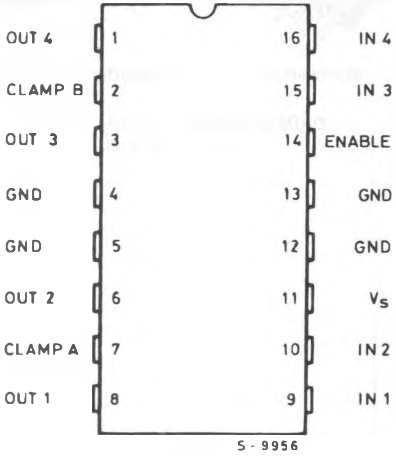
BLOCK DIAGRAM



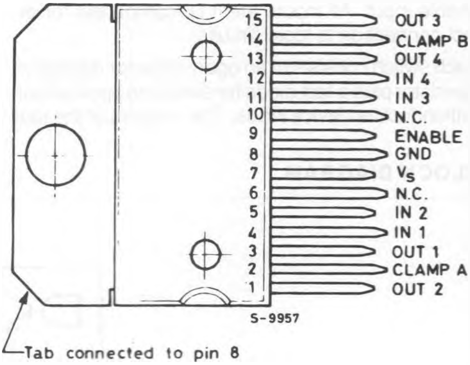
ABSOLUTE MAXIMUM RATINGS

V_o	Output Voltage	50	V
V_s	Logic Supply Voltage	7	V
V_{IN}, V_{EN}	Input Voltage, Enable Voltage	V_s	
I_C	Continuous Collector Current (for each channel)	1.8	A
I_C	Collector Peak Current (repetitive, duty cycle = 10 % t_{on} = 5 ms)	2.5	A
I_C	Collector Peak Current (non repetitive, t = 10 μs)	3.2	A
T_{op}	Operating Temperature Range (junction)	– 40 to + 150	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C
I_{sub}	Output Substrate Current	350	mA
P_{tot}	Total Power Dissipation at T_{pins} = 90 °C (powerdip) at T_{case} = 90 °C (multiwatt) at T_{amb} = 70 °C (powerdip) at T_{amb} = 70 °C (multiwatt)	4.3 20 1 2.3	W W W W

PIN CONNECTIONS (top views)



L6221A (Powerdip)



L6221N (Multiwatt-15)

THERMAL DATA

			Powerdip	Multiwatt-15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	–
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	–	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80 °C/W	35 °C/W

TRUTH TABLE

Enable	Input	Power Out
H	H	ON
H	L	OFF
L	X	OFF

For each input : H = High level
L = Low level
X = Don't care

PIN FUNCTIONS (see block diagram)

Name	Function
IN 1	Input to Driver 1
IN 2	Input to Driver 2
OUT 1	Output of Driver 1
OUT 2	Output of Driver 2
CLAMP A	Diode Clamp to Driver 1 and Driver 2
IN 3	Input to Driver 3
IN 4	Input to Driver 4
OUT 3	Output of Driver 3
OUT 4	Output of Driver 4
CLAMP B	Diode Clamp to Driver 3 and Driver 4
ENABLE	Enable Input to All Drivers
V_S	Logic Supply Voltage
GND	Common Ground

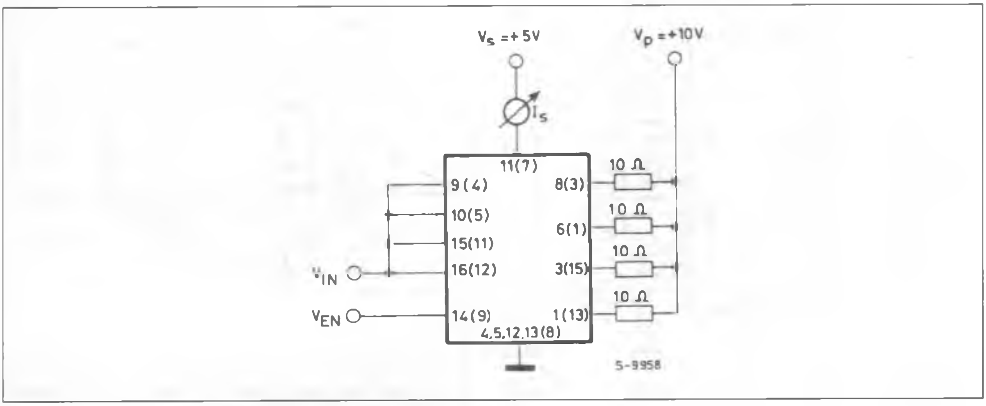
ELECTRICAL CHARACTERISTICS Refer to the test circuit to Fig. 1 to Fig. 9 (VS = 5V, Tamb = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min .	Typ .	Max .	Unit
V_S	Logic Supply Voltage			4.5		5.5	V
I_s	Logic Supply Current	All Outputs ON I_C = 0.7 A				20	m A
		All Outputs OFF				20	m A
$V_{CE(sus)}$	Output Sustaining Voltage	V_{IN} = V_{IN}L V_{EN} = V_{EN}H I_C = 100 mA		46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50V V_{EN} = V_{EN}H V_{IN} = V_{IN}L				1	mA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage (one input on ; all others inputs off.)	V_s = 4.5V V_{IN} = V_{IN}H V_{EN} = V_{EN}H	I_C = 0.6 A			1	V
			I_C = 1 A			1.2	V
			I_C = 1.8 A			1.6	V
V_{IN}L, V_{EN}L	Input Low Voltage					0.8	V
I_{IN}L, I_{EN}L	Input Low Current	V_{IN} = V_{IN}L V_{EN} = V_{EN}L				– 100	µ A
V_{IN}L, V_{EN}H	Input High Voltage			2.0			V
I_{IN}H , I_{EN}H	Input High Current	V_{IN} = V_{IN}H V_{EN} = V_{EN}H				± 10	µ A
I_R	Clamp Diode Leakage Current	V_R = 50 V V_{EN} = V_{EN}H V_{IN} = V_{IN}L				100	µ A
V_F	Clamp Diode Forward Voltage	I_F = 1 A				1.6	V
		I_F = 1.8 A				2.0	V
$t_{d\ (on)}$	Turn on Delay Time	V_p = 5V R_L = 10Ω				2	µ s
$t_{d\ (off)}$	Turn off Delay Time	V_p = 5V R_L = 10Ω				5	µ s
ΔI_s	Logic Supply Current Variation	V_{IN} = 5V V_{EN} = 5V I_{out} = – 500 mA for Each Channel				150	m A

TEST CIRCUITS

(X) = Referred to Multiwatt package
X = Referred to Powerdip package

Figure 1 : Logic supply current.



Set V_{IN} = 4.5V, V_{EN} = 0.8V, or V_{IN} = 0.8V, V_{EN} = 4.5V, for I_S (all outputs off)
Set V_{IN} = 2V, V_{EN} = 2V, for I_S (all outputs on)

Figure 2 : Output Sustaining Voltage.

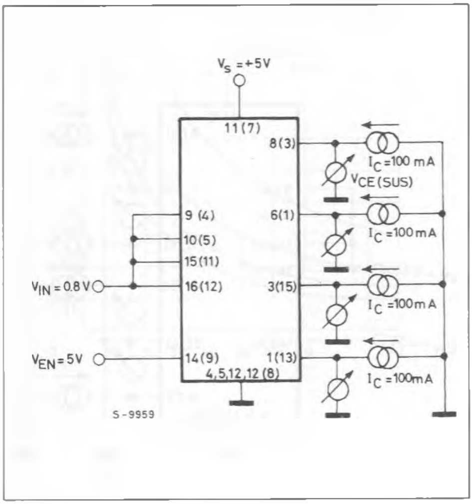


Figure 3 : Output Leakage Current.

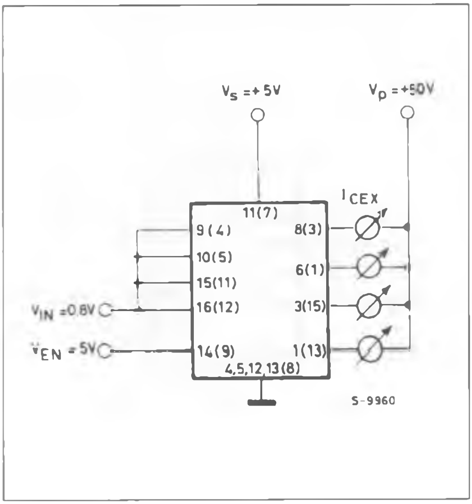


Figure 4 : Collector-emitter Saturation Voltage.

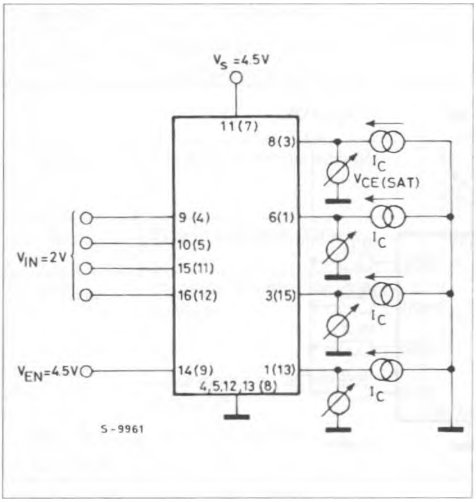
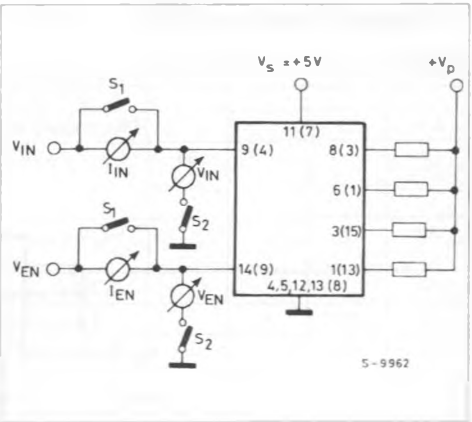


Figure 5 : Logic Input Characteristics.



Set S_1. S_2 open. V_{IN}. V_{EN} = 0.8V for I_{IN} L. I_{EN} L
Set S_1. S_2 open. V_{IN}. V_{EN} = 2V for I_{IN} H. I_{EN} H
Set S_1. S_2 close. V_{IN}. V_{EN} = 0.8V for V_{IN} L. V_{EN} L
Set S_1. S_2 close. V_{IN}. V_{EN} = 2V for V_{IN} H. V_{EN} H

Figure 6 : Clamp Diode Leakage Current.

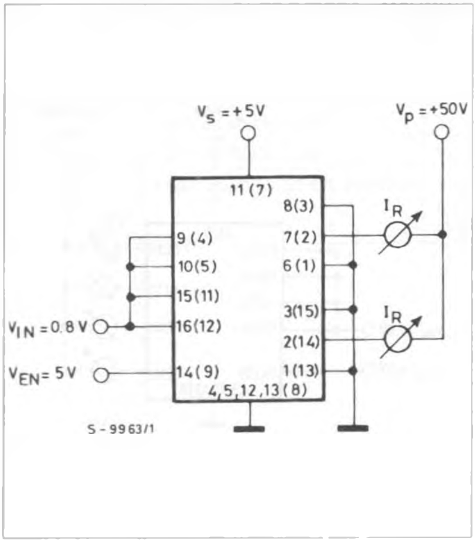


Figure 7 : Clamp Diode Forward Voltage.

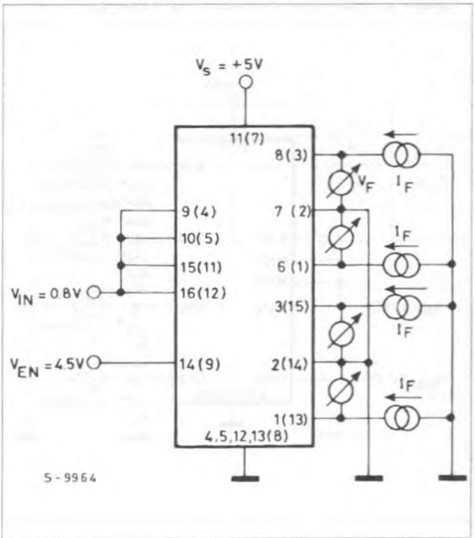


Figure 8 : Switching Times Test Circuit.

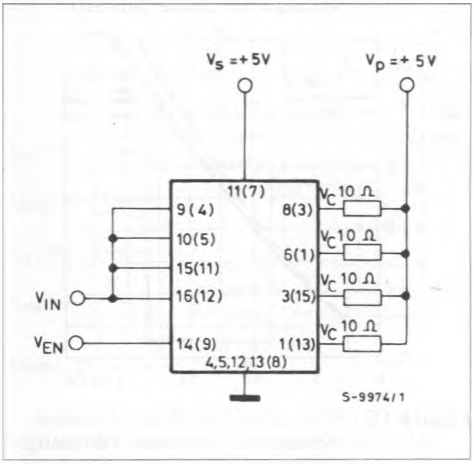


Figure 9 : Switching TImes Waveforms.

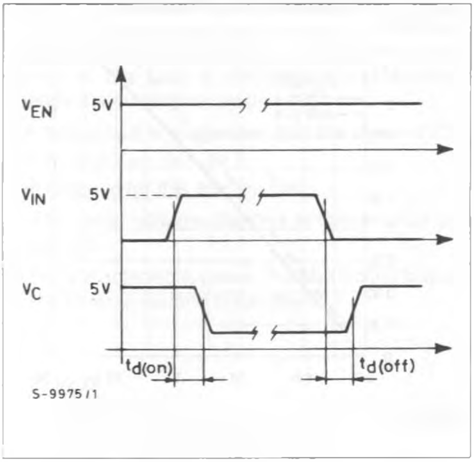


Figure 10 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221A).

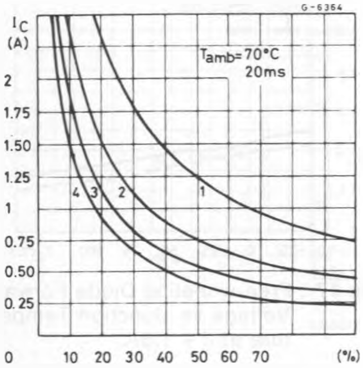


Figure 11 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221N).

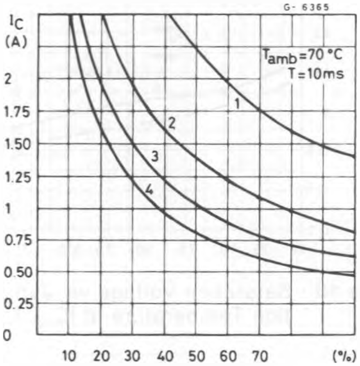


Figure 12 : Collector Saturation Voltage vs. Collector Current.

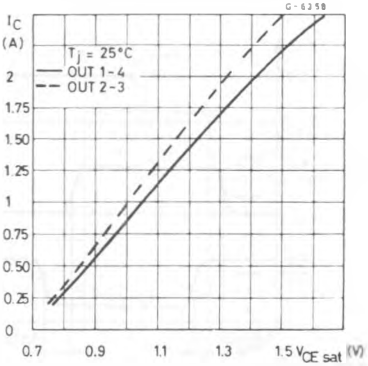


Figure 13 : Free-wheeling Diode Forward Voltage vs. Diode Current.

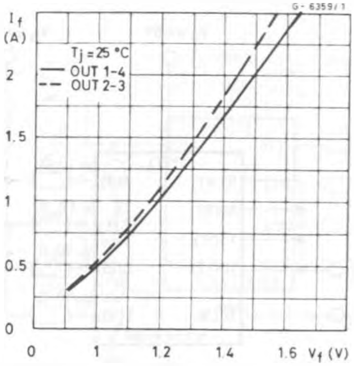


Figure 14 : Collector Saturation Voltage vs. Junction Temperature at I_C = 1A.

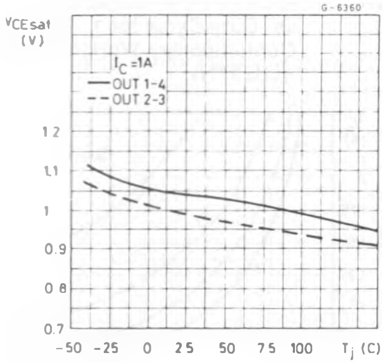


Figure 15 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at I_F = 1A.

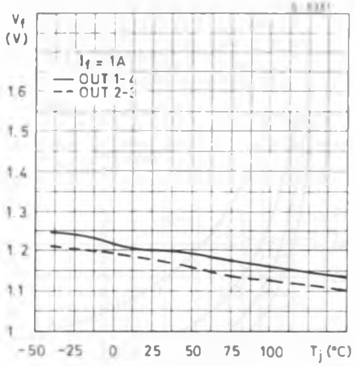


Figure 16 : Saturation Voltage vs. Junction Temperature at IC = 1.8A.

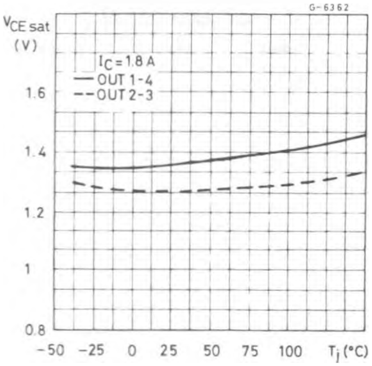
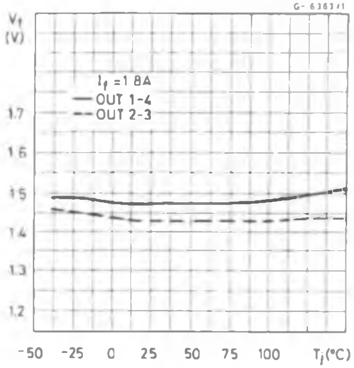


Figure 17 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at If = 1.8A.



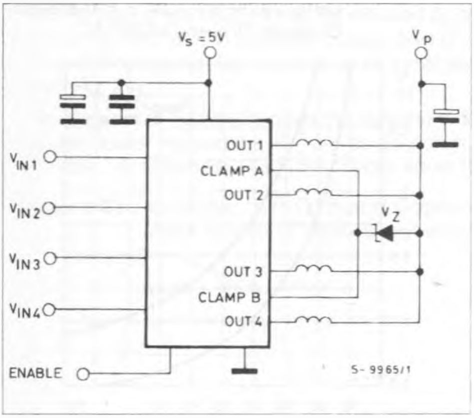


Figure 18.

APPLICATION INFORMATION

When inductive loads are driven by L6221A/N, a zener diode in series with the integral free-wheeling diodes increases the voltage across which energy stored in the load is discharged and therefore speeds the current decay (fig. 18).

For reliability it is suggested that the zener is chosen so that $V_p + V_z < 35$ V.

The reasons for this are two fold :

1) The zener voltage changes in temperature and current.

2) The instantaneous power must be limited to avoid the reverse second breakdown.

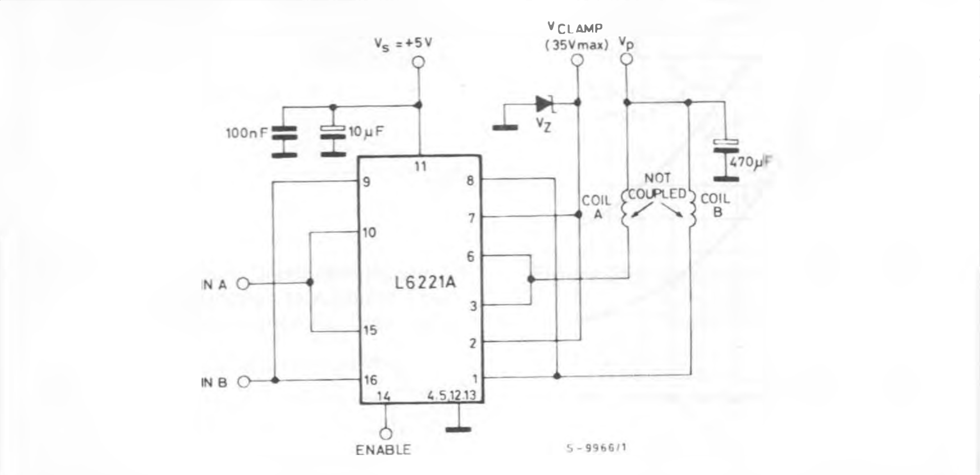


Figure 19 : Driver for Solenoids up to 3A.

Some care must be taken to ensure that the collectors are placed close together to avoid different current partitioning at turn-off.

We suggest to put in parallel channel 1 and 4 and channel 2 and 3 as shown in figure 19 for the similar electrical characteristics of the logic section (turn-on and turn-off delay time) and the power stages (collector saturation voltage, free-wheeling diode forward voltage).

Figure 20 : Saturation Voltage vs. Collector Current.

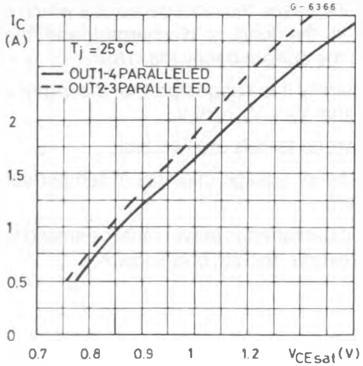


Figure 21 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221A).

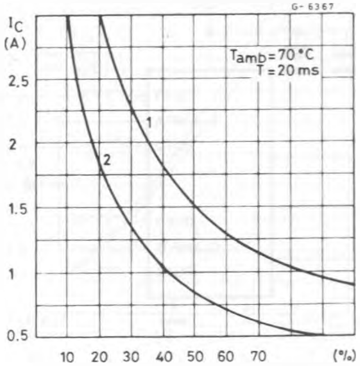
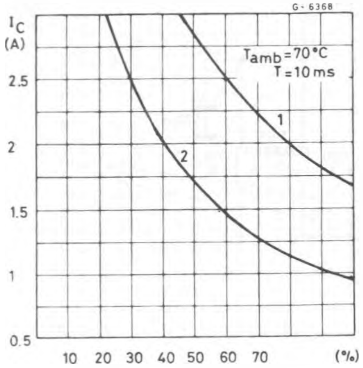


Figure 22 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221N).



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L6221A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 23) or to an external heatsink (Fig. 24).

The diagram of figure 25 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side " α" of two equal square copper areas having a thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 23 : Example of P.C. Board Copper Area Which is Used as Heatsink.

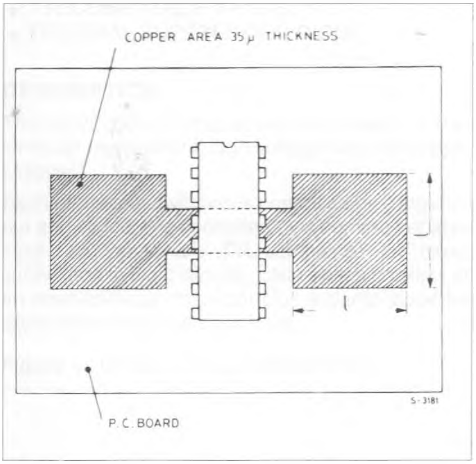


Figure 24 : External Heatsink Mounting Example.

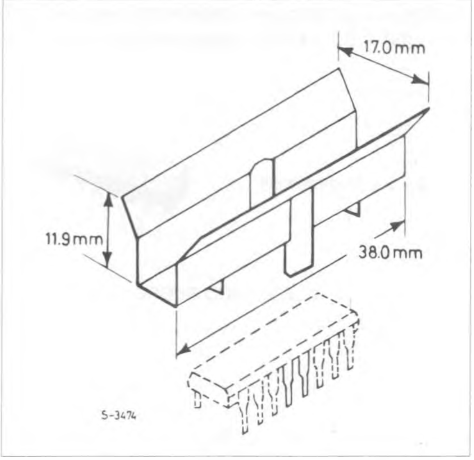


Figure 25 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side " α".

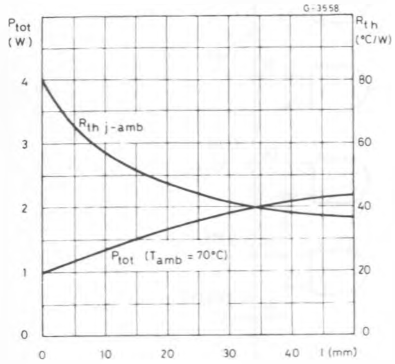


Figure 26 : Maximum Allowable Power Dissipation vs. Ambient Temperature.