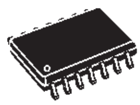
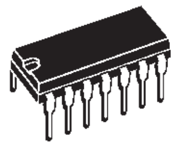
L6386

HIGH-VOLTAGE HIGH AND LOW SIDE DRIVER

- HIGH VOLTAGE RAIL UP TO 600V
- dV/dt IMMUNITY +- 50 V/nsec iN FULL TEMPERATURE RANGE
- DRIVER CURRENT CAPABILITY:
  400 mA SOURCE,
  650 mA SINK
- SWITCHING TIMES 50/30 nsec RISE/FALL WITH 1nF LOAD
- CMOS/TTL SCHMITT TRIGGER INPUTS WITH HYSTERESIS AND PULL DOWN
- UNDER VOLTAGE LOCK OUT ON LOWER AND UPPER DRIVING SECTION
- INTEGRATED BOOTSTRAP DIODE
- OUTPUTS IN PHASE WITH INPUTS



SO14



DIP14

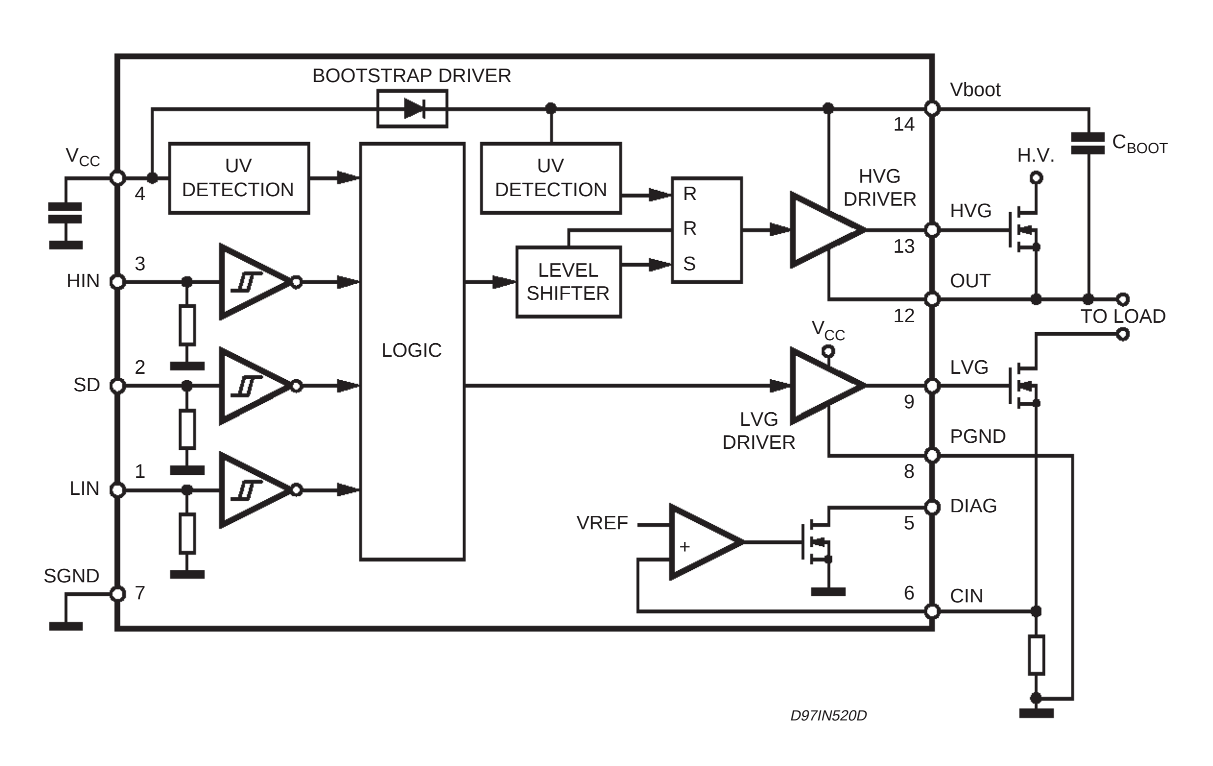
ORDERING NUMBERS:

SO14	DIP14
L6386D	L6386

DESCRIPTION

The L6386 is an high-voltage device, manufactured with the BCD ”OFF-LINE” technology. It has a Driver structure that enables to drive independent referenced Channel Power MOS or IGBT. The Upper (Floating) Section is enabled to work with voltage Rail up to 600V. The Logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices.

BLOCK DIAGRAM

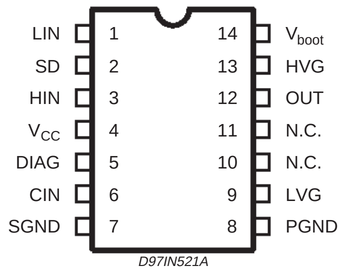


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vout	Output Voltage	-3 to Vboot - 18	V
Vcc	Supply Voltage	- 0.3 to +18	V
Vboot	Floating Supply Voltage	-1 to 618	V
Vhvg	Upper Gate Output Voltage	- 1 to Vboot	V
Vlvg	Lower Gate Output Voltage	-0.3 to Vcc +0.3	V
Vi	Logic Input Voltage	-0.3 to Vcc +0.3	V
Vdiag	Open Drain Forced Voltage	-0.3 to Vcc +0.3	V
Vcin	Comparator Input Voltage	-0.3 to Vcc +0.3	V
dVout/dt	Allowed Output Slew Rate	50	V/ns
Ptot	Total Power Dissipation (Tj = 85 °C)	750	mW
Tj	Junction Temperature	150	°C
Ts	Storage Temperature	-50 to 150	°C

Note: ESD immunity for pins 12, 13 and 14 is guaranteed up to 900V (Human Body Model)

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	SO14	DIP14	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	165	100	°C/W

PIN DESCRIPTION

N.	Name	Type	Function
1	LIN	I	Lower Driver Logic Input
2	SD (*)	I	Shut Down Logic Input
3	HIN	I	Upper Driver Logic Input
4	VCC	I	Low Voltage Supply
5	DIAG	O	Open Drain Diagnostic Output
6	CIN	I	Comparator Input
7	SGND		Ground
8	PGND		Power Ground
9	LVG (*)	O	Low Side Driver Output
10, 11	N.C.		Not Connected
12	OUT	O	Upper Driver Floating Driver
13	HVG (*)	O	High Side Driver Output
14	Vboot		Bootstrapped Supply Voltage

(*) The circuit guarantees 0.3V maximum on the pin (@ Isink = 10mA), with VCC >3V. This allows to omit the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vout	12	Output Voltage		Note1		580	V
Vboot-Vout	14	Floating Supply Voltage		Note1		17	V
fsw		Switching Frequency	HVG,LVG load CL = 1nF			400	kHz
Vcc	4	Supply Voltage				17	V
T_j		Junction Temperature		-45		125	°C

Note 1: if the condition Vboot - Vout < 18V is guaranteed, Vout can range from -3 to 580V.

ELECTRICAL CHARACTERISTICS
AC Operation (Vcc = 15V; Tj = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ton	1.3 vs 9, 13	High/Low Side Driver Turn-On Propagation Delay	Vout = 0V		110	150	ns
toff		High/Low Side Driver Turn-Off Propagation Delay	Vout = 0V		105	150	ns
tsd	2 vs 9,13	Shut Down to High/Low Side Propagation Delay	Vout = 0V		105	150	ns
tr	13,9	Rise Time	CL = 1000pF		50		ns
tf	13,9	Fall Time	CL = 1000pF		30		ns

DC Operation (Vcc = 15V; Tj = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Low Supply Voltage Section							
Vcc	4	Supply Voltage				17	V
Vccth1		Vcc UV Turn On Threshold		11.5	12	12.5	V
Vccth2		Vcc UV Turn Off Threshold		9.5	10	10.5	V
Vcchys		Vcc UV Hysteresis			2		V
Iqccu		Undervoltage Quiescent Supply Current	Vcc ≤ 11V		200		µA
Iqcc		Quiescent Current	Vcc = 15V		250	320	µA
Bootstrapped Supply Section							
Vboot	14	Bootstrapped Supply Voltage				17	V
Vbth1		Vboot UV Turn On Threshold		10.7	11.9	12.9	V
Vbth2		Vboot UV Turn Off Threshold		8.8	9.9	10.7	V
Vbhys		Vboot UV Hysteresis			2		V
Iqboot		Vboot Quiescent Current	Vout = Vboot			200	µA
Ilk		Leakage Current	Vout = Vboot = 600V			10	µA
Rdson		Bootstrap Driver on Resistance (*)	Vcc ≥ 12.5V; Vin = 0V		125		Ω
Driving Buffers Section							
Iso	9, 13	High/Low Side Driver Short Circuit Source Current	VIN = Vih (tp < 10µs)	300	400		mA
Isi		High/Low Side Driver Short Circuit Sink Current		500	650		mA
Logic Inputs							
Vil	1,2,3	Low Level Logic Threshold Voltage				1.5	V
Vih		High Level Logic Threshold Voltage		3.6			V
Iih		High Level Logic Input Current	VIN = 15V		50	70	µA
Iil		Low Level Logic Input Current	VIN = 0V			1	µA

(*) R_{DSON} is tested in the following way: $R_{DSON} = \frac{(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})}{I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})}$

where I_1 is pin 8 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$.

DC OPERATION (continued)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Sense Comparator							
Vio		Input Offset Voltage		-10		10	mV
Iio	6	Input Bias Current	Vcin ≥ 0.5		0.2		µA
Vol	2	Open Drain Low Level Output Voltage, Iod = -2.5mA				0.8	V
Vref		Comparator Reference voltage		0.460	0.5	0.540	V

Figure 1. Timing Waveforms

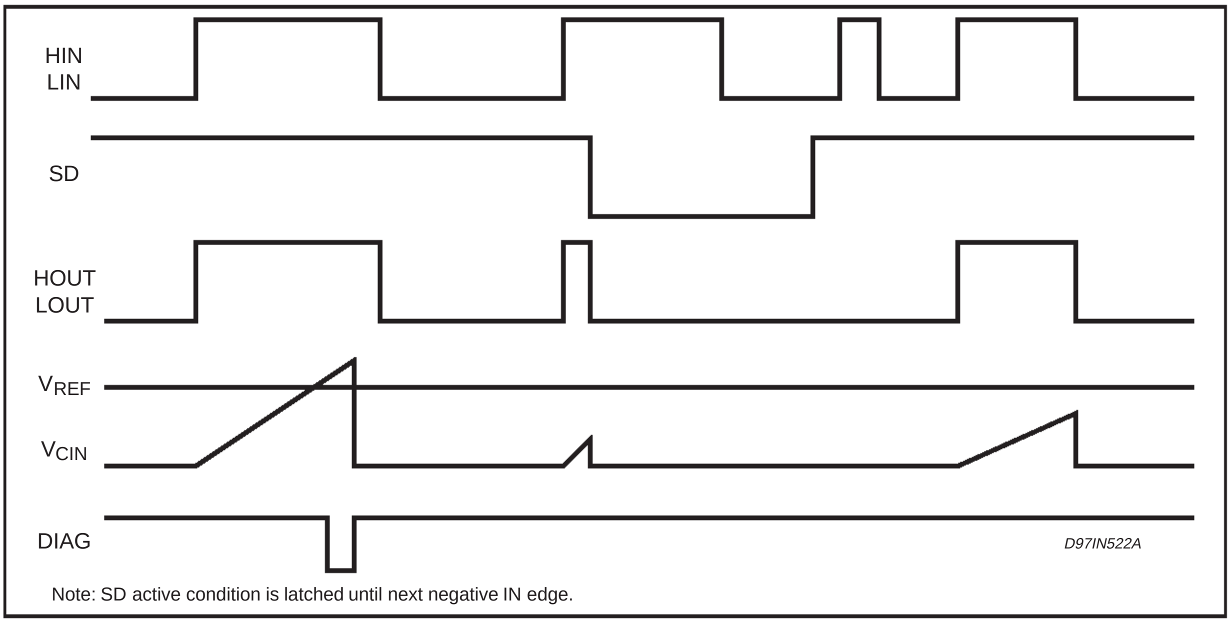


Figure 2. Typical Rise and Fall Times vs. Load Capacitance

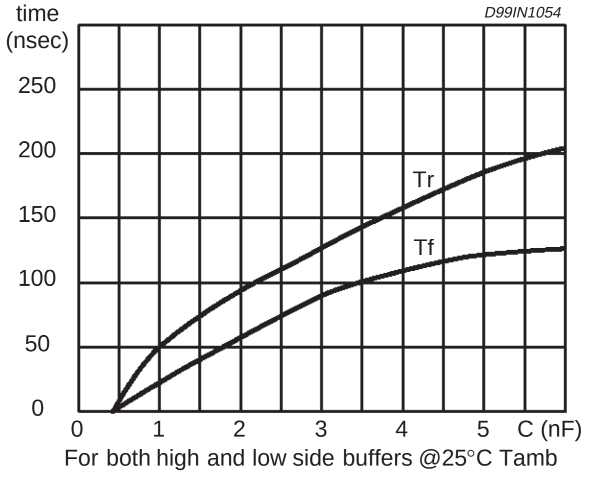
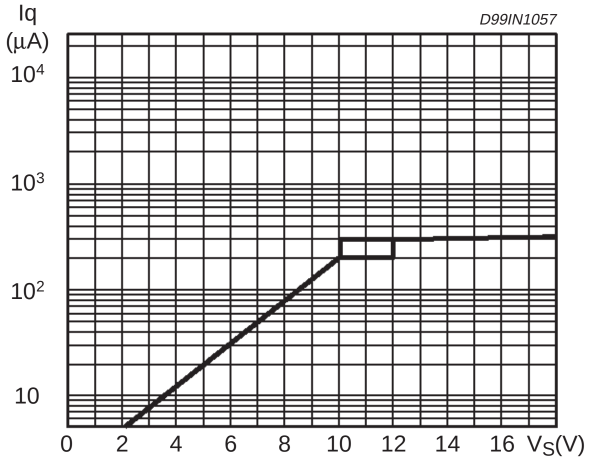


Figure 3. Quiescent Current vs. Supply Voltage



BOOTSTRAP DRIVER

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (fig. 4a). In the L6386 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in fig. 4b

An internal charge pump (fig. 4b) provides the DMOS driving voltage .

The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

CBOOT selection and charging:

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge :

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss .

It has to be:

$$C_{BOOT} >>> C_{EXT}$$

e.g.: if Q_{gate} is 30nC and V_{gate} is 10V, C_{EXT} is 3nF. With C_{BOOT} = 100nF the drop would be 300mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than 200µA, so if HVG T_{ON} is 5ms, C_{BOOT} has to supply 1µC to C_{EXT}. This charge on a 1µF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current). This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSON} (typical value: 125 Ohm). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge}R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}}R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the T_{charge} is 5µs. In fact:

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 4. Bootstrap Driver.

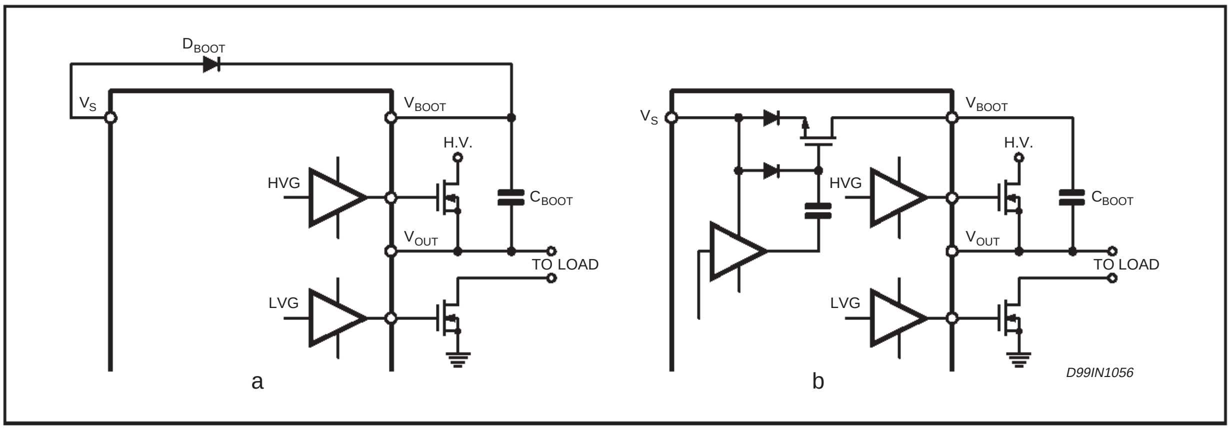


Figure 5. Turn On Time vs. Temperature

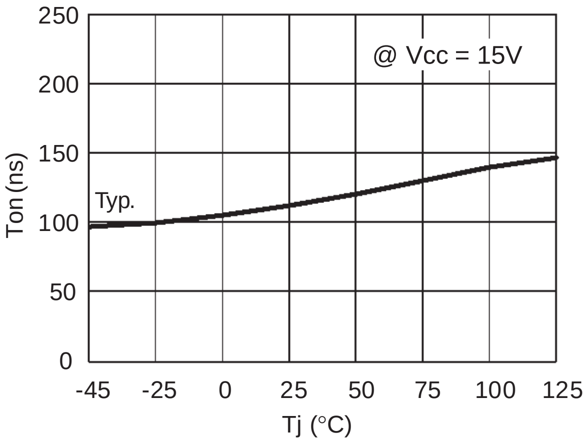


Figure 6. Turn Off Time vs. Temperature

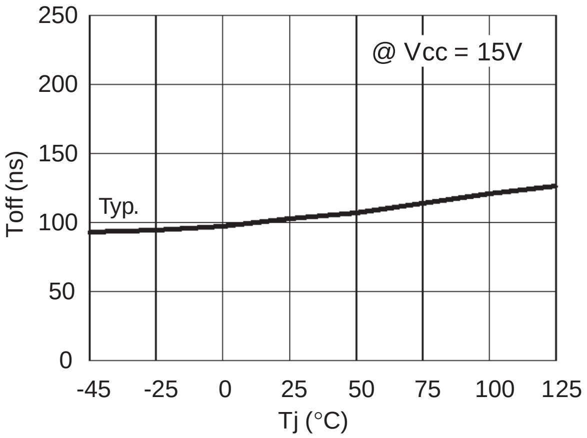


Figure 7. Shutdown Time vs. Temperature

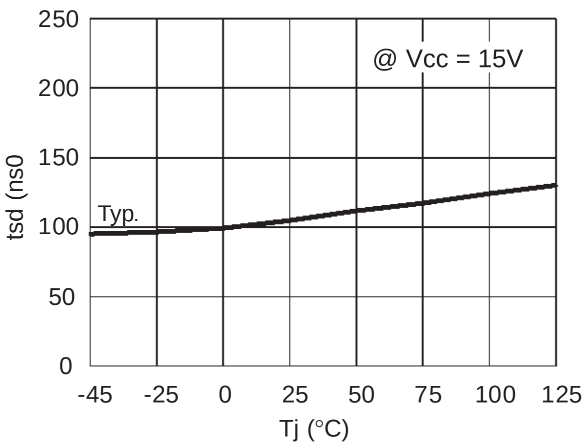


Figure 8. V_{BOOT} UV Turn On Threshold vs. Temperature

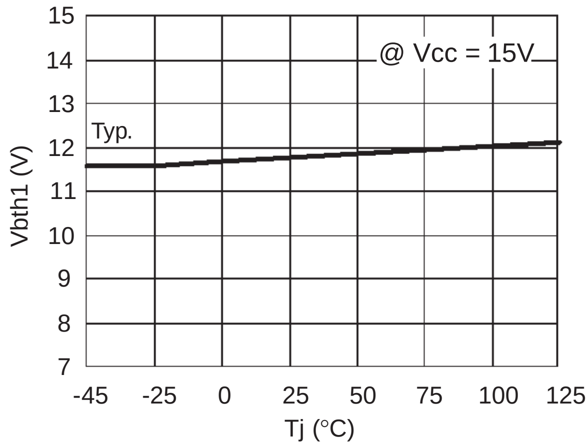


Figure 9. V_{BOOT} UV Turn Off Threshold vs. Temperature

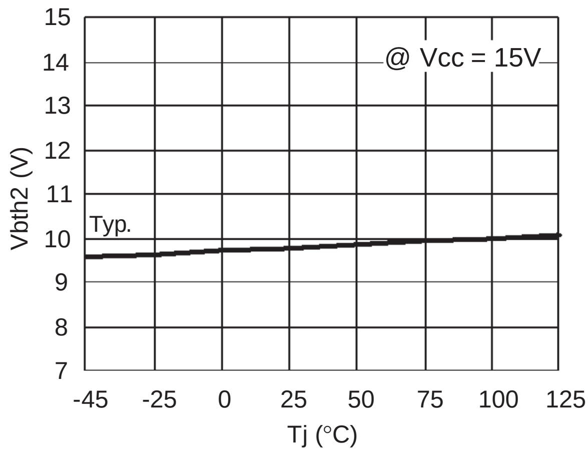


Figure 10. V_{BOOT} UV Hysteresis

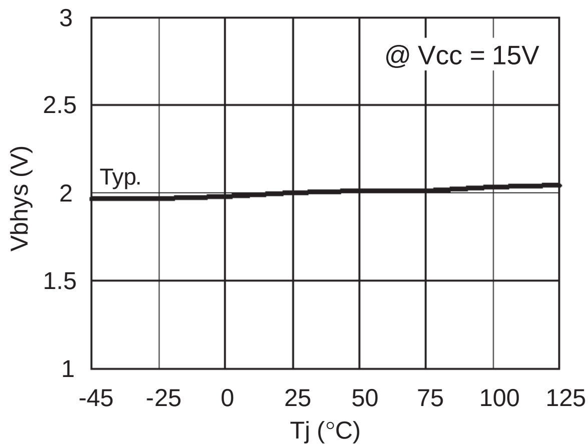


Figure 11. Vcc UV Turn On Threshold vs. Temperature

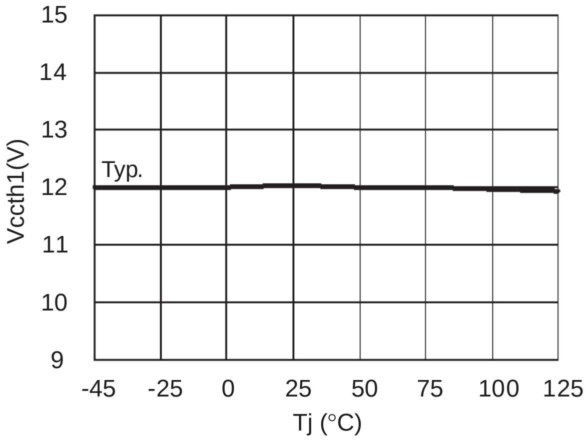


Figure 12. Vcc UV Turn Off Threshold vs. Temperature

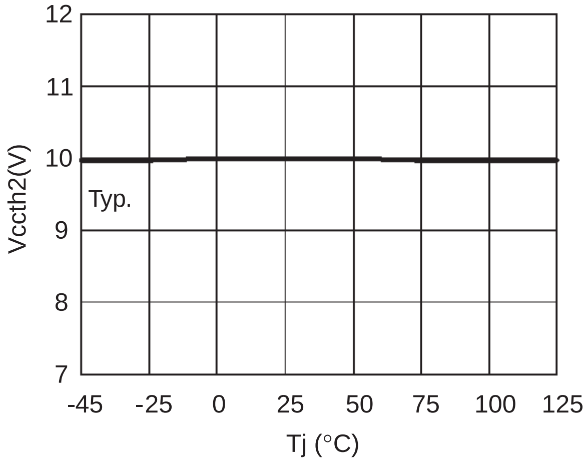


Figure 13. Vcc UV Hysteresis vs. Temperature

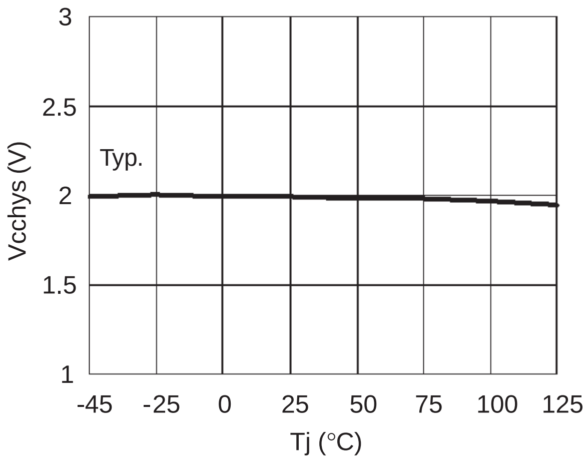


Figure 14. Output Source Current vs. Temperature

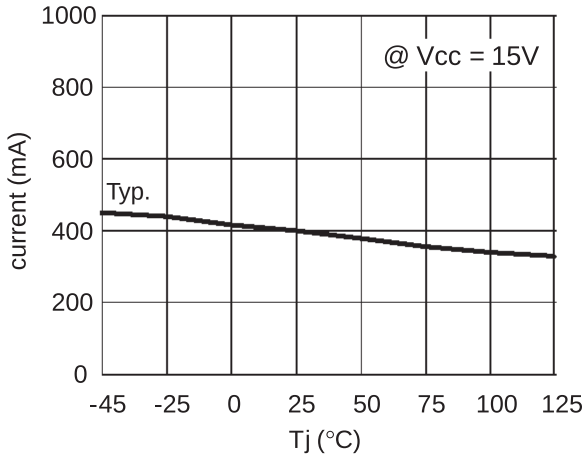
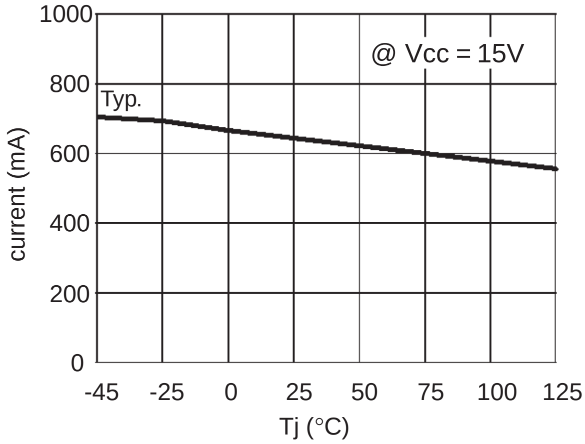
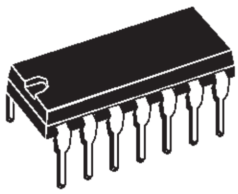


Figure 15. Output Sink Current vs. Temperature

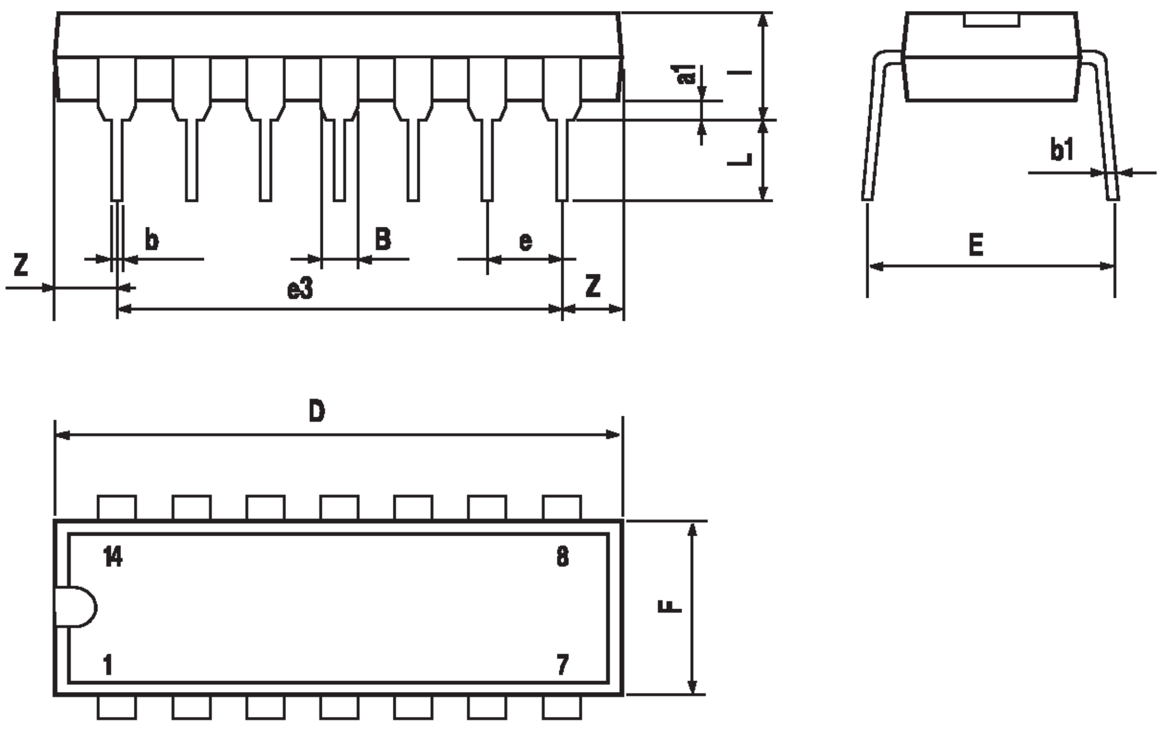


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

OUTLINE AND MECHANICAL DATA



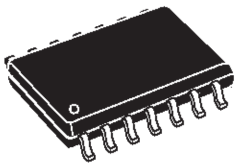
DIP14



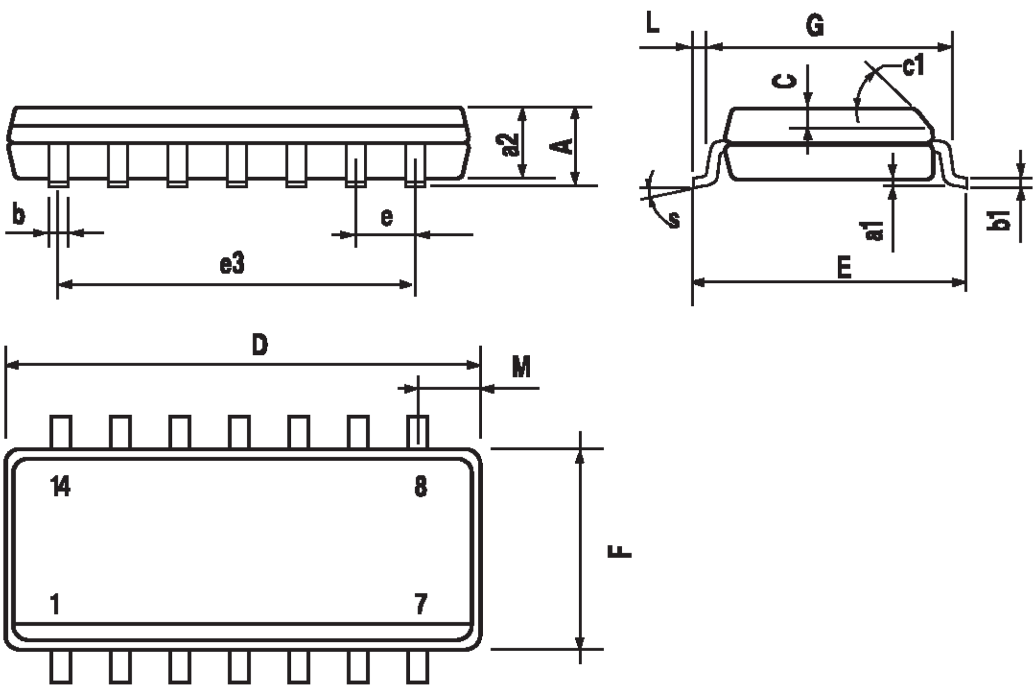
DIM.	mm			inch		
	MIN..	TYP.	MAX..	MIN..	TYP..	MAX..
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F (1)	3.8		4	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.68			0.027
S	8° (max)					

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA



SO14



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