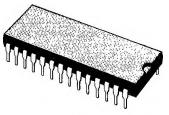
SGS-THOMSON MICROELECTRONICS

L6603
L6604

MEMORY CARD INTERFACE

ADVANCE DATA

- Single Power Supply operation
- Internal Clock Generator or External Clock Input
- Adjustable Precision of PVS Output Voltage (2 %)
- 100 mV/step of the Writing Output Voltage
- I/O, Reset and Clock Outputs Protection Against Short Circuit to GND and to V_{pvs}.



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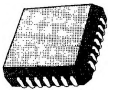
ORDER CODE : L6603



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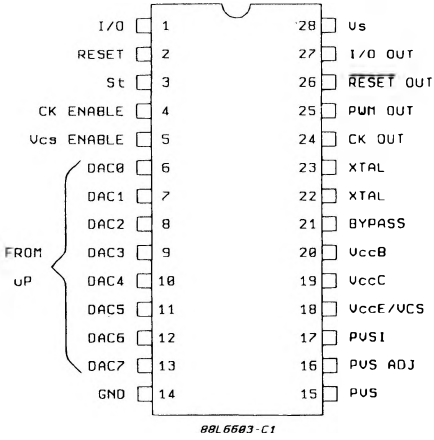
DESCRIPTION

The L6603 and L6604 are integrated circuits for application as interface between different types of memory card and a microprocessor which excanges data with cards. Its operate with a single power supply.

CONNECTION DIAGRAMS



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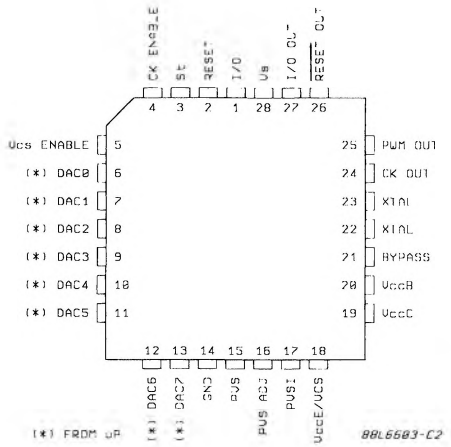

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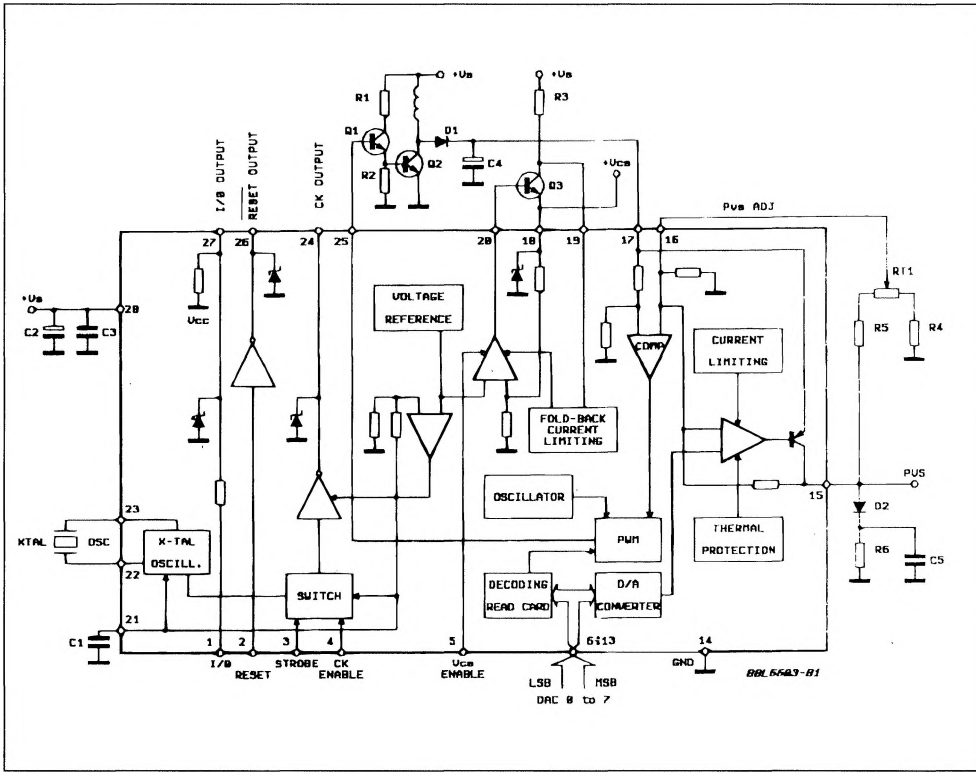
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Supply Voltage	10	V
T_{op}	Operating Temperature Range	– 20 to 70	°C
T_{stg}	Storage Temperature Range	– 40 to 150	°C

THERMAL DATA (*)

			DIP 28	PLCC 28	
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	100	°C/W

(*) With all the pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

Pin	Name	Function
1	I/O	Input of the Bidirectional Data Line
2	RESET	Control Input for Reset of Memory Card FA Function
3	St	Strobe for Card with Memory (TTL compatible)
4	CK ENABLE	Commutation for µP Cards CK ENABLE = 1 (internal clock)
5	VCS ENABLE	Control Input for VCS Supply Voltage
6 to 13	DACO to DAC7	Control Inputs for Programmation of V_{PVS} Supply (see operation of programming supply V_{PVS})
14	GND	Ground
15	V_{PVS}	Programmable Supply for Memory Card (no use with decoupling capacitor) Note 7 (to the credit card)
16	V_{PVS} Adj	Adjustment Input for 2 % Precision V_{PVS} Output
17	PVS I	Input for V_{PVS} Regulator
18 19 20	V_{CS} V_{CC} E C B	Inputs for Connection of Power Transistor (V_{CC} regulator) (decoupling capacitor on pin 18 > 100 nF if necessary) Note 8 (pin 18 to the credit card)
21	BYPASS	Output Voltage of Regulator for Clock Circuits (decoupling capacitor > 150 nF). Note 9
22 23	XTAL XTAL	Inputs for X-tal Connection. Note 10
24	CK OUT	Output for Clock Signal (TTL levels). Note 11 (to the credit card)
25	PWM OUT	Output for DC/DC Converter
26	$\overline{\text{RESET}}$/OUT	Reset Output. Note 11 (to the credit card)
27	I/O Out	Output I/O. Note 11 (to the credit card)
28	V_S	General Power Supply

Note 1 For inputs V_{vss} enable, Reset, I/0, St, CK enable DAC (0 - 7).
Note 2 For inputs DAC (0 - 7)
Note 3 For input CK enable
Note 4 For input Reset
Note 5 For input V_{vcs} enable
Note 6 For input I/0
Note 7 Typical internal thermal protection & current limiting system
Note 8 Current limiting with "fold back system"

$$I_{lim}\ max\ (A) = \frac{0.75\ V}{Rlim}$$

Note 9 Internal current limiting system
Note 10 Input for external clock (fig. 3)
Note 11 Output protected against short-circuit to ground and to & V_{pvs}

ELECTRICAL CHARACTERISTICS (V_S = 8.5 V ; T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Note
V_{IH}	Input High Voltage		2			V	1
V_{IL}	Input Low Voltage				0.8	V	1
I_{IH}	Input High Current				250	µA	2
					500	µA	3
					100	µA	4
					400	µA	5
					– 200	µA	6
I_{IL}	Input Low Current				– 150	µA	2
					– 300	µA	3
					+ 10	µA	4
					– 200	µA	5
					– 300	µA	6
I_{SW}	Supply Current Writing Mode (pin 28)	$V_{PVS} = V_{PVSW}$ max	tbd			mA	
I_{SR}	Supply Current Reading Mode (pin 28)	$V_{PVS} = V_{PVSR}$	tbd			mA	
V_{CS}	Output Voltage Range	V_S = 7 to 10 V ; I_{CS} = 0 to – 200 mA ; T_{amb} = – 20 to 70 °C ;	4.8	5	5.2	V	
$\frac{\Delta V_{CS}}{\Delta V_{CS}}$	Load Regulation	I_{CS} = 0 to – 200 mA		0.18		%	
$\frac{\Delta V_{CS}}{\Delta V_S}$	Line Regulation	V_S = 7 to 10 V ;		– 50		dB	
$\frac{\Delta V_{CS}}{\Delta T}$	Temperature Coeff. of Output Voltage V_{CS}	T_{amb} = – 20 to 70 °C		65		dB	
t_{off1}	Fall Time of V_{CS}	Fig. 1 CL = 30 pF		5	25	µs	
t_{off2}	Fall Time of V_{PVS}	Fig. 1 CL = 30 pF ; ΔV_{PVS} = 0.1 V		40	100	µs	
$I_{CS\ max}$	Operating Curr. Limit	V_{CS} = – 4 % ; R_{lim} = 3 ohm	– 220			mA	
I_{CS1}	Short Circuit Current limit			– 70	– 100	mA	
$V_{PVSWMAX}$	Maximum Programming Voltage (writing mode memory)	V_S = 7 to 10 V ; I_{PVS} = 0 to – 50 mA ;	24.5	25.5	26.5	V	
$V_{PVSWMIN}$	Minimum Programming Voltage (writing mode memory)	V_S = 7 to 10 V ; I_{PVS} = 0 to – 50 mA ;	4.9	5.1	5.3	V	
V_{PVSR}	Output Voltage Range of PVSP (reading mode memory)	V_S = 7 to 10 V ; I_{PVS} = 0 to – 20 mA ;	4.8	5	5.2	V	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Note
$\frac{\Delta V_{PVS}}{V_{PVS}}$	Load Regulation	I_{PVS} = 0 to – 50 mA ;		0.8		%	
$\frac{\Delta V_S}{\Delta V_{PVS}}$	Line Regulation	I_{VPS} = 0 mA ; V_S = 7 to 10 V		50		dB	
$\frac{\Delta V_{PVS}}{\Delta T}$	Temperature coeff. of Ouptut Voltage V_{PVS}	I_{PVS} = 0 mA ; T_{amb} = – 20 to 70 °C		74		dB	
I_{PVSMAX}	Short Circuit Current Limit		– 50	– 65	– 80	mA	
V_{PVS} ADJ – V_{CS}	Differential Volt. between V_{PVS} (reading mode) & V_{CS}		– 5		5	%	
t_{pLH1}	Turn ON Time of V_{CS}	Fig. 1 CL = 30 pF ;		12	50	µs	
t_{pLH2}	Turn ON Time of V_{PVS}	Fig. 1 CL = 30 pF ; ΔV_{PVS} = 0.1 V		25	100	µs	
t_{on1}	Rise Time of V_{CS}	Fig. 1 CL = 30 pF ;		10	50	µs	
t_{on2}	Rise Time of V_{PVS}	Fig. 1 CL = 30 pF; ΔV_{PVS} = 0.1 V		30	100	µs	

ELECTRICAL CHARACTERISTICS (V_S = 8.5 V ; T_{amb} = 25 °C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Note
V_{OH1}	High Output Voltage (pin 26)	(PIN 26) V_{CS} min I_{OH} = – 200/µA	4.2	4.8		V	
V_{OL1}	Low Output Voltage (pin 26)	(PIN 26) V_{IH} = 2 V ; I_{OL} = + 200/µA		0.15	0.4	V	
V_{SC1}	Max Output Voltage during Short-circuit between V_{PVS} and Pin 26				V_{CS} + 0.3	V	
I_{SC2}	Short-circuit Curr. Limit (pin 26)				– 0.5	mA	
V_{OH2}	High Output Voltage (pin 27)	V_{CS} min ; I_{OH} = – 500/µA V_{IH} max = 2 V	1.9			V	
V_{OL2}	Low Output Voltage (pin 27)	V_{CS} max ; I_{OL} = + 200/µA V_{IH} min = 0.8 V			0.9	V	
V_{SC2}	Max Output Voltage during Short-circuit between V_{PVS} and Pin 27				V_{CS} + 0.3	V	
I_{SC3}	Short-circuit Curr. Limit (pin 27)	I/O = 4.2 V			– 30	mA	
V_{OH3}	High Output Voltage (pin 24)	I_{OH} = – 200/µA	3.5	4.1		V	
V_{OH4}	High Output Voltage (pin 24)	I_{OH} = – 10/µA	4.1	4.2		V	
V_{OL3}	Low Output Voltage (pin 24)	I_{OL} = + 200/µA		0.1	0.4	V	
V_{SC3}	Max Output Voltage during Short-circuit between Pin 24 & V_{PVS} Output				V_{CS} + 0.3	V	
I_{SC4}	Short-Circuit Curr. Limit (pin 24)				– 35	mA	
t_{on}	Rise Time of Clock Output (pin 24)	Fig. 2 f_{XTAL} = 4.91 MHz ; CL = 30 pF		15		ns	
t_{off}	Fall Time of Clock Output (pin 24)	Fig. 2 f_{XTAL} = 4.91 MHz ; CL = 30 pF		18		ns	
	Duty Cycle (T1/T)	f_{XTAL} = 4.91 MHz ; CL = 30 pF	40		60	%	

OPERATION OF PROGRAMMING SUPPLY V_{PVS}

The output voltage V_{pvs} can be programmed from 5 V to 25.5 V by steps of 0.1 V and can be expressed as follows :

$$V_{pvs} = \frac{\text{code DAC 0-7}}{10}$$

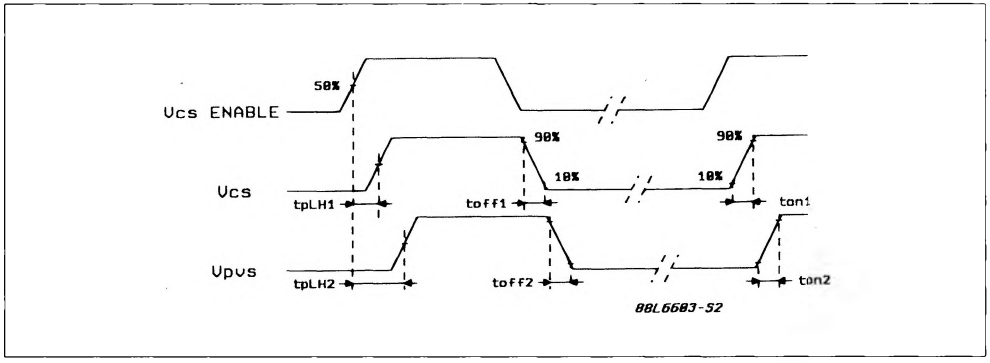
Two operating modes are possible

Reading mode (code DAC = 50) : V_{pvs} = 5 V ;

Writing mode (code 51 to 255) : V_{pvs} = 5.1 to 25.5 V

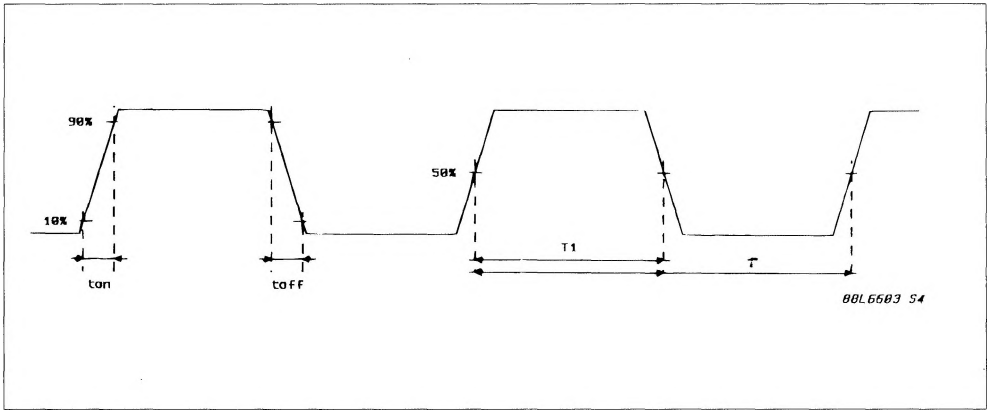
In this case, the voltage drop between output of converter DC/DC (PVSI) and V_{pvs} is constant and is tipically to 3 V.

Figure 1 : V_{CS} and V_{PVS} Delay Times Versus V_{CS} Enable.



C_{tot} load = 30 pF.

Figure 2 : Clock Output Waveform.



C_{tot} load = 30 pF.

Figure 3 : Input for External Clock.

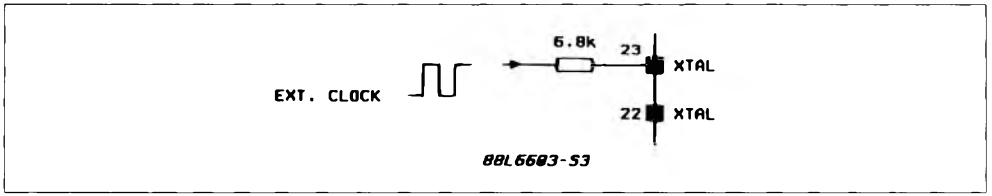


Figure 4 : Application Circuit.