1 K × 8 CMOS Dual Port RAM 3.3 Volt

Introduction

The L67130/67140 are very low power CMOS dual port static RAMs organized as 1024 × 8. They are designed to be used as a stand-alone 8 bits dual port RAM or as a combination MASTER/SLAVE dual port for 16 bits or more width systems. The MHS MASTER/SLAVE dual port approach in memory system applications results in full speed, error free operation without the need for additional discrete logic.

Master and slave devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in the memory. An automatic power down feature controlled by $\overline{CS}$ permits the onchip circuitry of each port in order to enter a very low stand by power mode.

Using an array of eight transistors (8T) memory cell and fabricated with the state of the art 1.0 µm lithography named SCMOS, the M67130/140 combine an extremely low standby supply current (typ = 1.0 µA) with a fast access time at 45 ns over the full temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5 µW.

For military/space applications that demand superior levels of performance and reliability the L67130/67140 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

Features

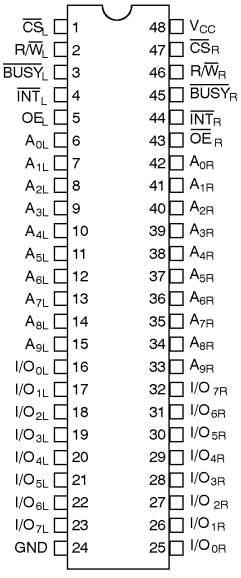
- Single 3.3 V ± 0.3 volt power supply
- Fast access time
  45 ns(*) to 70 ns
- 67130L/67140L low power
  67130V/67140V very low power
- Expandable data bus to 16 bits or more using master/slave devices when using more than one device.
- On chip arbitration logic
- $\overline{BUSY}$ output flag on master
- $\overline{BUSY}$ input flag on slave
- $\overline{INT}$ flag for port to port communication
- Fully asynchronous operation from either port
- Battery backup operation : 2 V data retention

(*) Preliminary

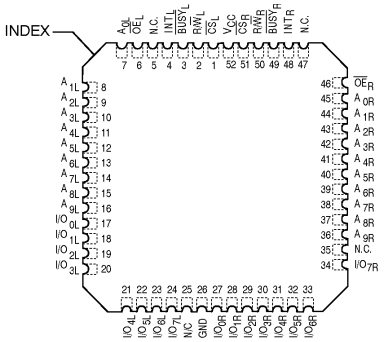
Interface

Pin Configuration

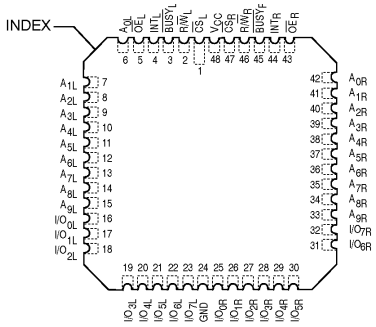
48 PIN DIL (top view), ceramic, plastic 600 mils



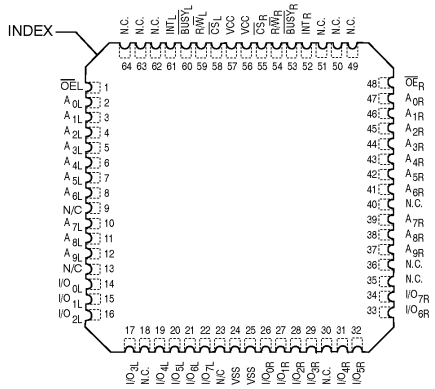
52 PIN PLCC (top view)



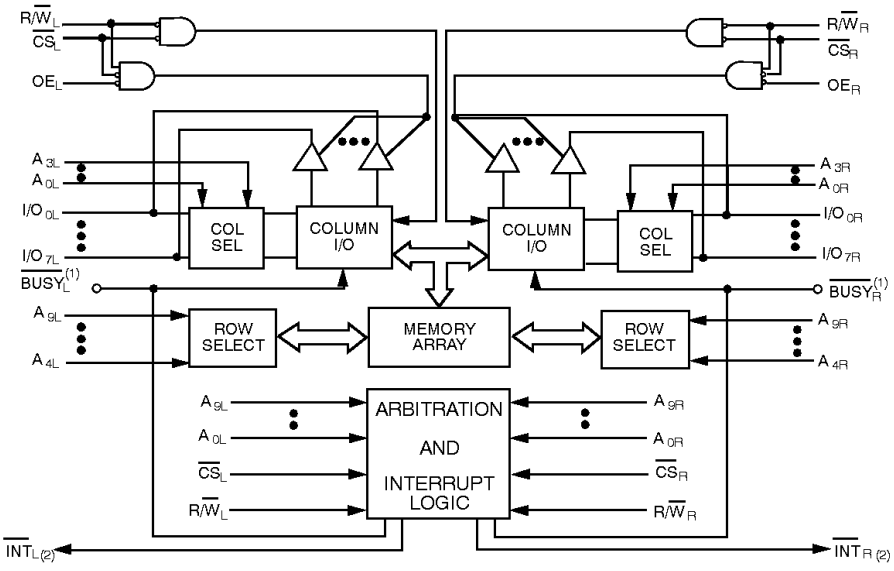
48 PIN PLCC (top view)



64 PIN VQFP (top view)



Block Diagram



Notes :
1. L 67130 (MASTER) : $\overline{BUSY}$ is open drain output and requires pullup resistor
   L 67140 (SLAVE) : $\overline{BUSY}$ in input
2. Open drain output requires pull-up resistor.

Pin Names

LEFT PORT	RIGHT PORT	NAMES
$\overline{CS}_L$	$\overline{CS}_R$	Chip select
R/$\overline{W}_L$	R/$\overline{W}_R$	Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-9L}	A_{0R-9R}	Address
I/O_{0L-7L}	I/O_{0R-7R}	Data Input/Output
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
VCC		Power
GND		Ground

Functional Description

The L 67130/L 67140 has two ports with separate control, address and I/0 pins that permit independent read/write access to any memory location. These devices have an automatic power-down feature controlled by $\overline{CS}$. $\overline{CS}$ controls on-chip power-down circuitry which causes the port concerned to go into stand-by mode when not selected ($\overline{CS}$ high). When a port is selected access to the full memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In read mode, the port's $\overline{OE}$ turns the Output drivers on when set LOW. Non-conflicting READ/WRITE conditions are illustrated in table 1.

Interrupt Logic

The interrupt flag ($\overline{INT}$) allows communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Similarly, the right port interrupt flag (INT_R) is set when the left port writes to memory location 3FF (hex), and the right port must read memory location 3FF in order to clear the interrupt flag (INT_R). The 8 bit message at 3FE or 3FF is user-defined. If the interrupt function is not used, address locations 3FE and 3FF are not reserved for mail boxes but become part of the RAM. See table 3 for the interrupt function.

Arbitration Logic

The arbitration logic will resolve an address match or a chip select match down to a minimum of 5 ns and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the inhibited port.

The $\overline{BUSY}$ flags are required when both ports attempt to access the same location simultaneously.Should this conflict arise, on-chip arbitration logic will determine which port has access and set the $\overline{BUSY}$ flag for the inhibited port. $\overline{BUSY}$ is set at speeds that allow the processor to hold the operation with its associated address and data. It should be noted that the operation is invalid for the port for which $\overline{BUSY}$ is set LOW. The inhibited port will be given access when $\overline{BUSY}$ goes inactive.

A conflict will occur when both left and right ports are active and the two addresses coincide. The on-chip arbitration determines access in these circumstances. Two modes of arbitration are provided : (1) if the addresses match and are valid before $\overline{CS}$ on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for access ; or (2) if the $\overline{CS}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to table 2). The inhibited port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation in both arbitration modes.

Data Bus Width Expansion

Master/Slave Description

Expanding the data bus width to 16 or more bits in a dual-port RAM system means that several chips may be active simultaneously. If every chip has a hardware arbitrator, and the addresses for each chip arrive at the same time one chip may activate its L $\overline{BUSY}$ signal while another activates its R $\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To overcome this "Busy Lock-Out" problem, MHS has developed a MASTER/SLAVE system which uses a single hardware arbitrator located on the MASTER. The SLAVE has $\overline{BUSY}$ inputs which allow direct interface to the MASTER with no external components, giving a speed advantage over other systems.

When dual-port RAMs are expanded in width, the SLAVE RAMs must be prevented from writing until the $\overline{BUSY}$ input has been settled. Otherwise, the SLAVE chip may begin a write cycle during a conflict situation. On the opposite, the write pulse must extend a hold time beyond $\overline{BUSY}$ to ensure that a write cycle occurs once the conflict is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE must be inhibited by the MASTER's maximum arbitration time. If a conflict then occurs, the write to the SLAVE will be inhibited because of the MASTER's $\overline{BUSY}$ signal.

Truth Table

Table 1 : Non Contention Read/Write Control(4)

LEFT OR RIGHT PORT(1)				FUNCTION
R/$\overline{W}$	$\overline{CS}$	$\overline{OE}$	D0–7	
X	H	X	Z	Port Disabled and in Power Down Mode. ICCSB or ICCSB1
L	L	X	$DATA_{IN}$	Data on Port Written into memory(2)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

Notes : 1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE.

Table 2 : Arbitration[5]

LEFT PORT		RIGHT PORT		FLAGS		FUNCTION
$\overline{CS}_L$	$A_{0L} - A_{9L}$	$\overline{CS}_R$	$A_{0L} - A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{9R}$	L	$\neq A_{0L} - A_{9L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L–Port Wins
L	RV5L	L	RV5L	L	H	R–Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CS}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CS}$						
LL5R	$= A_{0R} - A_{9R}$	LL5R	$= A_{0L} - A_{9L}$	H	L	L–Port Wins
RL5L	$= A_{0R} - A_{9R}$	RL5L	$= A_{0L} - A_{9L}$	L	H	R–Port Wins
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	L	H	Arbitration Resolved

Notes : 5. $\overline{INT}$ Flags Don't Care.
6. X = DON'T CARE, L = LOW, H = HIGH.
LV5R = Left Address Valid ≥ 5 ns before right address.
RV5L = Right address Valid ≥ 5 ns before left address.
Same = Left and Right Addresses match within 5 ns of each other.
LL5R = Left $\overline{CS}$ = LOW ≥ 5 ns before Right $\overline{CS}$.
RL5L = Right $\overline{CS}$ = LOW ≥ 5 ns before left $\overline{CS}$.
LW5R = Left and Right $\overline{CS}$ = LOW within 5 ns of each other.

Table 3 : Interrupt Flag [7, 10]

LEFT PORT					RIGHT PORT					FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	A_{OL}–A_{9L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	A_{OR}–A_{9R}	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L[8]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H[9]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[9]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H[8]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

Notes : 7. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
8. If $\overline{BUSY}_L$ = L, then NC.
9. If $\overline{BUSY}_R$ = L, then NC.
10. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage (VCC–GND) : . . . . . –0.3 V to 7.0 V
Input or output voltage applied : . . . (GND –0.3 V) to (VCC + 0.3 V)
Storage temperature : . . . . . –65°C to + 150°C

**** Notice***

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extented periods may affect reliability.

OPERATING RANGE	OPERATING SUPPLY VOLTAGE	OPERATING TEMPERATURE
Military	V_{CC} = 3.3 V ± 0.3 V	– 55 °C to + 125 °C
Automotive	V_{CC} = 3.3 V ± 0.3 V	– 40 °C to + 125 °C
Industrial	V_{CC} = 3.3 V ± 0.3 V	– 40 °C to + 85 °C
Commercial	V_{CC} = 3.3 V ± 0.3 V	0 °C to + 70 °C

DC Parameters

Parameter	Description	Version	L 67130/ 140–45		L 67130/ 140–55		L 67130/ 140–70		Unit	Value
			COM	IND MIL AUTO	COM	IND MIL AUTO	COM	IND MIL AUTO		
			Preliminary							
I_{CCSB} (11)	Standby supply current (Both ports TTL level inputs)	V L	1 5	1 10	1 5	1 10	1 5	1 10	mA mA	Max Max
I_{CCSB1} (12)	Standby supply current (Both ports CMOS level inputs)	V L	10 100	20 200	10 100	20 200	10 100	20 200	µA µA	Max Max
I_{CCOP} (13)	Operating supply current (Both ports active)	V L	80 80	90 100	70 70	80 90	60 60	70 80	mA mA	Max Max
$I_{CCOP\ 1}$ (14)	Operating supply current (One port active – One port standby)	V L	50 60	55 65	40 50	45 55	35 45	40 50	mA mA	Max Max

Notes : 11. $\overline{CS}_L = \overline{CS}_R \geq 2.2$ V.
12. $\overline{CS}_L = \overline{CS}_R \geq$ VXX – 0.2 V.
13. Both ports active – Maximum frequency – Outputs open – $\overline{OE}$ = VIH.
14. One port active (f = MAX) – Output open – One port stand-by TTL or CMOS Level inputs – $\overline{CS}_L = \overline{CS}_R \geq 2.2$ V.

PARAMETER	DESCRIPTION	L 67130–45/55/70 L 67140–45/55/70	UNIT	VALUE
$II/O_{(15)}$	Input/Output leakage current	± 10	µA	Max
$VIL_{(16)}$	Input low voltage	0.7	V	Max
$VIH_{(16)}$	Input high voltage	1.8	V	Min
$VOL_{(17)}$	Output low voltage (I/O_0–I/O_7)	0.5	V	Max
VOL	Open drain output low voltage (BUSY, INT) I_{OL} = 16 mA	0.5	V	Max
$VOH_{(17)}$	Output high voltage	1.5	V	Min
$C\ IN_{(21)}$	Input capacitance	5	pF	Max
$C\ OUT_{(21)}$	Output capacitance	7	pF	Max

Notes : 15. V_{CC} = 5.5 V, Vin = Gnd to V_{CC}, $\overline{CS}$ = VIH, Vout = 0 to V_{CC}.
16. VIH max = V_{CC} + 0.3 V, VIL min – 0.3 V or –1 V pulse width 50 ns.
17. V_{CC} min, IOL = 4 mA, IOH = –4 mA.

Data-Retention Mode

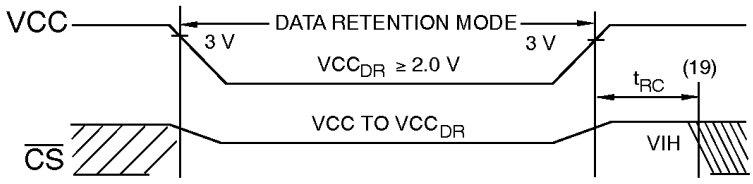
MHS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1 – Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to VCC_{DR}.

2 – $\overline{CS}$ must be kept between V_{CC} – 0.2 V and 70 % of Vcc during the power up and power down transitions.

3 – The RAM can begin operation > tRC after Vcc reaches the minimum operating voltage (3 volts).

Timing



PARAMETER	TEST CONDITIONS (18)	MAX		UNIT
		COM	MIL IND AUTO	
ICC_{DR1}	@ VCC_{DR} = 2 V	10	20	µA

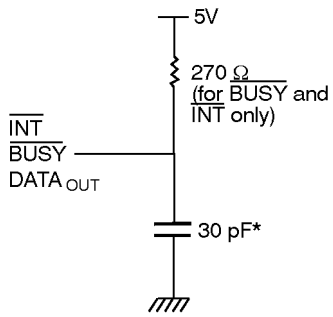
Notes : 18. $\overline{CS}$ = Vcc, Vin = Gnd to Vcc.
19. t_{RC} = Read cycle time.

AC Test Conditions

Input Pulse Levels : GND to 3.0 V
Input Rise/Fall Times : 5 ns
Input Timing Reference Levels : 1.5 V

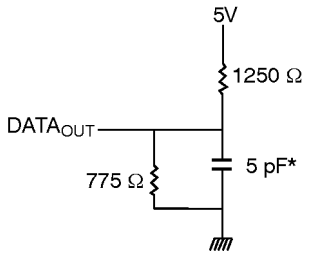
Output Reference Levels : 1.5 V
Output Load : see figures 1, 2

Figure 1. Output Load.



* Including scope and jig

Figure 2. Output load.
(For t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

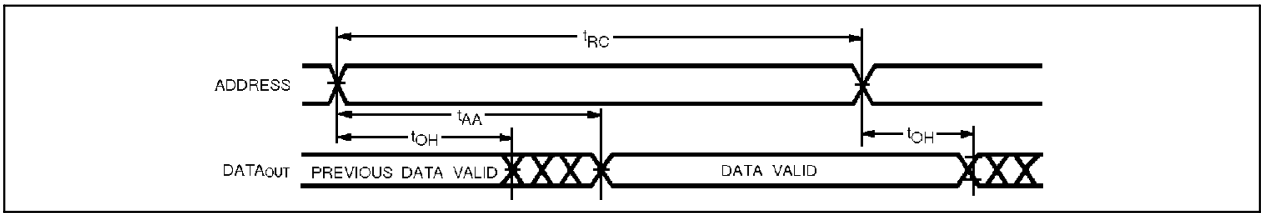


AC Parameters

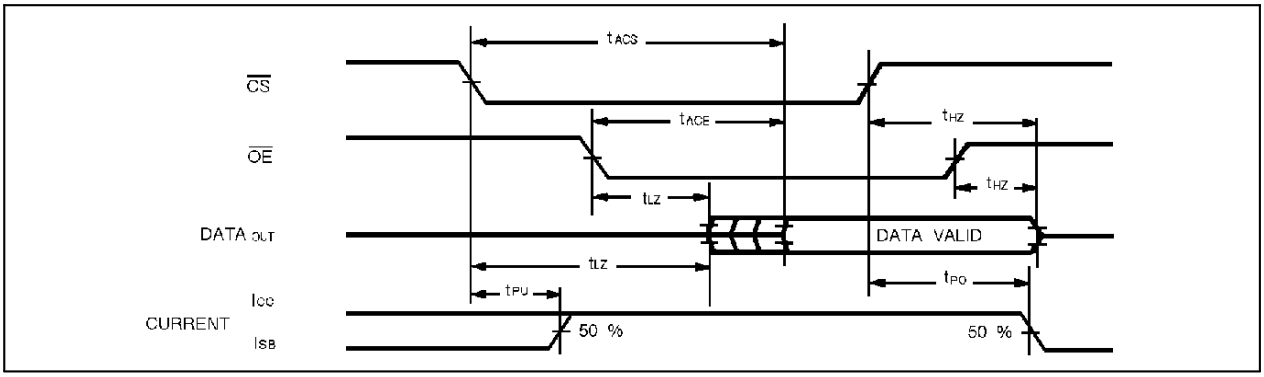
READ CYCLE		PARAMETER	L67130–45 L67140–45		L67130–55 L67140–55		L67130–70 L67140–70		UNIT
SYMBOL (23)	SYMBOL (24)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
			PRELIMINARY						
TAVAVR	t_{RC}	Read cycle time	45	–	55	–	70	–	ns
TAVQV	t_{AA}	Address access time	–	45	–	55	–	70	ns
TELQV	t_{ACS}	Chip Select access time (22)	–	45	–	55	–	70	ns
TGLQV	t_{AOE}	Output enable access time	–	30	–	35	–	40	ns
TAVQX	t_{OH}	Output hold from address change	0	–	0	–	0	–	ns
TELQZ	t_{LZ}	Output low Z time (20, 21)	5	–	5	–	5	–	ns
TEHQZ	t_{HZ}	Output high Z time (20, 21)	–	20	–	30	–	35	ns
TPU	t_{PU}	Chip Select to power up time (21)	0	–	0	–	0	–	ns
TPD	t_{PD}	Chip disable to power down time (21)	–	50	–	50	–	50	ns

Notes :
20. Transition is measured ± 500 mV from low or high impedance voltage with load (figures 1 and 2).
21. This parameter is guaranteed but not tested.
22. To access RAM $\overline{CS}$ = VIL.
23. STD symbol.
24. ALT symbol.

Timing Waveform of Read Cycle nº 1, Either Side (25, 26, 28)



Timing Waveform of Read Cycle nº 2, Either Side (25, 27, 29)



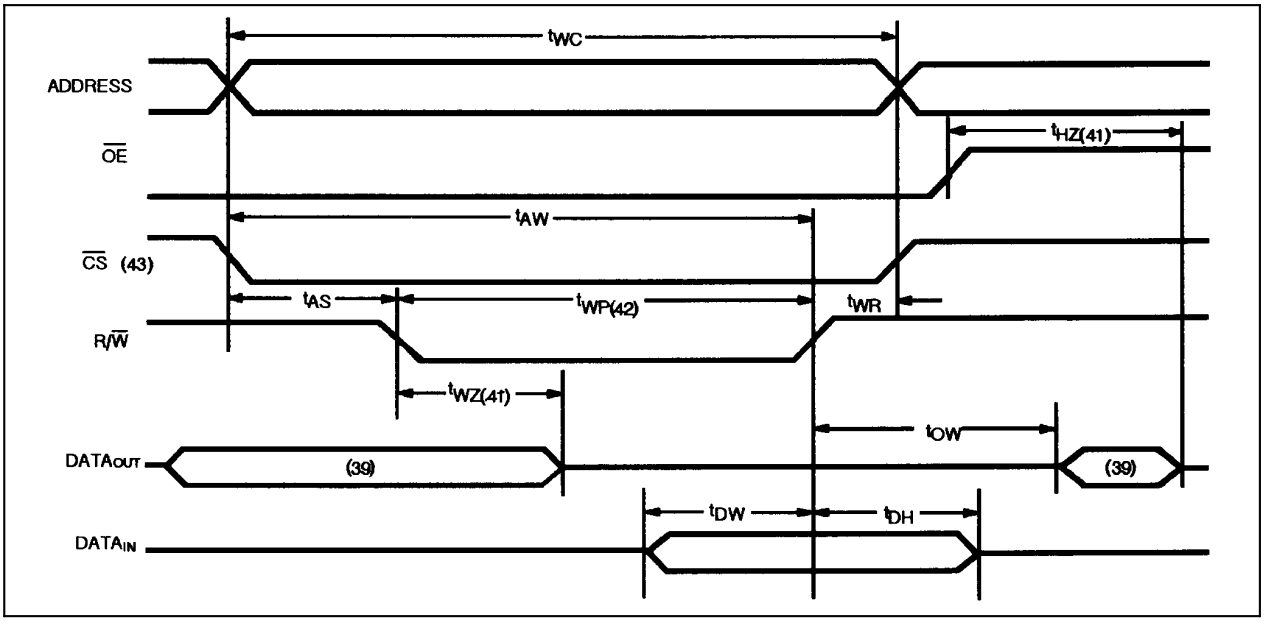
Notes :
25. R/W is high for read cycles.
26. Device is continuously enabled, $\overline{CS}$ = VIL.
27. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
28. $\overline{OE}$ = VIL.
29. To access RAM, $\overline{CS}$ = VIL.

AC Parameters

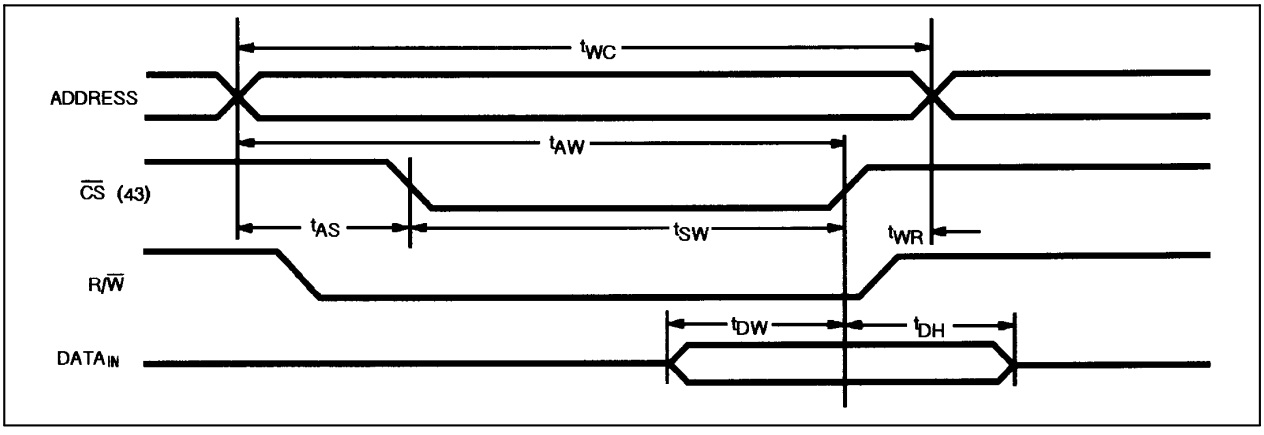
WRITE CYCLE		PARAMETER	L67130–45 L67140–45		L67130–55 L67140–55		L67130–70 L67140–70		UNIT
SYMBOL (34)	SYMBOL (35)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
			PRELIMINARY						
TAVAVW	t_{WC}	Write cycle time	45	–	55	–	70	–	ns
TELWH	t_{SW}	Chip select to end of write (32)	35	–	40	–	45	–	ns
TAVWH	t_{AW}	Address valid to end of write	35	–	40	–	45	–	ns
TAVWL	t_{AS}	Address Set–up Time	0	–	0	–	0	–	ns
TWLWH	t_{WP}	Write Pulse Width	35	–	40	–	45	–	ns
TWHAX	t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
TDVWH	t_{DW}	Data Valid to end of write	25	–	25	–	30	–	ns
TGHQZ	t_{HZ}	Output high Z time (30, 31)	–	20	–	30	–	40	ns
TWHDX	t_{DH}	Data hold time (33)	0	–	0	–	0	–	ns
TWLQZ	t_{WZ}	Write enable to output in high Z (30, 31)	–	20	–	30	–	40	ns
TWHQX	t_{OW}	Output active from end of write (30, 31, 33)	0	–	0	–	0	–	ns

Notes :
30. Transition is measured ± 500 mV from low or high impedance voltage with load (figures 1 and 2).
31. This parameter is guaranteed but not tested.
32. To access RAM $\overline{CS}$ = VIL.
    This condition must be valid for entire t_{SW} time.
33. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions.
    Although t_{DH} and t_{OW} values vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
34. STD symbol.
35. ALT symbol.

Timing Waveform of Write Cycle nº 1, R/$\overline{W}$ Controlled Timing (36, 37, 38, 42)



Timing Waveform of Write Cycle nº 2, $\overline{CS}$ Controlled Timing (36, 37, 38, 40)



Notes :

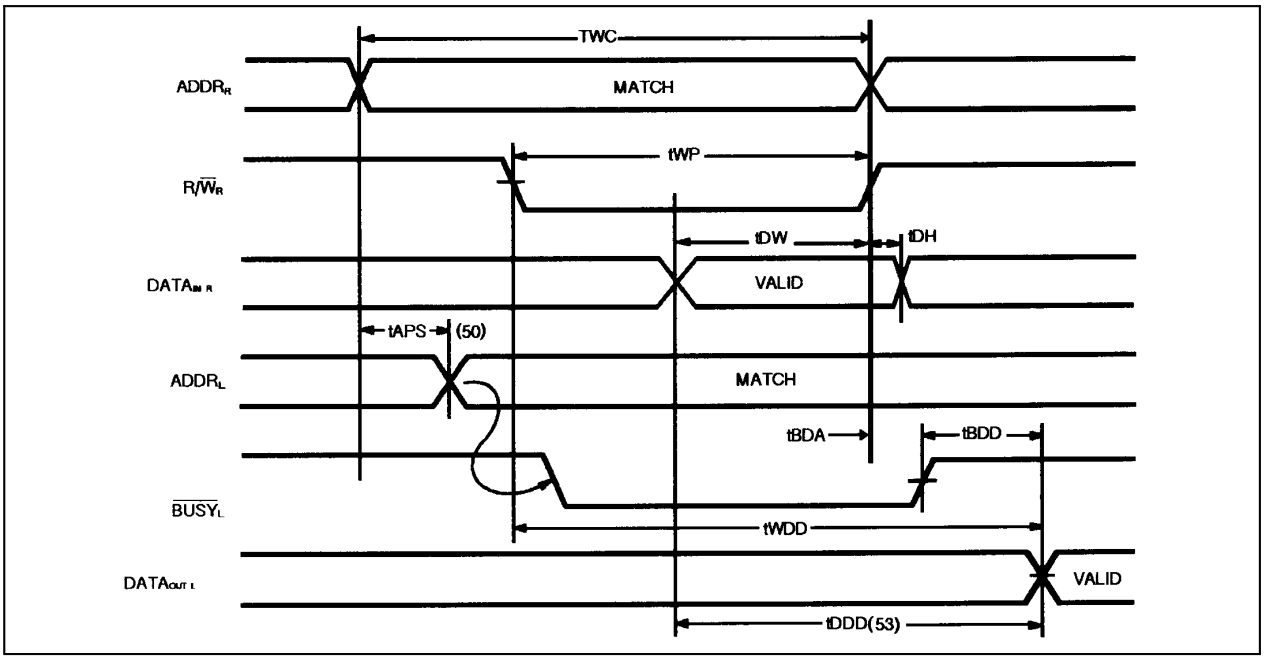
36. R/W must be high during all address transitions.
37. A write occurs during the overlap (t_{SW} or t_{WP}) of a low $\overline{CS}$ and a low R/$\overline{W}$.
38. t_{WR} is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
39. During this period, the I/O pins are in the output state, and input signals must not be applied.
40. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
41. Transition is measured ± 500 mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100 % tested.
42. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
43. To access RAM, $\overline{CS}$ = VIL.

AC Parameters

SYMBOL	PARAMETER	L67130–45 L67140–45		L67130–55 L67140–55		L67130–70 L67140–70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
BUSY TIMING (For L 67130 only)								
t_{BAA}	$\overline{BUSY}$ Access time to address	–	35	–	45	–	50	ns
t_{BDA}	$\overline{BUSY}$ Disable time to address	–	35	–	40	–	40	ns
t_{BAC}	$\overline{BUSY}$ Access time to Chip Select	–	30	–	35	–	50	ns
t_{BDC}	$\overline{BUSY}$ Disable time to Chip Select	–	25	–	30	–	40	ns
t_{WDD}	Write Pulse to data delay (44)	–	70	–	80	–	90	ns
t_{DDD}	Write data valid to read data delay (44)	–	45	–	55	–	70	ns
t_{APS}	Arbitration priority set–up time (45)	5	–	5	–	5	–	ns
t_{BDD}	$\overline{BUSY}$ disable to valid data	–	Note 46	–	Note 46	–	Note 46	ns
BUSY TIMING (For L 67140 only)								
t_{WB}	Write to $\overline{BUSY}$ input (47)	0	–	0	–	0	–	ns
t_{WH}	Write hold after $\overline{BUSY}$ (48)	30	–	30	–	30	–	ns
t_{WDD}	Write pulse to data delay (49)	–	70	–	80	–	90	ns
t_{DDD}	Write data valid to read data delay (49)	–	45	–	55	–	70	ns

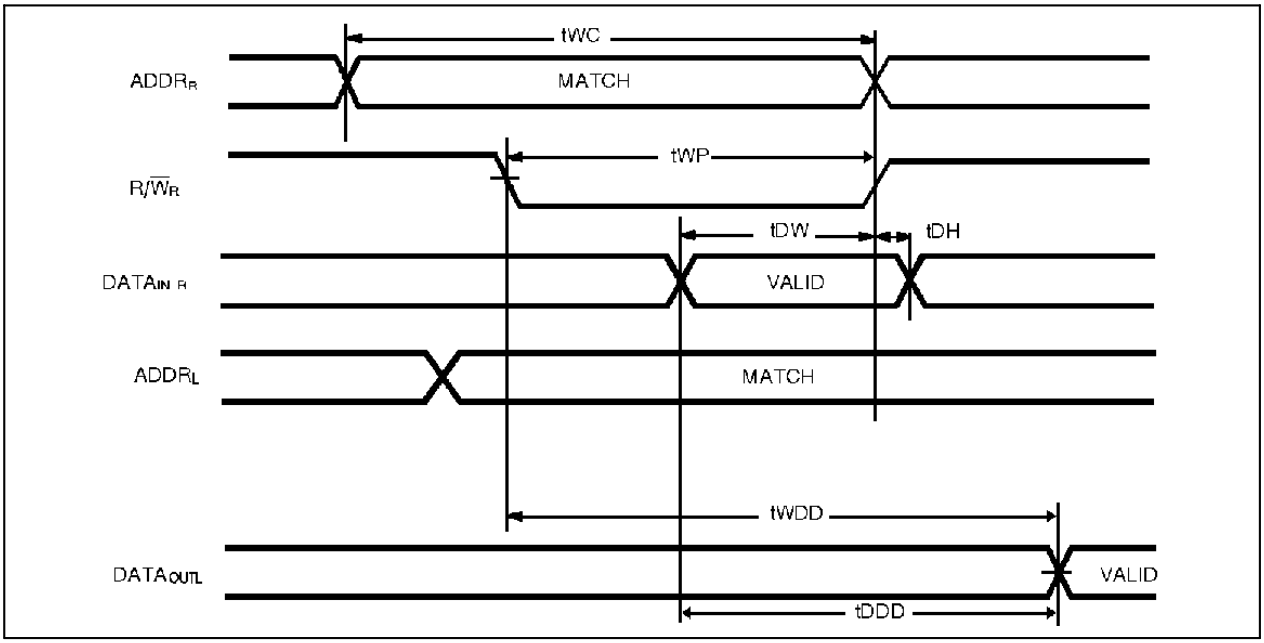
Notes :
44. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveform of Read with $\overline{BUSY}$ (For L67130 only)”.
45. To ensure that the earlier of the two ports wins.
46. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
47. To ensure that the write cycle is inhibited during contention.
48. To ensure that a write cycle is completed after contention.
49. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveforms of Read with Port to port delay (For L67140 only)”.

Timing Waveform of Read with $\overline{BUSY}$ (50, 51, 52) (For L 67130)



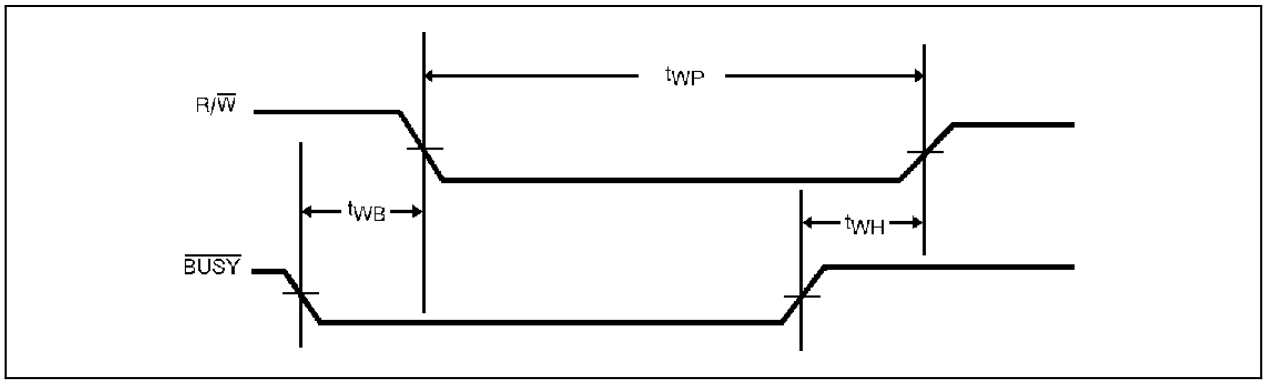
Notes :
50. To ensure that the earlier of the two port wins.
51. Write cycle parameters should be adhered to, to ensure proper writing.
52. Device is continuously enabled for both ports.
53. $\overline{OE}$ at L for the reading port.

Timing Waveform of Write with Port-to-port (54, 55, 56) (For L 67140 only)

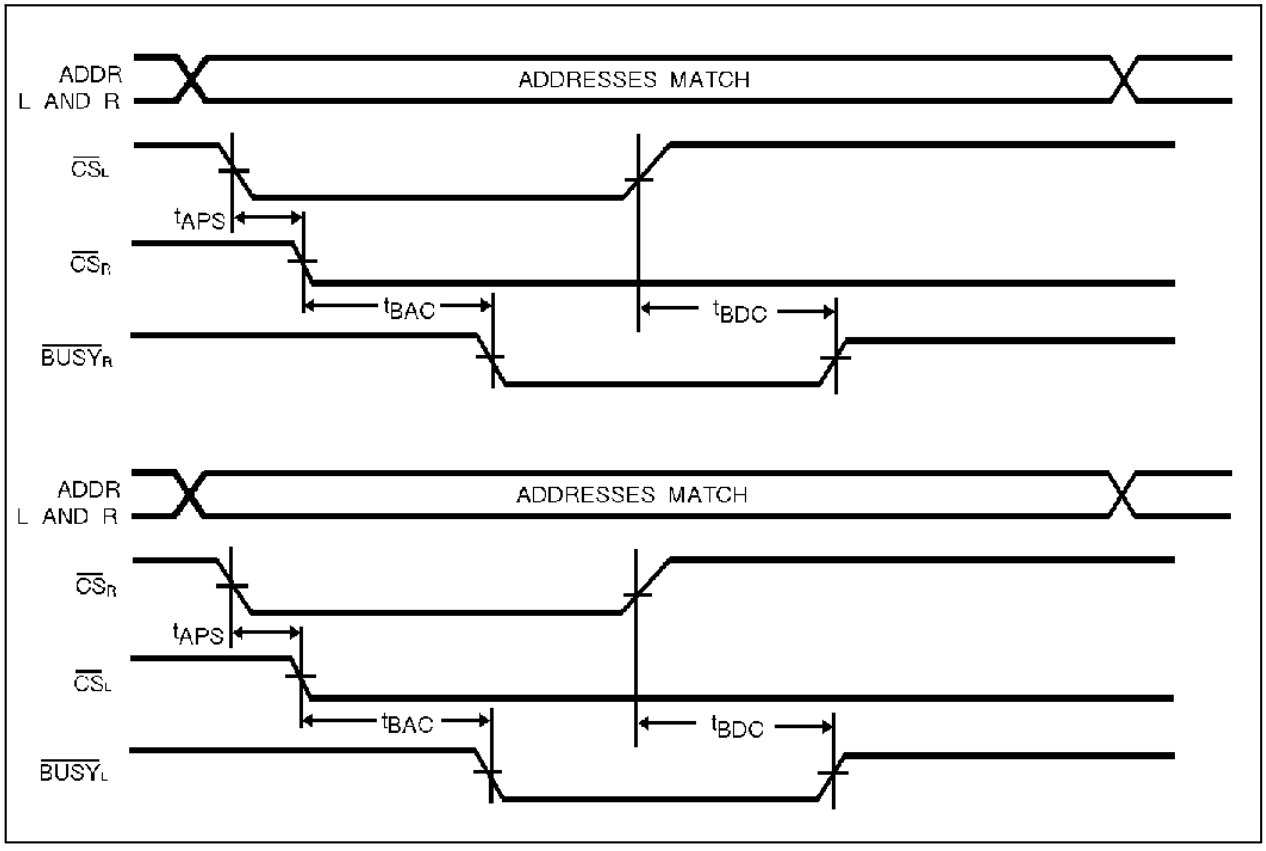


Notes :
54. Assume $\overline{BUSY}$ = H for the writing port, and $\overline{OE}$ = L for the reading port.
55. Write cycle parameters should be adhered to, to ensure proper writing.
56. Device is continuously enabled for both ports.

Timing Waveform of Write with $\overline{\text{BUSY}}$ (For L 67140)

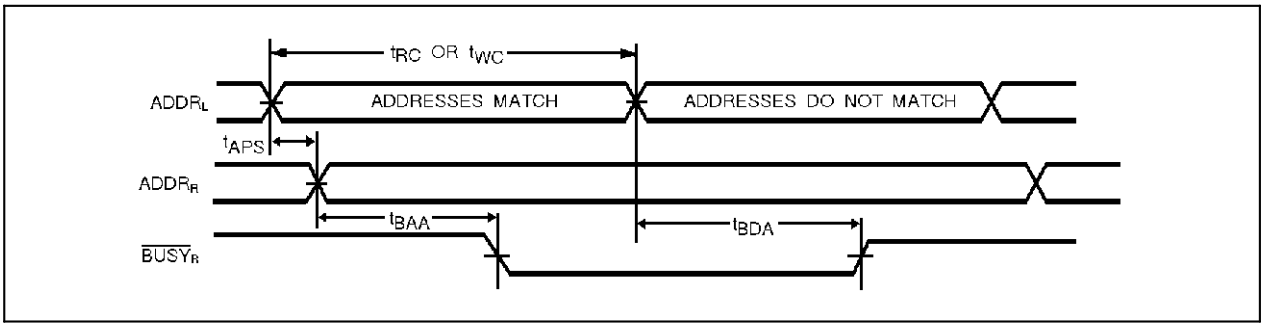


Timing Waveform of Contention Cycle nº 1, $\overline{\text{CS}}$ Arbitration (For L 67130 only)

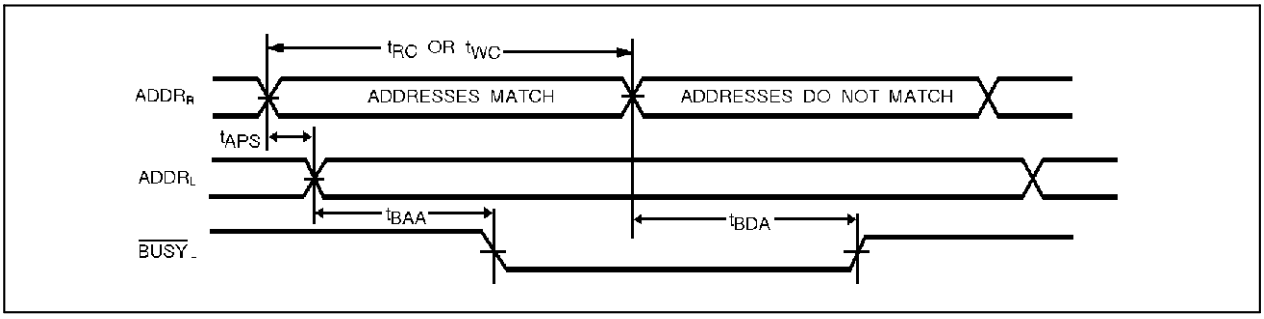


Timing Waveform of Contention Cycle nº 2, Address Valid Abritration (For L 67130 only) (57)

Left Address Valid First :

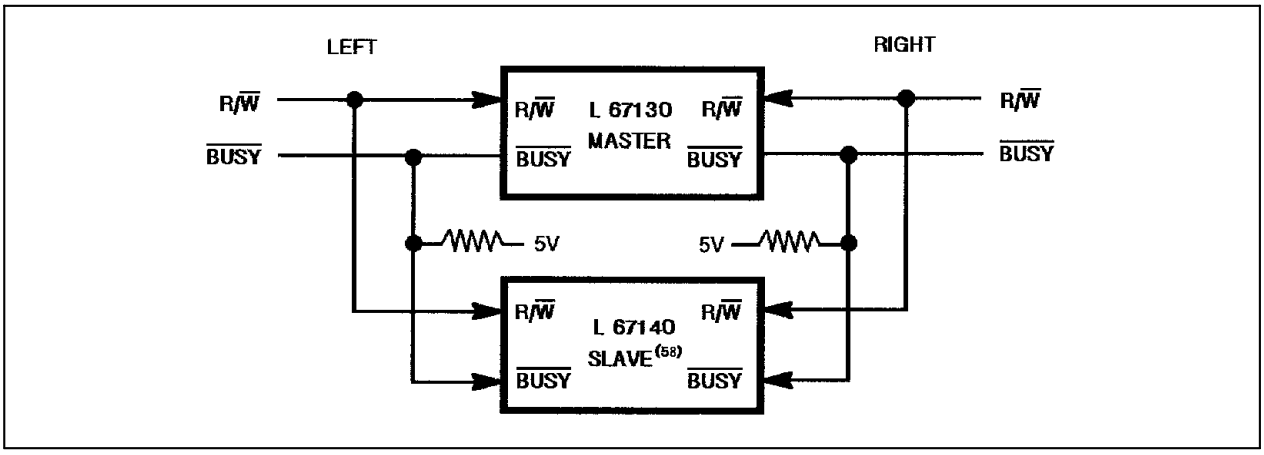


Right Address Valid First :



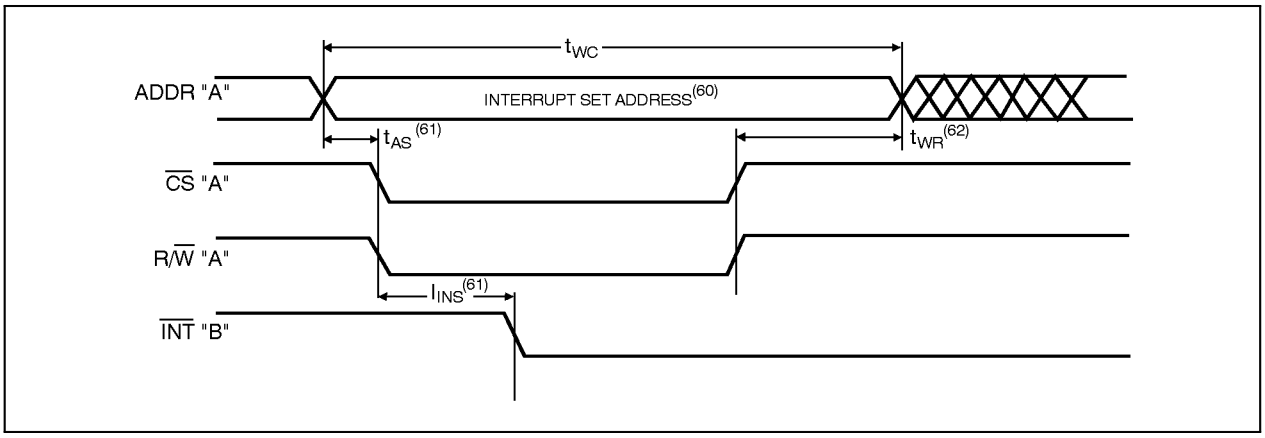
Note : 57. $\overline{CS}_L = \overline{CS}_R = V_{IL}$

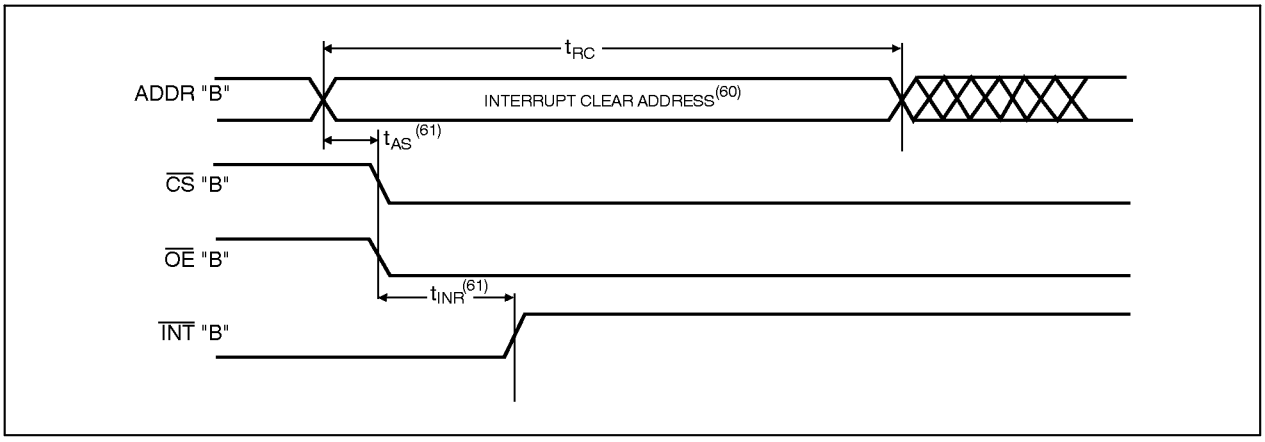
16 Bit Master/Slave Dual-port Memory Systems



Note : 58. No arbitration in L 67140 (SLAVE). $\overline{BUSY}$ IN inhibits write in L 67140 (SLAVE).

Waveform of Interrupt Timing (59)





Notes : 59. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from “A”.
60. See interrupt truth table.
61. Timing depends on which enable signal is asserted last.
52. Timing depends on which enable signal is de-asserted first.

AC Electrical Characteristics over the Full Operating Temperature and Supply Voltage Range

INTERRUPT TIMING	PARAMETER	L 67130/140–45		L 6 7130/140–55		L 6 7130/140–70		UNIT
SYMBOL		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{AS}	Address set–up time	0	—	0	—	0	—	ns
t_{WR}	Write recovery time	0	—	0	—	0	—	ns
t_{INS}	Interrupt set time	—	40	—	45	—	60	ns
t_{INR}	Interrupt reset time	—	40	—	45	—	60	ns

Ordering Information

TEMPERATURE RANGE PACKAGE DEVICE SPEED FLOW

C **L** **S3** — **67130V** — **55**

C = Commercial 0° to +70°C
I = Industrial –40° to +85°C
A = Automotive –40° to +125°C
M = Military –55° to +125°C
S = Space –55° to +125°C

3.3 V ± 0.3 Volt

1K = 48 pin DIL ceramic 600 mils
CK = 48 pin DIL side-brazed 600 mils
4K = 48 pin LCC
S3 = 52 pin PLCC
3K = 48 pin DIL plastic 600 mils
RD = 64 pin VQFP

45 ns
55 ns
70 ns

67130 = 8K (1K × 8) Master
67140 = 8K (1K × 8) Slave
L = Low power
V = Very low power
EL = Low power and rad tolerant
EV = Very low power and rad tolerant

blank = MHS standards
/883 = MIL-STD 883 Class B or S
P883 = MIL-STD 883 + PIND TEST
SB/SC = SCC9000 level B/C
SHXXX = Special customer request
FHXXX = Flight models (space)
MHXXX = Mechanical parts (space)
LHXXX = Life test parts (space)