Ordering number : EN4371

Monolithic Linear IC

SANYO | No. 4371 | **LA5607**

BS/CS Tuner Regulator with Reset, On/Off Function

Overview

The LA5607 is a low-dropout voltage regulator IC for BS/CS tuner applications, equipped with four regulators capable of ON/OFF control plus reset function.

Applications

- BS/CS tuner power supply system.
- Audio Video (AV) equipments with BS/CS recievers.
- Compact electronic equipment.

Functions

- Four low-dropout regulators (15.7 V/300 mA, 12 V/150 mA, 9 V/100 mA and 5 V/500 mA).
- Output on/off control ("L" active).
- On-chip protective circuitry (current limitter, thermal shut down).
- On-chip microcontroller reset signal generation circuit.

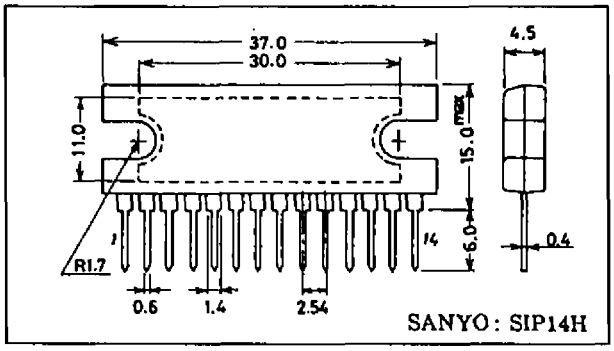
Features

- Supports compact set design while incorporating four regulators needed by BS/CS tuners.
- Flexible system design by independent on/off control of V_O1, V_O4, as well as V_O2 and V_O3 pair.
- Reduces internal loss by employment of low-dropout voltage regulators.
- Adapting three input pins contributes power dissipation reduction and heat sink design.
- On-chip reset signal generation circuit is most suitable for tuners using microcontrollers.

Package Dimensions

unit : mm

3023A-SIP14H



Specifications

Maximum Ratings at Ta = 25°C

				unit
Maximum input voltage	V_{IN} max	$V_{IN}1 \geq V_{IN}2 \geq V_{IN}3$	35	V
Enable pin voltage	V_{EN} max	EN1, EN2, EN3	V_{IN} max	V
Allowable power dissipation	Pd max	With infinite heat sink	15	W
		With no heat sink	4.3	W
Operating temperature	Topr		−20 to +80	°C
Storage temperature	Tstg		−55 to +150	°C

Operating Conditions at Ta = 25°C

				unit
Output current 1	I_O1	Regulator 1	5 to 300	mA
Output current 2	I_O2	Ragulator 2	1 to 150	mA
Output current 3	I_O3	Regulator 3	1 to 100	mA
Output current 4	I_O4	Regulator 4	5 to 500	mA
Reset output source current	I_{ORH}	SOURCE	0 to 200	μA
Reset output sink current	I_{ORL}	SINK	0 to 2	mA

Operating Characteristics at Ta = 25°C and the specified Test Circuit

Regulator 1 ($V_{EN}1$ = "L", V_O1: ON, $V_{IN}1$ = 18.7 V and I_O1 = 300 mA)			min	typ	max	unit
Output voltage 1	V_O1		14.9	15.7	16.5	V
Dropout voltage	$V_{DROP1\text{-}1}$			0.3	0.6	V
	$V_{DROP1\text{-}2}$	I_O1 = 150mA		0.15	0.3	V
Line regulation	$\Delta V_{OLN}1$	17.5V≤$V_{IN}1$≤23V		20	100	mV
Load regulation	$\Delta V_{OLD}1$	5mA≤I_O1≤300mA		40	200	mV
Peak output current	$I_{OP}1$		300	540		mA
Output short current	$I_{OSC}1$			150		mA
Output on control voltage	$V_{ENL}1$	V_O1: On			0.4	V
Output off control voltage	$V_{ENH}1$	V_O1: Off	2.0		$V_{IN}1$	V
Output "L"-level voltage	V_O1 OFF				0.2	V
Output noise voltage	$V_{NO}1$	10Hz≤f≤100kHz		110		μVrms
Ripple rejection	Rrej1	f = 120Hz, 18V≤$V_{IN}1$≤23V		50		dB
Regulator 2 ($V_{EN}2$ = "L", V_O2: ON, $V_{IN}2$ = 15.0V, I_O2 = 150mA)						
Output voltage 2	V_O2		11.4	12.0	12.6	V
Dropout voltage	$V_{DROP}2$			0.3	1.0	V
Line regulation	$\Delta V_{OLN}2$	12.6V≤$V_{IN}2$≤23V		20	100	mV
Load regulation	$\Delta V_{OLD}2$	1mA≤I_O2≤150mA		20	70	mV
Peak output current	$I_{OP}2$		150	270		mA
Output short current	$I_{OSC}2$			70		mA
Output on control voltage	$V_{ENL}2$	V_O2: On			0.4	V
Output off control voltage	$V_{ENH}2$	V_O2 :Off	2.0		$V_{IN}2$	V
Output "L"-level voltage	V_O2OFF				0.2	V
Output noise voltage	$V_{NO}2$	10Hz≤f≤100kHz		110		μVrms
Ripple rejection	Rrej2	f = 120Hz, 13V≤$V_{IN}2$≤23V		50		dB
Regulator 3 ($V_{EN}2$ = "L", V_O3: ON, $V_{IN}2$ = 12V, I_O3 = 100mA)						
Output voltage 3	V_O3		8.55	9.0	9.45	V
Dropout voltage	$V_{DROP}3$			0.3	1.0	V
Line regulation	$\Delta V_{OLN}3$	10.45V≤$V_{IN}2$≤23V		20	100	mV
Load regulation	$\Delta V_{OLD}3$	1mA≤I_O3≤100mA		20	50	mV
Peak output current	$I_{OP}3$		100	180		mA
Output short current	$I_{OSC}3$			40		mA
Output on control voltage	$V_{ENL}2$	V_O3: On			0.4	V
Output off control voltage	$V_{ENH}2$	V_O3: Off	2.0		$V_{IN}2$	V
Output "L"-level voltage	V_O3 OFF				0.2	V
Output noise voltage	$V_{NO}3$	10Hz≤f≤100kHz		70		μVrms
Ripple rejection	Rrej3	f = 120Hz, 11V≤$V_{IN}2$≤23V		55		dB
Regulator 4 ($V_{EN}3$ = "L", V_O4: ON, $V_{IN}3$ = 8.0V, I_O4 = 500mA)						
Output voltage 4	V_O4		4.75	5.0	5.25	V
Dropout voltage	$V_{DROP4\text{-}1}$			0.4	1.0	V
	$V_{DROP4\text{-}2}$	I_O4 = 250mA		0.3	0.8	V
Line regulation	$\Delta V_{OLN}4$	6.25V≤$V_{IN}3$≤23V		20	100	mV
Load regulation	$\Delta V_{OLD}4$	5mA≤I_O4≤500mA		30	150	mV
Peak output current	$I_{OP}4$		500	900		mA
Output short current	$I_{OSC}4$			250		mA
Output on control voltage	$V_{ENL}3$	V_O4: On			0.4	V
Output off control voltage	$V_{ENH}3$	V_O4: Off	2.0		$V_{IN}3$	V
Output "L"-level voltage	V_O4 OFF				0.2	V
Output noise voltage	$V_{NO}4$	10Hz≤f≤100kHz		70		μVrms
Ripple rejection	Rrej4	f = 120Hz, 7V≤$V_{IN}3$≤23V		60		dB
Current dissipation 1	I_Q1	I_O1, I_O2, I_O3, I_O4 = 0		11		mA
Current dissipation 2	I_Q2	I_O1 = 300mA, I_O2 = 150mA, I_O3 = 100mA, I_O4 = 500mA		53		mA

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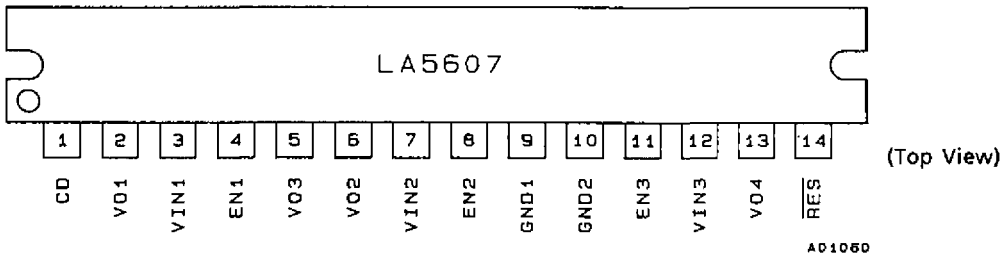
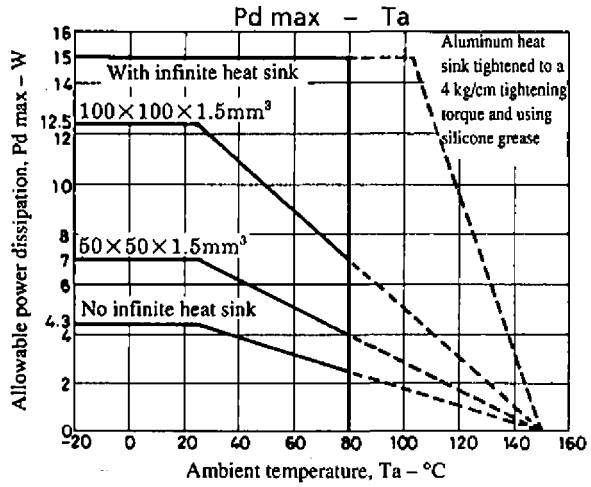
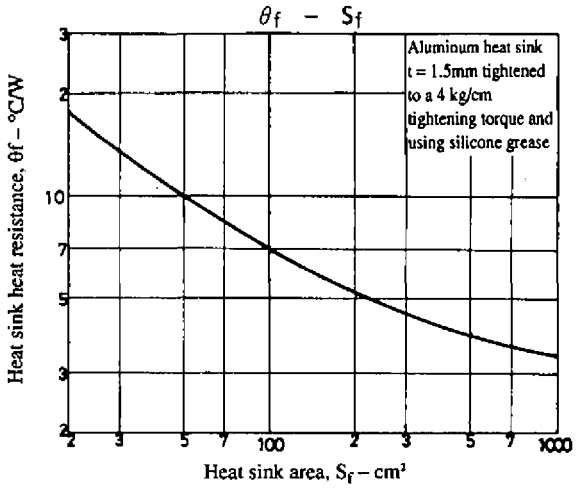
Reset Circuit			min	typ	max	unit
"H"-level reset output voltage	$V_{\overline{ORH}}$	$I_{\overline{ORH}}$ = 200 µA, CD pin open	4.83	4.98	5.13	V
"L"-level reset output voltage	$V_{\overline{ORL}}$	$I_{\overline{ORL}}$ = 2 mA, CD pin shorted to ground (GND)		100	200	mV
Reset threshold voltage	V_{RT}	I_O4 = 5mA	3.95	4.2	4.45	V
Reset hysteresis voltage	Vhys	I_O4 = 5mA	50	100	200	mV
Reset output delay time	td	Cd = 0.1µF	7.5	10	12.5	ms

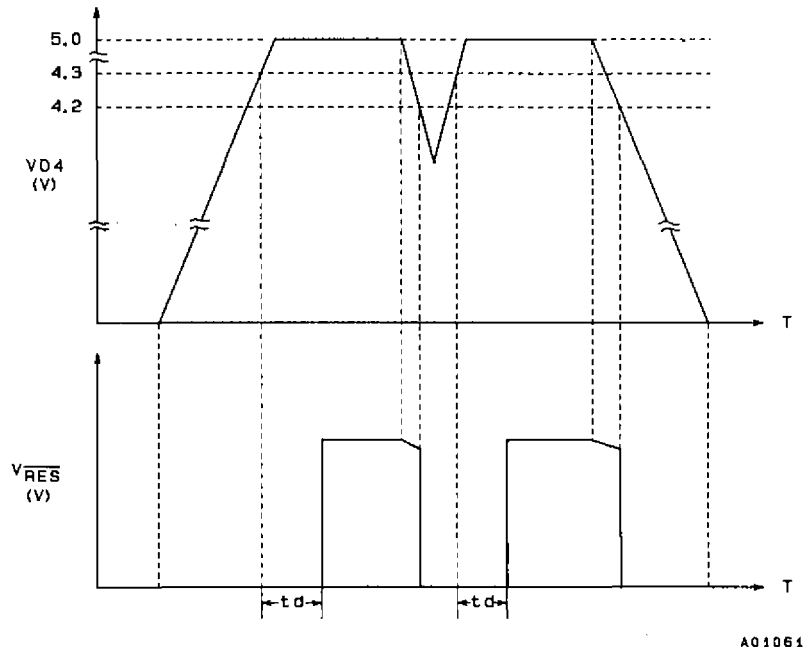
Pin Assignments





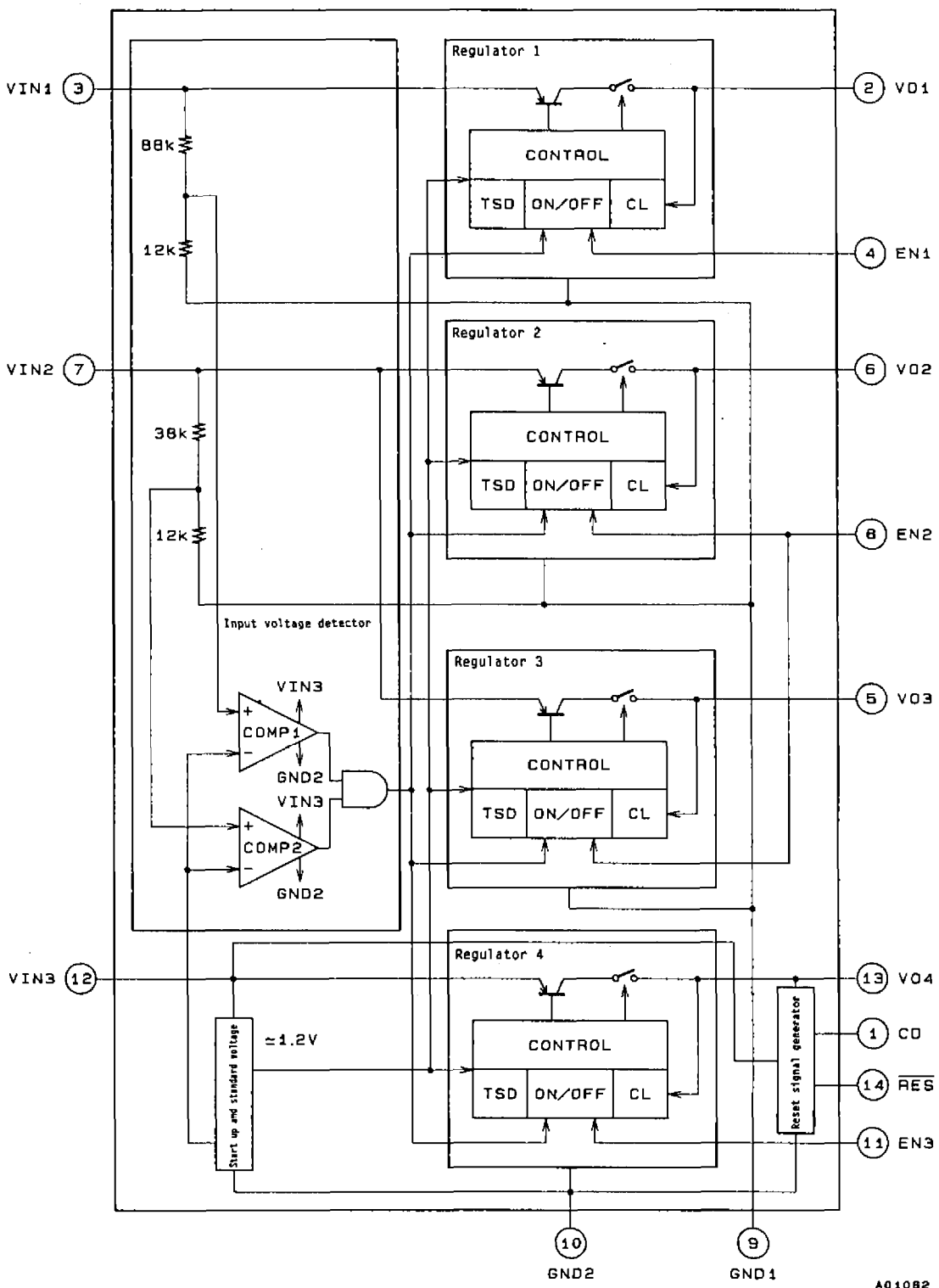


Reset Operation



td = 100 × Cd (µF) [ms]

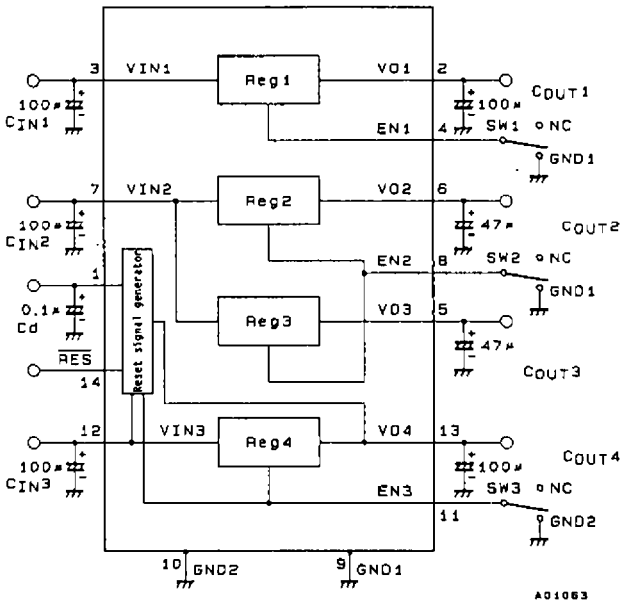
Block Diagram



TSD: Thermal Shut Down Circuit
ON/OFF: Output on/off Control Circuit
CL: Current Limitter Circuit

Unit (resistance: Ω)

Test Circuit



Unit (capacitance: F)

Function Table

The following table indicates conditions for operation with $V_{IN}1 \geq V_{IN}2 \geq V_{IN}3$ ($V_{IN}1 \geq 11$ V, $V_{IN}2 \geq 6$ V and $V_{IN}3 \geq 4$V).

EN1, EN2, EN3	V_O1, V_O2/V_O3, V_O4
H	L
L	H

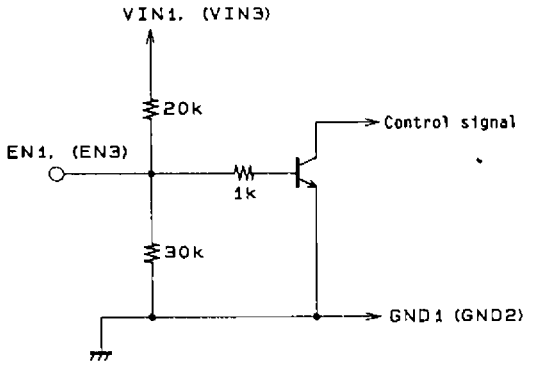
① Within the table H of EN indicates an H level or open and L indicates an L level.

② H of V_O in the table indicates an output on voltage while L indicates an output off voltage.

③ All output voltages corresponding to all EN locations are controlled independently.
($EN1 \rightarrow V_O1$, $EN2 \rightarrow V_O2$ and V_O3, $EN3 \rightarrow V_O4$)

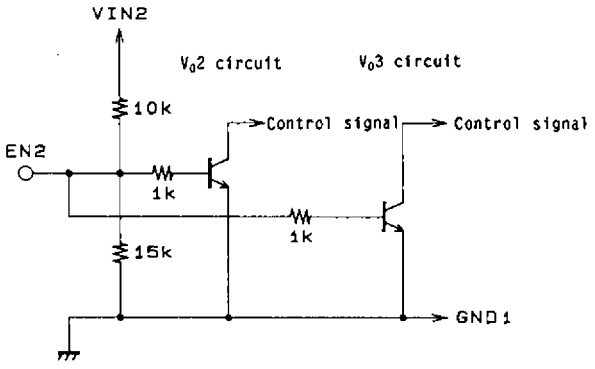
EN (On/Off Control) Input Equivalent Block Diagram

① V_O1 (V_O4)



② V_O2 and V_O3

Unit (resistance: Ω)



Notes for Above Applications

① GND1 and GND2 should be at same electric potential; since these are connected to the substrate of the LA5607, the lowest possible electric potential should be used. (If the electric potential of GND1 and GND2 differ, performance characteristics of the LA5607 can not be guaranteed.)

② Rise and fall times for $V_{IN}1$, $V_{IN}2$ and $V_{IN}3$ should be unified and concerning these pins operating in an open-circuit state or connected to the ground state is forbidden.

③ When $V_{IN}1$ and $V_{IN}2$ are open or lower than the required value, V_O1 to V_O4 are forced off for the IC's protection.

④ Use output capacitors $C_{OUT}1$ and $C_{OUT}4$ rated at 100 μF or more and $C_{OUT}2$ and $C_{OUT}3$ rated at 47 μF or more. To prevent oscillation at low temperature, be sure to use less temperature sensitive capacitors.

⑤ Use delay capacitor Cd which has little change in capacity caused by temperature, such as a tantalum capacitor.

⑥ In order to provide stable operation, $C_{IN}1$ to $C_{IN}3$ and $C_{OUT}1$ to $C_{OUT}4$ should be mounted as close to the LA5607 as possible.