Ordering number: EN 2895A

Monolithic Linear IC

No.2895A

LA5690D, 5690S

Voltage Regulator Driver with Watchdog Timer

The LA5690 is a single-chip voltage regulator for microcomputer system monitor use that performs the functions of 5V output voltage control, watchdog timer, and voltage detector. The LA5690 uses a minimum number of parts to provide the basic functions.

Applications

- Microcomputer system for car equipment, refrigeration/heating equipment, office automation equipment

Functions

- Output voltage 5Vcontrol
- Watchdog timer
- Power-ON reset function
- Positive/negative logic output for reset

Features

- An external PNP transistor can be used to provide a low-saturation voltage regulator.
- CK input with edge detector
- Variable detection voltage
- Reset output with pull-up resistor of 10kΩ

Maximum Ratings at Ta = 25°C

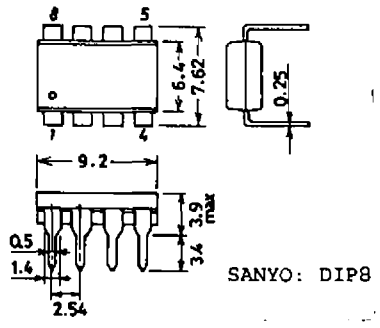
				unit
Control Pin Voltage	V_{CONT} max	1sec	60	V
Control Pin Voltage	V_{CONT} max		41	V
Control Pin Current	I_{CONT} max	*$V_{CC} \geqq 6V$	11	mA
CK Input Voltage	V_{CK} max		25	V
Reset Pin Voltage	$V_{\overline{RES}}$ max, V_{RES} max		41	V
Allowable Power Dissipation	Pd max		500	mW
Operating Temperature	**Topr**		−40 to +85	°C
Storage Temperature	Tstg		−55 to +150	°C

*: A PNP transistor is connected to the LA5690D, 5690S externally to provide a low-saturation voltage regulator. Therefore, $I_{CONT} \leqq 100mA$ will flow, as starting current, in the V_{CC} range where the output cannot be regulated.

Operating Conditions at Ta = 25°C

				unit
Control Pin Voltage	V_{CONT}		6 to 40	V
Control Pin Current	I_{CONT} max		10	mA
Reset Output Current	$I_{\overline{RES}}$ max, I_{RES} max	External R pull-up	8	mA
Reset Detection Voltage	V_S min		4	V

Package Dimensions (unit: mm)
3001B [LA5690D]



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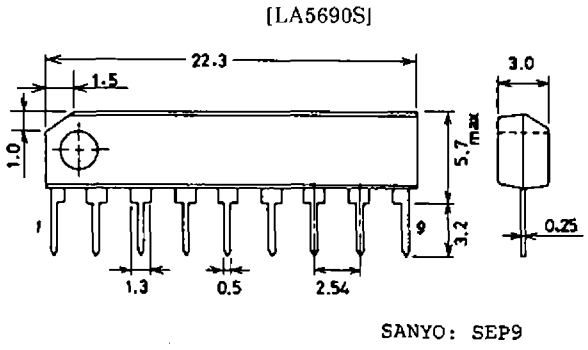
Package Dimensions (unit: mm)
3017B [LA5690S]



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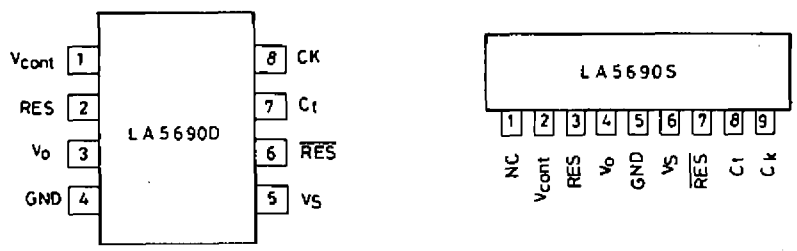
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Operating Characteristics at Ta = 25°C, V_{CC} = 14V, I_O = 50mA, unless otherwise specified

			min	typ	max	unit
Operating Voltage	V_O		4.8	5.0	5.2	V
Line Regulation	ΔV_{OLN1}	9V ≦ V_{CC} ≦ 16V		2	10	mV
	ΔV_{OLN2}	6V ≦ V_{CC} ≦ 40V		4	30	mV
Load Regulation	ΔV_{OLD}	1mA ≦ I_O ≦ 50mA		4	30	mV
Current Dissipation	I_{CC}	I_O = 0		4.9	6.5	mA
Output Noise Voltage	V_{NO}	10Hz ≦ f ≦ 100kHz, V_{CK} = 0		200		μV
Temperature Coefficient of Output Voltage	$\Delta V_O / \Delta Ta$	I_O = 5mA, −40°C ≦ Ta ≦ +85°C		±0.2		mV/°C
Reference Voltage	V_{REF}		1.13	1.18	1.23	V
"H"-Level CK Input Voltage	V_{IH}		2			V
"L"-Level CK Input Voltage	V_{IL}				0.8	V
"H"-Level CK Input Current	I_{IH}	V_{CK} = 5V		0.3	0.7	mA
"L"-Level CK Input Current	I_{IL}	V_{CK} = 0	−1.0	−0.1		μA
"H"-Level Reset Output Voltage	$V_{\overline{ORH}}/V_{ORH}$		4.8	5.0	5.2	V
"L"-Level Reset Output Voltage	$V_{\overline{ORL1}}/V_{ORL1}$			40	200	mV
"L"-Level Reset Output Voltage	$V_{\overline{ORL2}}/V_{ORL2}$	$I_{\overline{RES}} = I_{RES}$ = 8mA		0.16	0.8	V
CK Input Pulse Width	t_{CKW}	V_{CK} = 5V	3			μs
Reset Output Delay Time	t_d	C_t = 1μF	7.5	10	12.5	ms
Watchdog Time	t_{WD}	C_t = 1μF	3.8	5.0	6.2	ms
Watchdog Reset Time	t_{WR}	C_t = 1μF	0.1	0.25	0.4	ms
Reset Hysteresis Voltage	Vhys	V_S = 4.5V	100	200	300	mV

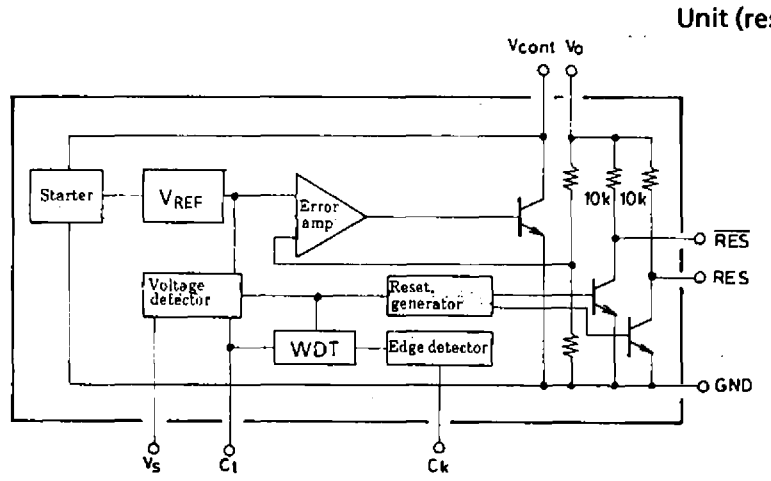
Pin Assignment



The NC pin, which is left open, must not be used for wiring.

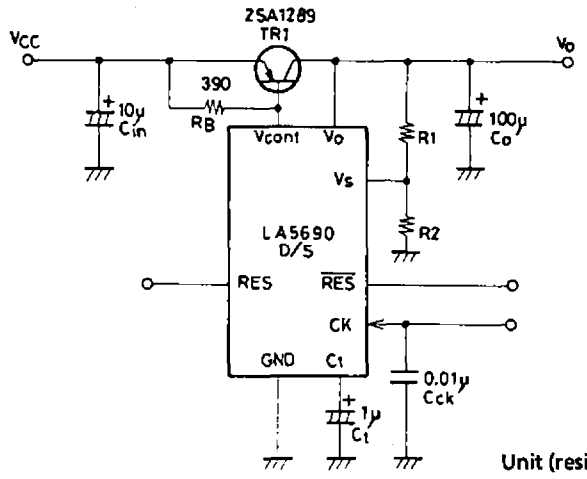
Equivalent Circuit Block Diagram

Unit (resistance: Ω)



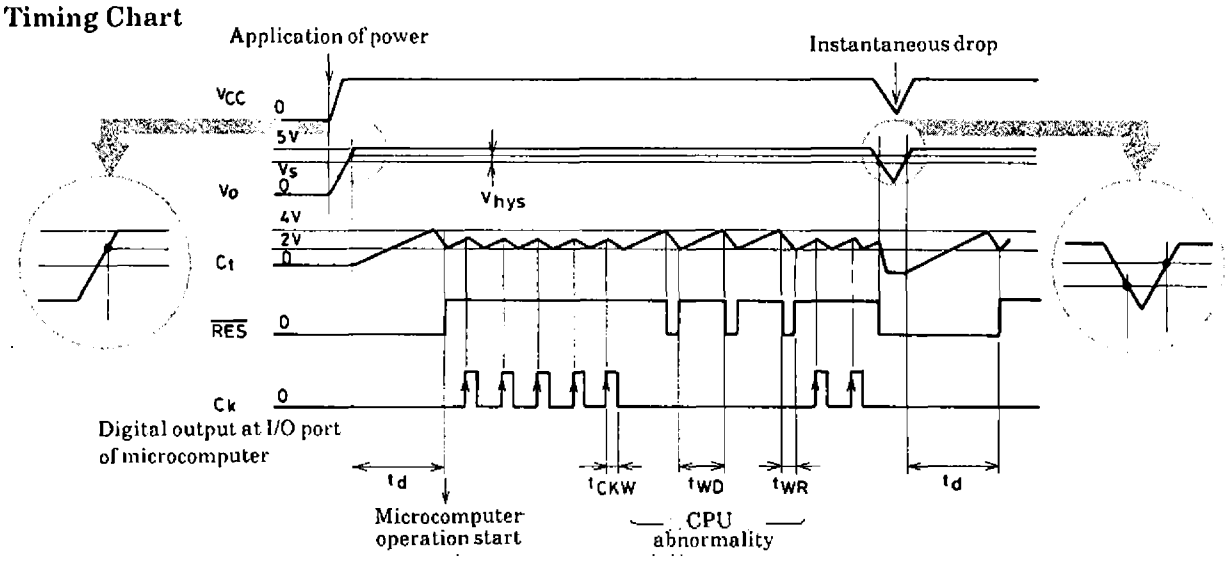
The reset output contains a pull-up resistor of 10kΩ.

Test Circuit



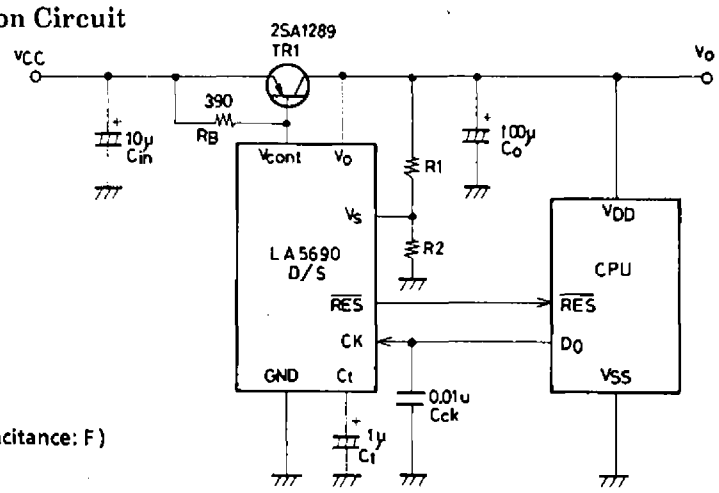
Unit (resistance: Ω, capacitance: F)

Timing Chart



Note : Edge-triggered at the point indicated by the arrow of C_K signal.

Sample Application Circuit



Unit (resistance: Ω, capacitance: F)

TR1 : 2SA1289 (60V/5A, TO-220)

C_t : Sanyo OS capacitor

$V_S = V_{REF} \times (\frac{R1}{R2} + 1)$

$V_{REF} \fallingdotseq 1.18(V)$

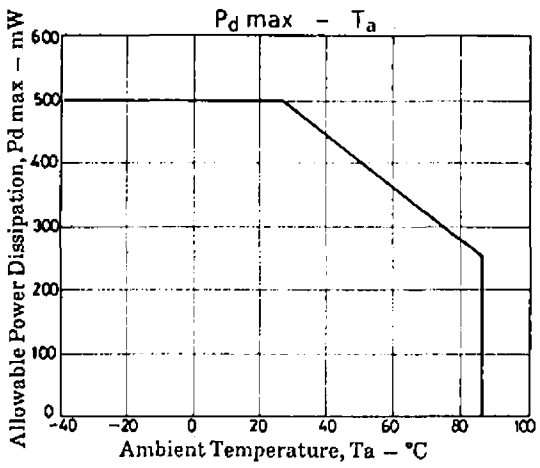
$t_d = 10 \times C_t(\mu F)[ms]$

$t_{WD} = 5 \times C_t(\mu F)[ms]$

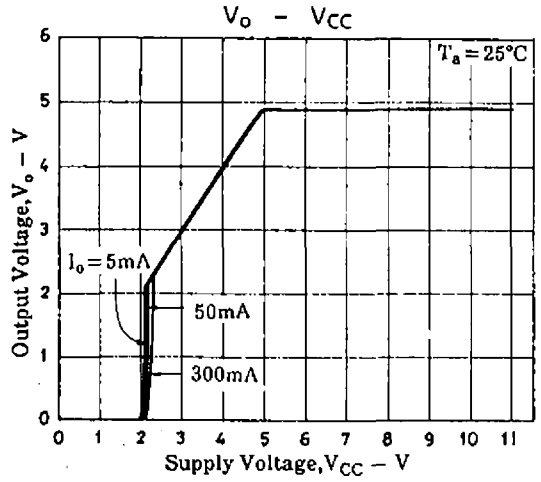
$t_{WR} = 0.25 \times C_t(\mu F)[ms]$

- C_t, C_O : Capacitors whose value does not vary with temperature very much.
- C_{CK} : Must be used to eliminate noise in the reset output.

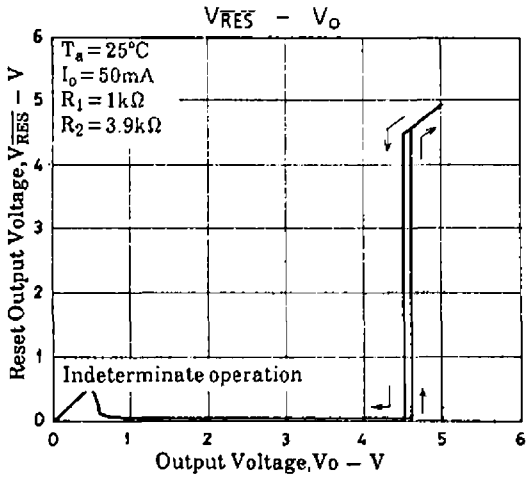
P_d max – T_a



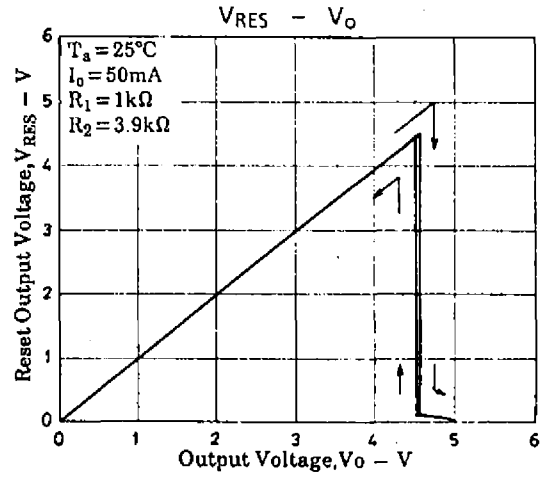
V_O – V_{CC}



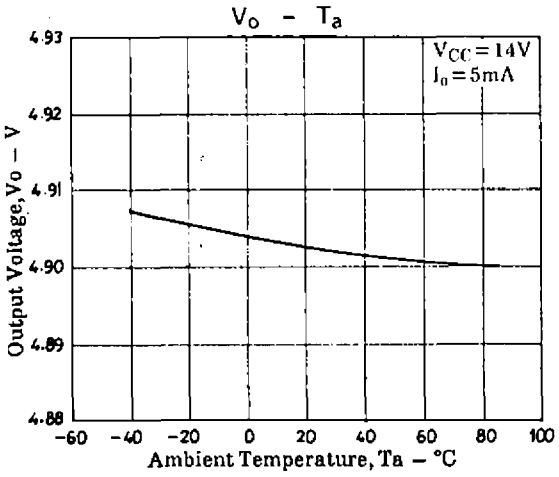
$\overline{V_{RES}}$ – V_O



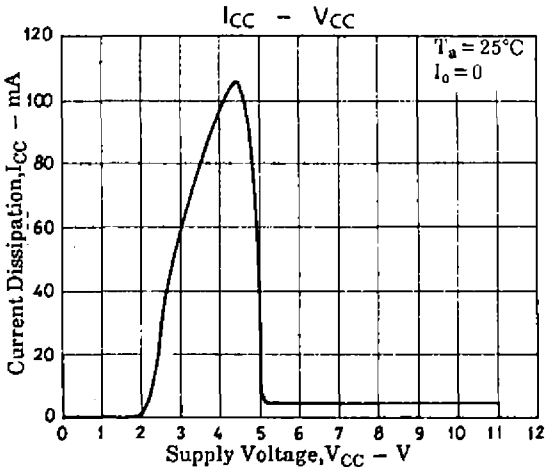
V_{RES} – V_O



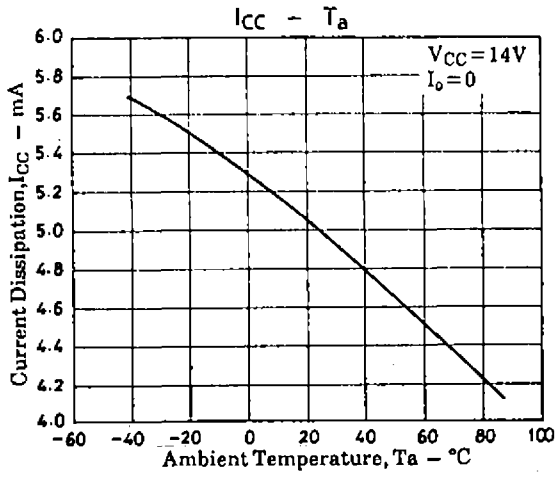
V_O – T_a



I_{CC} – V_{CC}



I_{CC} – T_a



R_{rej} – f