Ordering number: EN 1957A

Monolithic Linear IC

No.1957A

LA6082M

J-FET Input Dual Operational Amplifier

The LA6082M is a J-FET input dual operational amplifier. Application areas include general-purpose control equipment, measuring equipment (very low current measurement, long-integrating circuit, sample & hold circuit, impedance converter, etc.).

Features

- . High slew rate
- . High input impedance
- . Low input bias current
- . Low input offset current
- . No phase compensation required

Maximum Ratings at Ta=25°C

			unit
Maximum Supply Voltage	V_{CC}/V_{EE}	±18	V
Differential Input Voltage	V_{ID}	±30	V
Common-Mode Input Voltage	V_{IN} (Note)	±15	V
Allowable Power Dissipaiton	Pd max	300	mW
Operating Temperature	Topr	-30 to +85	°C
Storage Temperature	Tstg	-55 to +125	°C

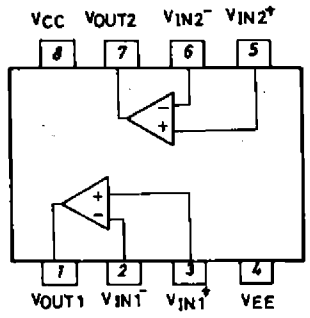
(Note) Allowable in the range of supply voltage. The above value is for V_{CC}=+15V, V_{EE}=-15V.

Operating Characteristics at Ta=25°C, V_{CC}=+15V, V_{EE}=-15V

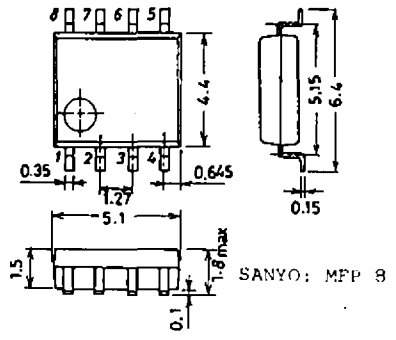
			min	typ	max	unit
Input Offset Voltage	V_{IO}	R_S=50ohms		5.0	15.0	mV
Input Offset Current	I_{IO}			5	200	pA
Input Bias Current	I_B			30	400	pA
Common-Mode Input Voltage Range	V_{ICM}		±10			V
Common-Mode Rejection Ratio	CMR		70	76		dB
Large Amplitude Voltage Gain	VG	$R_L \geq$2kohms, V_O=±10V	25	200		V/mV
Maximum Output Voltage	Vopp1	$R_L \geq$10kohms	±12	±13.5		V
	Vopp2	$R_L \geq$2kohms	±10	±12		V

Continued on next page.

Pin Assignment



Package Dimensions 3032B-M8IC
(unit : mm)

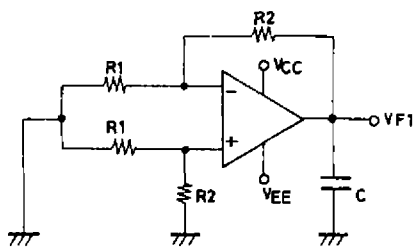


SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Continued from preceding page.			min	typ	max	unit
Supply Voltage Rejection Ratio	SVR		70	76		dB
Supply Current	I_{CC}	$R_L=\infty$		4	5.6	mA
Gain-Bandwidth Product	f_T	$A_V=1$		3		MHz
Equivalent Input Noise Voltage	V_{NI}	R_S=100ohms, f=10Hz to 10kHz		4		uVrms
Input Resistance	r_i			10^{a}		ohm
Channel Separation	ch sep			120		dB
Slew Rate	S·R	R_L=2kohms, C_L=100pF, $A_V=1$, V_{IN}=10V		13		V/us

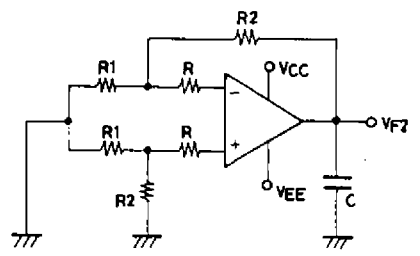
Test Circuits

1. Input Offset Voltage V_{IO}



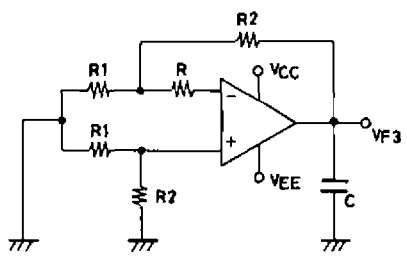
$$V_{IO}=\frac{V_{F1}}{1+R2/R1}$$

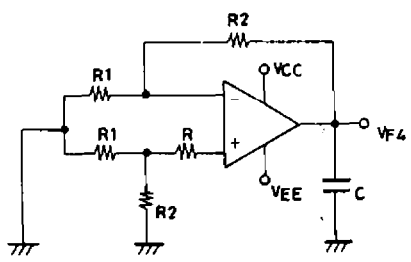
2. Input Offset Current I_{IO}



$$I_{IO}=\frac{V_{F2}-V_{F1}}{R(1+R2/R1)}$$

3. Input Bias Current I_B





$$I_B=\frac{V_{F4}-V_{F3}}{2R(1+R2/R1)}$$

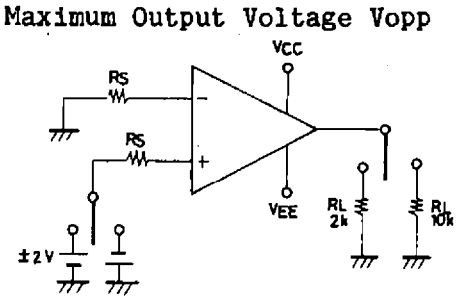
4. Common-Mode Rejection Ratio CMR
   Common-Mode Input Voltage Range V_{ICM}

$$CMR=20\log\left|\frac{(E_{C1}-E_{C2})(1+R2/R1)}{V_{F5}-V_{F6}}\right|$$

5. Voltage Gain VG

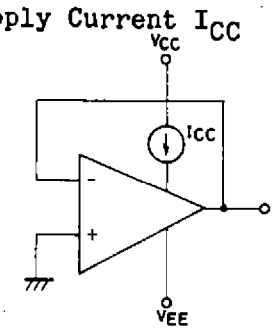
$$VG=\frac{(E_{K1}-E_{K2})(1+R2/R1)}{V_{F8}-V_{F7}}$$

6. Maximum Output Voltage Vopp

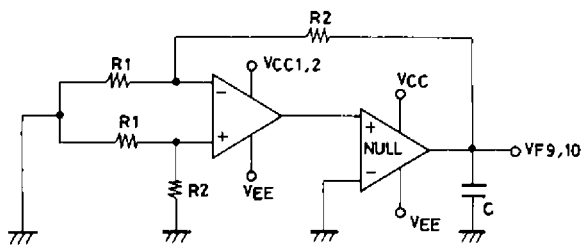


Unit (resistance: Ω)

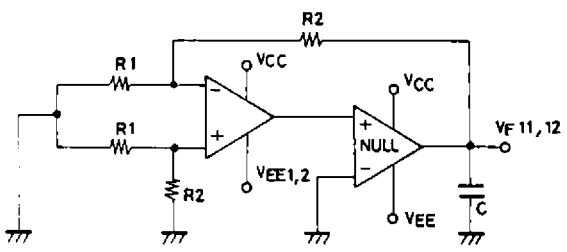
7. Supply Current I_{CC}



8. Supply Voltage Rejection Ratio SVR

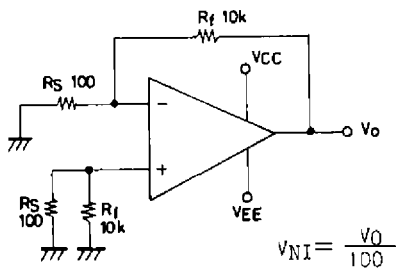


$$SVR(+) = 20\log\left|\frac{(1+R2/R1)(V_{CC1}-V_{CC2})}{V_{F9}-V_{F10}}\right|$$



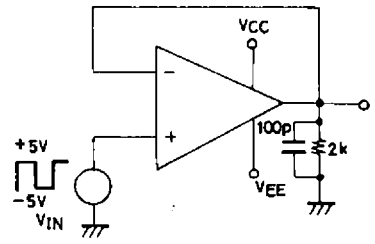
$$SVR(-) = 20\log\left|\frac{(1+R2/R1)(V_{EE1}-V_{EE2})}{V_{F11}-V_{F12}}\right|$$

9. Equivalent Input Noise Voltage V_{NI}



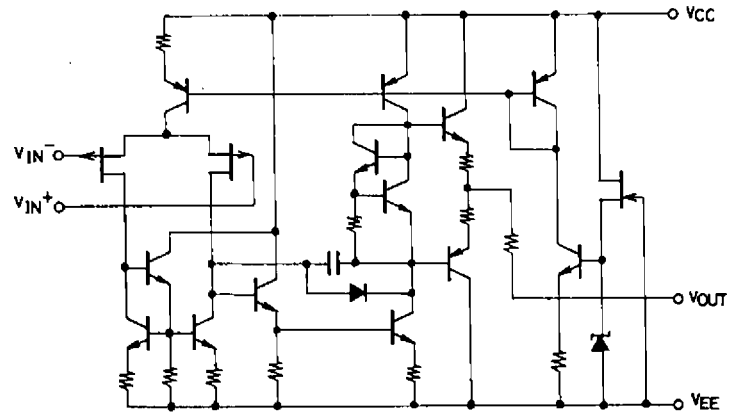
$$V_{NI} = \frac{V_O}{100}$$

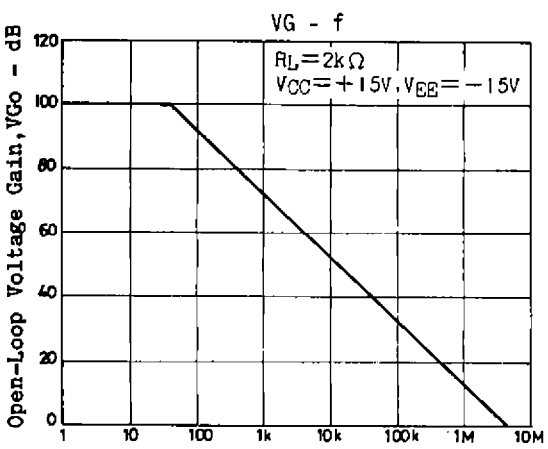
10. Slew Rate SR

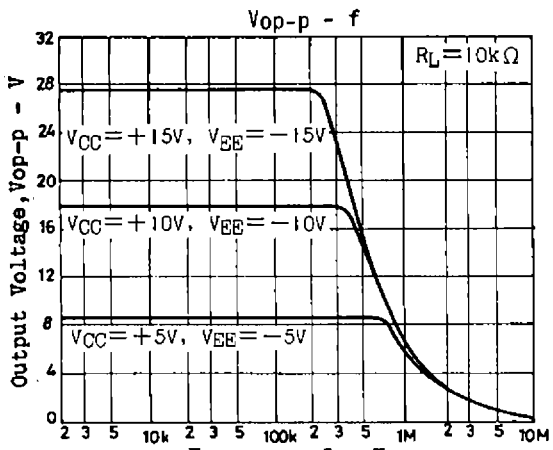


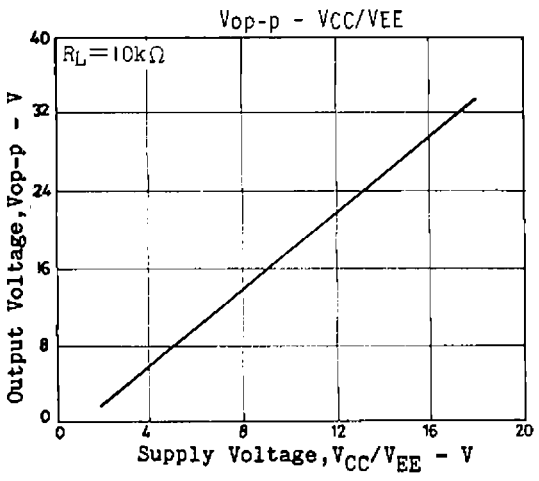
Unit (resistance:Ω capacitance:F)

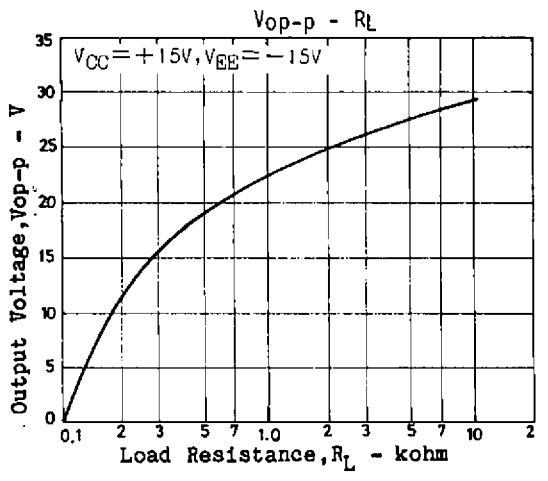
Equivalent Circuit

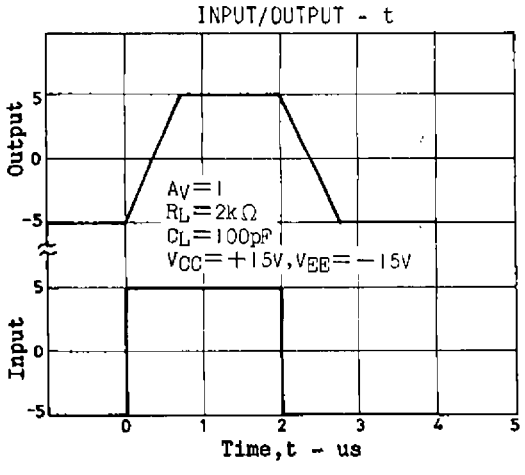


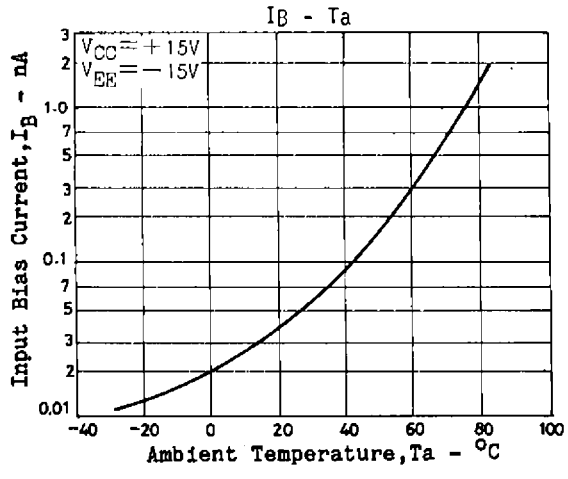

VG - f
RL=2kΩ
VCC=+15V, VEE=−15V
Open-Loop Voltage Gain, VGo - dB
120
100
80
60
40
20
0
1
10
100
1k
10k
100k
1M
10M
Frequency, f - Hz

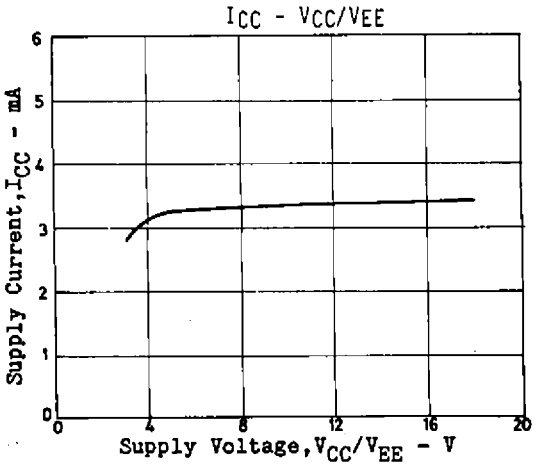

Vop-p - f
RL=10kΩ
VCC=+15V, VEE=−15V
VCC=+10V, VEE=−10V
VCC=+5V, VEE=−5V
Output Voltage, Vop-p - V
32
28
24
20
16
12
8
4
0
2 3 5 10k 2 3 5 100k 2 3 5 1M 2 3 5 10M
Frequency, f - Hz

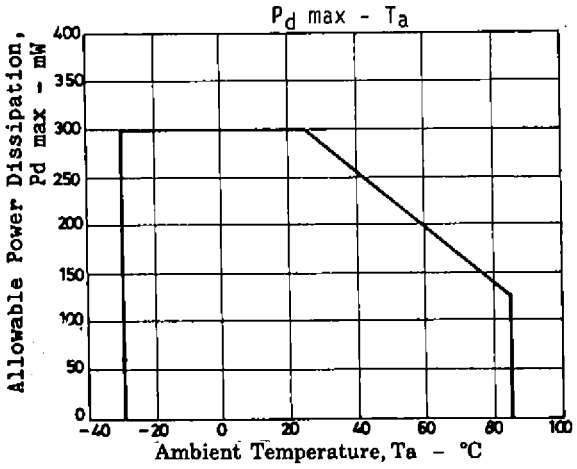

Vop-p - VCC/VEE
RL=10kΩ
Output Voltage, Vop-p - V
40
32
24
16
8
0
0
4
8
12
16
20
Supply Voltage, VCC/VEE - V


Vop-p - RL
VCC=+15V, VEE=−15V
Output Voltage, Vop-p - V
35
30
25
20
15
10
5
0
0.1
2
3
5
7
1.0
2
3
5
7
10
2
Load Resistance, RL - kohm


INPUT/OUTPUT - t
Output
5
0
-5
Input
5
0
-5
AV=1
RL=2kΩ
CL=100pF
VCC=+15V, VEE=−15V
0
1
2
3
4
5
Time, t - us

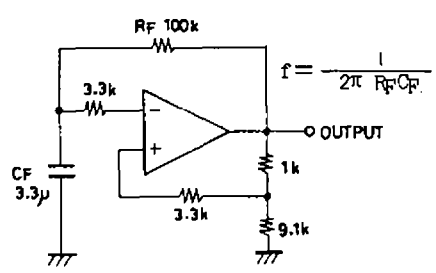

IB - Ta
VCC=+15V
VEE=−15V
Input Bias Current, IB - nA
3
2
1.0
7
5
3
2
0.1
7
5
3
2
0.01
-40
-20
0
20
40
60
80
100
Ambient Temperature, Ta - °C


ICC - VCC/VEE
Supply Current, ICC - mA
6
5
4
3
2
1
0
0
4
8
12
16
20
Supply Voltage, VCC/VEE - V


Pd max - Ta
Allowable Power Dissipation, Pd max - mW
400
350
300
250
200
150
100
50
0
-40
-20
0
20
40
60
80
100
Ambient Temperature, Ta - °C

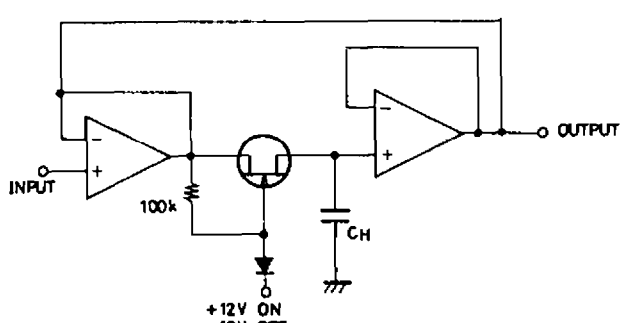
Sample Applicaiton Circuits

Unit (resistance: Ω, capacitance: F)



$$f = \frac{1}{2\pi R_F C_F}$$

0.5Hz SQUARE · WAVE Oscillator



SAMPLE & HOLD