Ordering number: EN 1967B

Monolithic Linear IC

SANYO No.1967B

# LA6082D,6082S

## J-FET Input Dual Operational Amplifiers

The LA6082 is a J-FET input dual operational amplifier. Application areas include general-purpose control equipment, measuring equipment (very low current measurement, long-integrating circuit, sample & hold circuit, impedance converter, etc.).

**Features**

- High slew rate
- High input impedance
- Low input bias current
- Low input offset current
- No phase compensation required

**Maximum Ratings** at Ta=25°C

| | | | unit |
|---|---|---|---|
| Maximum Supply Voltage | $V_{CC}/V_{EE}$ | ±18 | V |
| Differential Input Voltage | $V_{ID}$ | ±30 | V |
| Common-Mode Input Voltage | $V_{IN}$ (Note) | ±15 | V |
| Allowable Power Dissipation | Pd max | 570 | mW |
| Operating Temperature | Topr | -30 to +85 | °C |
| Storage Temperature | Tstg | -55 to +125 | °C |

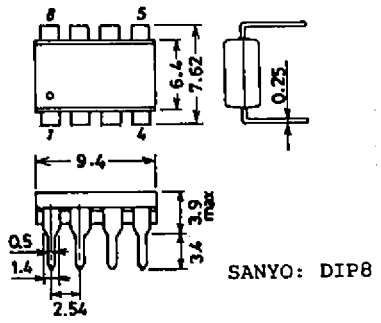
(Note) Allowable in the range of supply voltage. The above value is for $V_{CC}$=+15V, $V_{EE}$=-15V.

**Operating Characteristics** at Ta=25°C, $V_{CC}$=+15, $V_{EE}$=-15V

| | | | min | typ | max | unit |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{IO}$ | $R_S$=50ohms | | 5.0 | 15.0 | mV |
| Input Offset Current | $I_{IO}$ | | | 5 | 200 | pA |
| Input Bias Current | $I_B$ | | | 30 | 400 | pA |
| Common-Mode Input Voltage Range | $V_{ICM}$ | | ±10 | | | V |
| Common-Mode Rejection Ratio | CMR | | 70 | 76 | | dB |
| Large Amplitude Voltage Gain | VG | $R_L \geqq$2kohms, Vo=±10V | 25 | 200 | | V/mV |
| Maximum Output Voltage | Vopp1 | $R_L \geqq$10kohms | ±12 | ±13.5 | | V |
| | Vopp2 | $R_L \geqq$2kohms | ±10 | ±12 | | V |

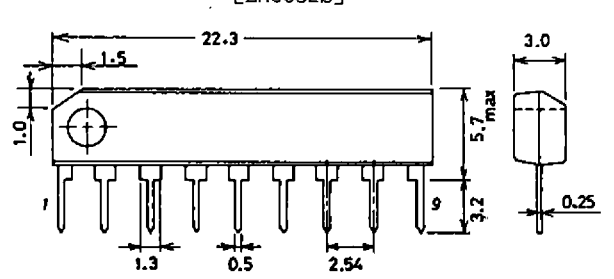
Continued on next page.

Package Dimensions 3001B-D8IC
(unit: mm) [LA6082D]




SANYO: DIP8

Package Dimensions 3017B-S9IC
(unit: mm) [LA6082S]




SANYO: SEP9

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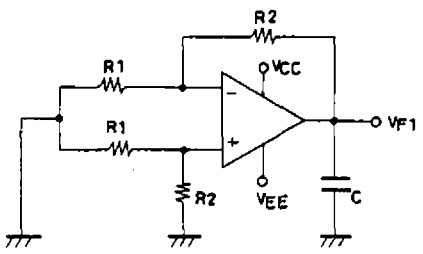
TOKYO OFFICE Tokyo Bldg.,1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

| Continued from preceding page. | | | min | typ | max | unit |
|---|---|---|---|---|---|---|
| Supply Voltage Rejection Ratio | SVR | | 70 | 76 | | dB |
| Supply Current | $I_{CC}$ | $R_L=\infty$ | | 4 | 5.6 | mA |
| Gain-Bandwidth Product | $f_T$ | $A_V=1$ | | 3 | | MHz |
| Equivalent Input Noise Voltage | $V_{NI}$ | $R_S$=100ohms, f=10Hz to 10kHz | | 4 | | uVrms |
| Input Resistance | $r_i$ | | | $10^{12}$ | | ohm |
| Channel Separation | C·S | | | 120 | | dB |
| Slew Rate | S·R | $R_L$=2kohms, $C_L$=100pF, $A_V=1$, $V_{IN}=10V$ | | 13 | | V/us |

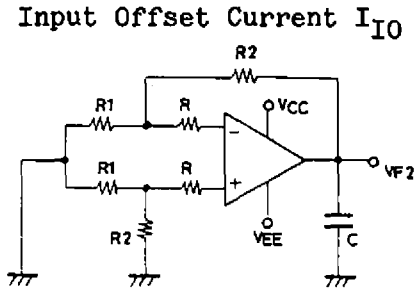
**Test Circuits**

1. Input Offset Voltage $V_{IO}$



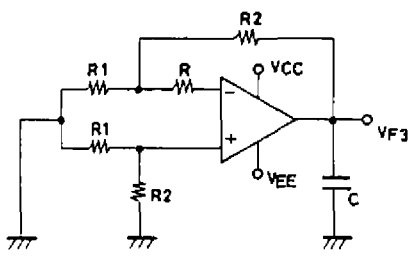

$$V_{IO}=\frac{V_{F1}}{1+R2/R1}$$

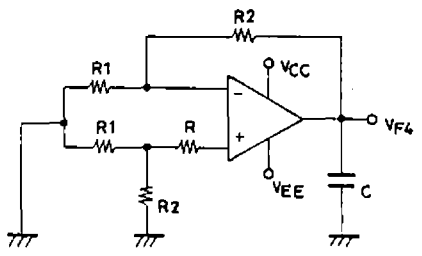
2. Input Offset Current $I_{IO}$




$$I_{IO}=\frac{V_{F2}-V_{F1}}{R(1+R2/R1)}$$

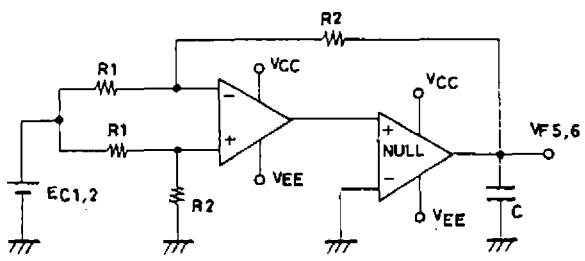
3. Input Bias Current $I_B$



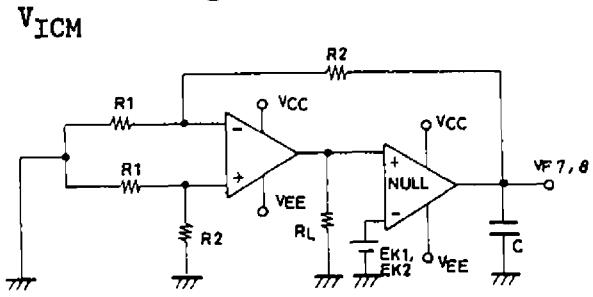

$$I_B=\frac{V_{F4}-V_{F3}}{2R(1+R2/R1)}$$

4. Common-Mode Rejection Ratio CMR
   Common-Mode Input Voltage Range $V_{ICM}$



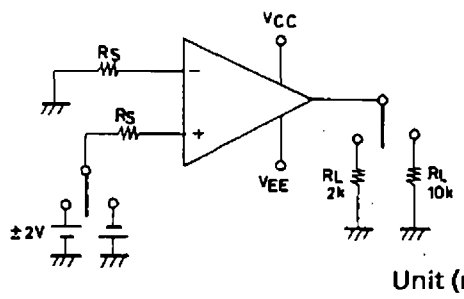

$$CMR=20\log\left|\frac{(E_{C1}-E_{C2})(1+R2/R1)}{V_{F5}-V_{F6}}\right|$$

5. Voltage Gain VG

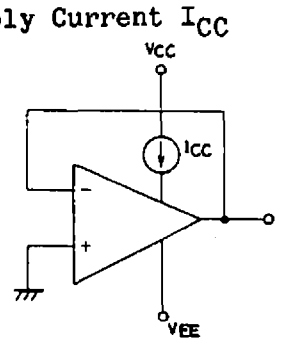



$$VG=\frac{(E_{K1}-E_{K2})(1+R2/R1)}{V_{F8}-V_{F7}}$$

6. Maximum Output Voltage Vopp

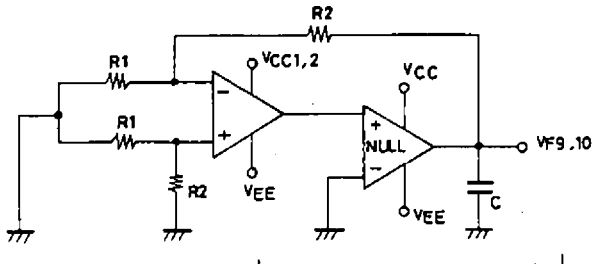



7. Supply Current $I_{CC}$

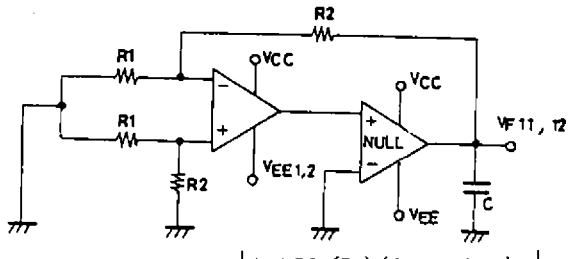



Unit (resistance: Ω)

## 8. Supply Voltage Rejection Ratio SVR

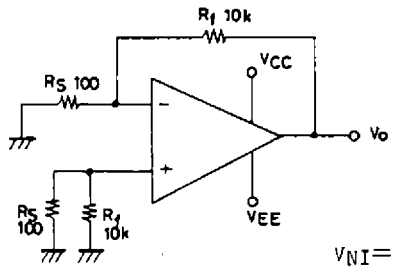



$$SVR(+) = 20\log \left| \frac{(1+R2/R1)(V_{CC1}-V_{CC2})}{V_{F9}-V_{F10}} \right|$$

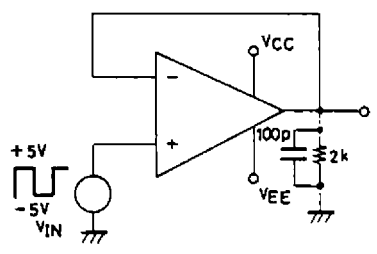



$$SVR(-) = 20\log \left| \frac{(1+R2/R1)(V_{EE1}-V_{EE2})}{V_{F11}-V_{F12}} \right|$$

## 9. Equivalent Input Noise Voltage $V_{NI}$ 10. Slew Rate SR

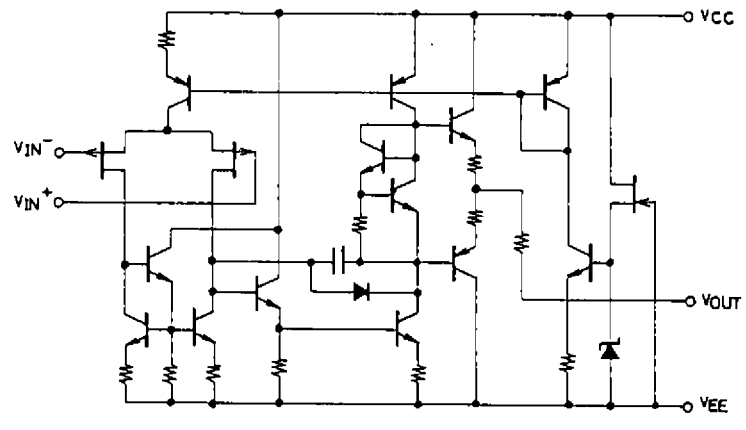



$$V_{NI} = \frac{V_O}{100}$$



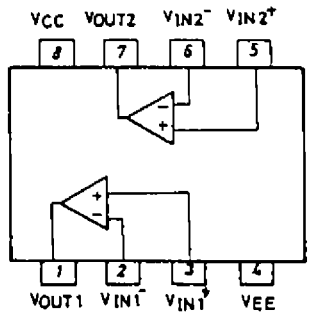

Unit (resistance:Ω capacitance:F)

## Equivalent Circuit

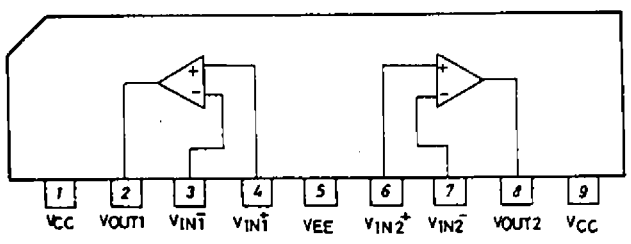



## Pin Assignment

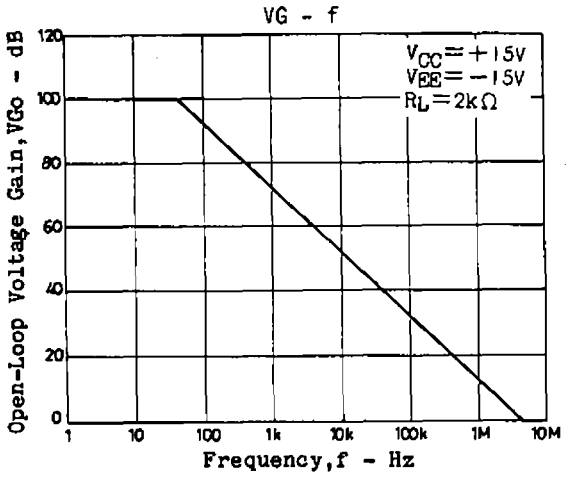
[LA6082D]



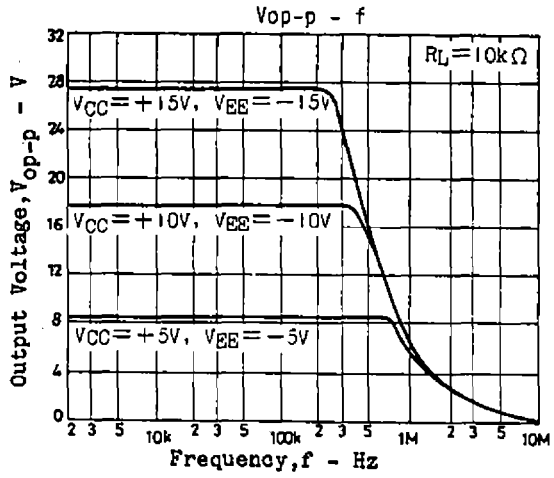

[LA6082S]



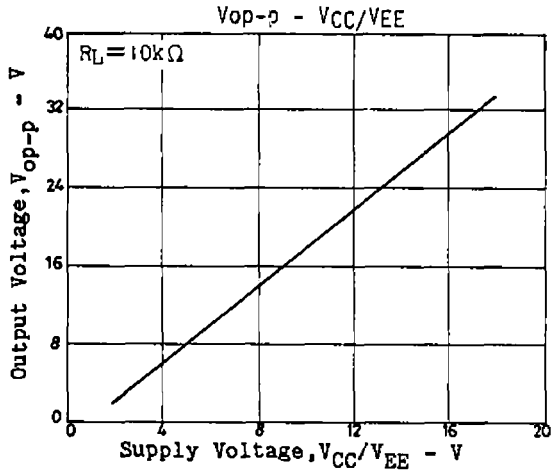
VG - f



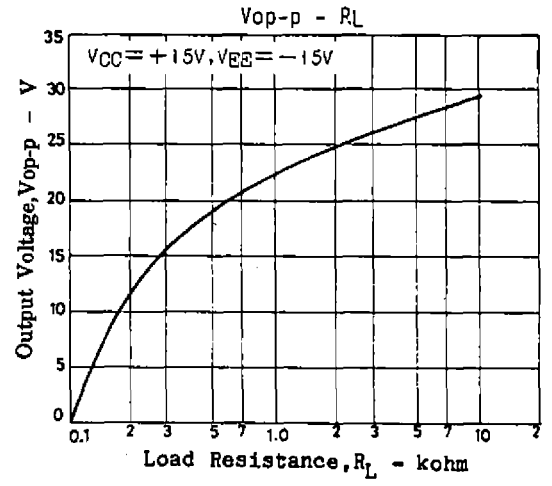

Vop-p - f



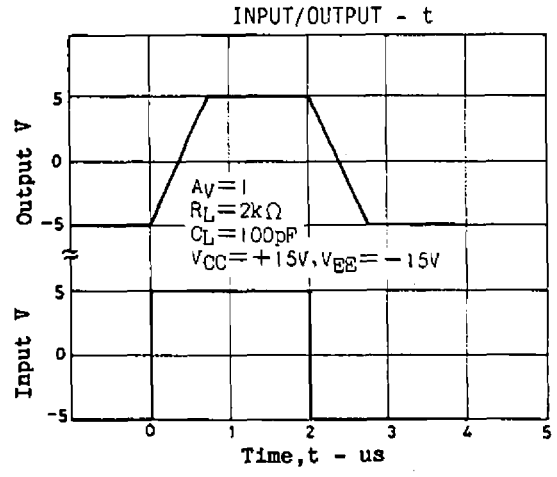

Vop-p - VCC/VEE



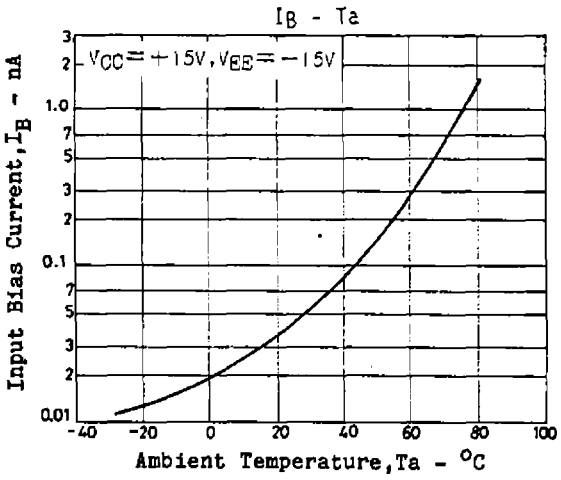

Vop-p - RL



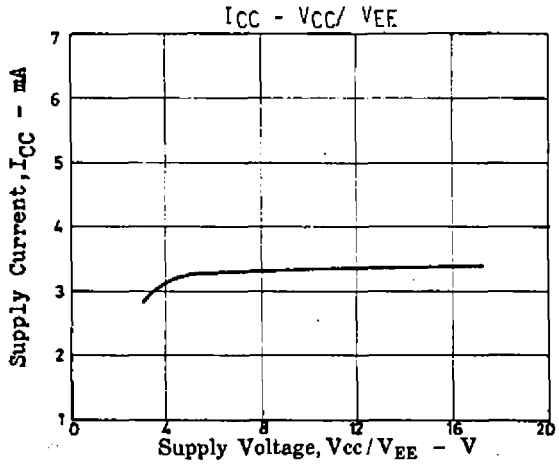

INPUT/OUTPUT - t



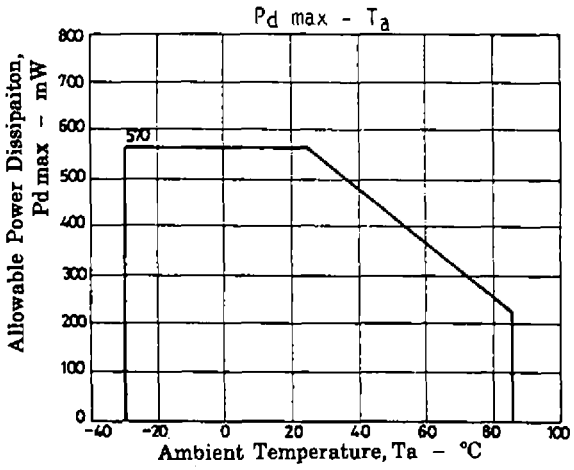

IB - Ta




ICC - VCC/ VEE

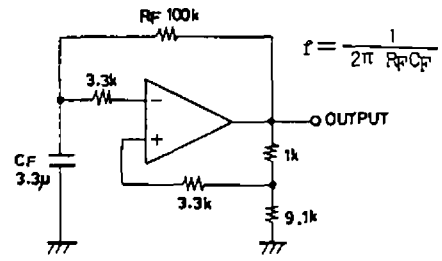



Pd max - Ta

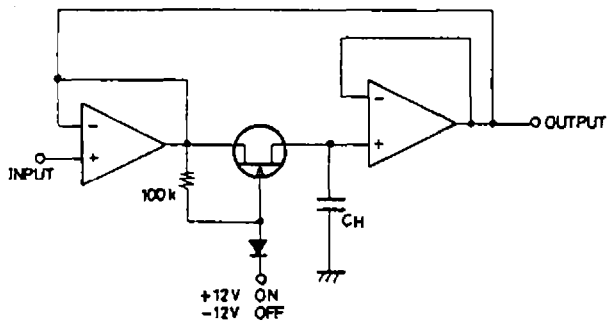


## Application Circuits

Unit (resistance: Ω, capacitance: F)




0.5Hz SQUARE WAVE OCSILLATOR




SAMPLE & HOLD

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