

LA70001, 70001M

Record/Playback Amplifiers for VHS Format VCRs

Overview

The LA70001 and LA70001M ICs provide record and playback amplifiers for VHS format VCRs. A system with an adjustment-free Y/C record current can be achieved by combining the LA70001/M with an LA71000M or LA71500M video signal processing IC.

Features

- Direct connection of the head to the playback amplifier input allows the number of external devices to be reduced.
- A fixed-current drive technique that is strongly resistant to load fluctuations is adopted in the record amplifier for stable recording characteristics. The record amplifier includes a built-in AGC circuit.
- These products have the same package dimensions as the LA70011 and LA70011M to allow a common PCB to be used. These products can also share the same PCB with the LA70020 by mounting the IC at the right end of the LA70020 socket.

Package Dimensions

unit: mm

3067-DIP24S



unit: mm

3112-MFP24S



Specifications Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7.0	V
		Ta ≤ 65°C [LA70001]	600	mW
Allowable power dissipation	Pd max	Ta \leq 65°C [LA70001M] (Using a 114.3 \times 76.1 \times 1.6 mm glass epoxy PCB)	500	mW
Operating temperature	Topr		-10 to +65	°C
Storage temperature	Tstg		-40 to +150	°C

Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		5.0	V
Operating supply voltage range	V _{CC} op		4.8 to 5.5	V

SANYO Electric Co., Ltd. Semiconductor Bussiness Headquarters TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-0005 JAPAN

Electrical Characteristics at $Ta = 25^{\circ}C$

Parameter		Symbol	Conditions		Ratings		Unit
T didinition		Cynibol		min	typ	max	
[Playback Mode]							
Current drain		I _{CCP}	The pin 13 inflow current.	23	29	35	mA
Voltage gain	CH1	G _{VP} 1	V _{IN} = 38 m Vp-p, f = 1 MHz	56	59	62	dB
Vonago gam	CH2	G _{VP} 2		56	59	62	dB
Voltage gain difference 1		ΔG_{VP} 1	G _{VP} 1—G _{VP} 2	-1	0	+1	dB
Equivalent input noise voltage	CH1 CH2	V _{NIN} 1 V _{NIN} 2	With the same conditions as for the voltage gain, the ratio of the output passed through a 1.1-MHz low-pass filter and the output with no input signal.		1.0	1.5	μVrms
Frequency characteristics	CH1	ΔV_{fp} 1	The ratio of the output for $V_{IN} = 38 \text{ mVp-p}$,				
	CH2	ΔV _{fp} 2	$f = 7 \text{ MHz}$ and G_{VP} 1, 2, 3, and 4.	-2.5	0		dB
Second harmonic distortion	CH1 CH2	V _{HDP} 1 V _{HDP} 2	With V_{IN} = 38 mVp-p, f = 4 MHz, the ratio of the 8-MHz output component (second harmonic) and the 4-MHz component (the fundamental).		-40	-35	dB
Maximum output level CH1 CH2		V _{OMP} 1 V _{OMP} 2	At f = 1 MHz, the output level when the ratio of the 3-MHz output (third harmonic) and the 1-MHz output (fundamental) is -30 dB.	1.0	1.2		Vр-р
Crosstalk SP		V _{CR} 1	The ratio of the V _{IN} = 38 mVp-p, f = 4 MHz output and G_{VP} 1.		-40	-35	dB
Output DC offset		ΔV_{ODC} 1	CH1 – CH2	-100	0	+100	mV
Envelope detector output pin vol	tage	V _{ENV}	The T6 DC level when there is no input signal.	0	0.8	1.3	V
		V _{ENVSP} 1	With a f = 4 MHz input, the T6 DC level when the T7A output level becomes 175 mVp-p.	2.0	2.5	3.0	V
Envelope detector output pin vol	tage SP1	V _{ENVSP} 2	With a f = 4 MHz input, the T6 DC level when the T7A output level becomes 400 mVp-p.	3.5	4.0	4.5	V
		V _{ENVEP} 1	With a f = 4 MHz input, the T6 DC level when the T7A output level becomes 125 mVp-p.	2.0	2.5	3.0	V
Envelope detector output pin vol	tage EP	V _{ENVEP} 2	With a f = 4 MHz input, the T6 DC level when the T7A output level becomes 300 mVp-p.	4.0	4.5	5.0	V
Switch transistor on resistance ir mode	n playback	R _{PON} 18	Measure the difference in the DC levels with a 1-mA and a 2-mA inflow current.		4	6	Ω
SW30 threshold level		SW30-1	$Lch \rightarrow Hch *1$	1.2		5.0	V
		SW30-2	$Hch \rightarrow Lch$	0.0		0.8	V
Record Mode]							
Current drain		I _{CCR}	The pin 13 inflow current.	43	50	57	mA
Record AGC amplifier output lev	rel	V _{RSP}	The output level when V_{IN} = 400 mVp-p, f = 4 MHz.	105	112	119	mVp-
Record AGC amplifier control		∆V _{AGC} 1-SP	At f = 4 MHz, when V _{IN} = 700 mVp-p: the output level /VRSP, EP		0.5	1.0	dB
characteristics		ΔV _{AGC} 2-SP	At $f = 4$ MHz, when $V_{IN} = 100$ mVp-p: the output level /VRSP, EP	-1.0	-0.5		dB
Record AGC amplifier frequency characteristics	,	ΔV_{FRS}	At V_{IN} = 400 mVp-p, the ratio of the outputs when f is 1 MHz and 7 MHz, i.e. the ratio of the 7-MHz value to the 1-MHz value.*2.	-1	0	+1	dB
Record AGC amplifier second had distortion	armonic	ΔV_{HDRS}	With V_{IN} = 400 mVp-p, f = 4 MHz, the ratio of the 8-MHz output component (second harmonic) and the 4-MHz component (the fundamental).		-45	-40	dB
Record AGC amplifier maximum	output level	ΔV_{MOSP}	At f = 4 MHz, the output level at which the second harmonic goes to -35 dB. $*3$	20	22		mAp-j
Record AGC amplifier muting att	tenuation	ΔV_{MRS}	When V _{IN} = 400 mVp-p and f = 4 MHz, the output level/VRSP, EP		-45	-40	dB
Record AGC amplifier cross mod relative level	dulation	ΔV _{CYS}	$\begin{array}{l} \mbox{T9A: } V_{IN} = 400 \mbox{ mVp-p, } f = 4 \mbox{ MHz} \\ \mbox{T10A: } V_{IN} = 2.4 \mbox{ Vp-p, } f = 629 \mbox{ kHz} \\ \mbox{The ratio of the } (4 \mbox{ MHz} \pm 629 \mbox{ kHz}) \mbox{ and the } 4 \mbox{MHz outputs.} \end{array}$		-45	-40	dB
Record muting threshold lovel		MUTE-1	MUTE OFF \rightarrow MUTE ON *1	1.2		2.8	V
Record muting threshold level		MUTE-2	MUTE ON \rightarrow MUTE OFF	3.2		5.0	V
Popord mode to playback made the	prochold lovel	PB-REC	$PB \rightarrow REC *1$	1.2		5.0	V
Record mode to playback mode th	II COLULU IEVEI	REC-PB	$REC \to PB$	0.0		0.8	V

Notes:Use a resistor with an accuracy of 1.0% for the resistor between pins 13 and 14. *1. This is the voltage application point *2. Here, fix the AGC amplifier gain by applying a 1.8-V DC level to the AGC detector filter pin (pin 15). *3. Here, adjust the output level by applying a DC voltage to the REC-CUR-Adj pin (pin 12).

Pin Functions

Pin No.	Pin name	Standa	rd DC voltage (V)	Equivalent circuit	Notes
1	N.C				
2	N.C				
3	HA (EP/SP)				EP 1.5 V SP
4	SW30			4 1kΩ SW30 Comp 1V 1V A09397	Hch Lch
5	H-SYNC			5 20kΩ 80kΩ 409398	SYNC H L 1.5 V
6	ENVDET-OUT	РВ	Provided in a separate document.		
		REC	0	20kΩ →→→ 	
7	PB-OUT	РВ	1.7		
		REC	2.1	(7) → ↓ 1 mA → × × × × × × × × × × × × ×	
8 20	GND				

Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Standa	ard DC voltage (V)	Equivalent circuit	Notes
9 REC-Y-IN		PB	4.0	300Ω 5kΩ 	
		REC	3.7		
10		PB	4.0	10 25kΩ 300Ω 5kΩ 	
10 REC-C-IN		REC	3.7		
11	REC/MUTE/PB			20kΩ PB/REC 12.4V 1) PB/REC 777 80kΩ 777 0.8V 7777 A09403	REC 3.0 V MUTE 1.0 V
12	REC-CURRENT-ADJ2	PB	2.5 V	100kΩ 100kΩ 300Ω 12 	
		REC	2.5 V	100kΩ 7777 A09404	
13	V _{CC}				
14	REC-CURRENT-ADJ1	PB	5.0		
		REC	4.5		

Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Standa	rd DC voltage (V)	Equivalent circuit	Notes
15 REC-AGC		PB	0		
	RECAGONIET	REC	1.6	10kΩ 70μA 10kΩ 777 600Ω 777 409406	
16	L IN H IN	PB	2.1	REC ON VCC	
19		REC	4.1		
17	REC_SP_OUT	PB	2.1 V	-PB-ON -PB-ON - - - - - - - - - - - - -	
		REC	4.1 V		
18	PB FILT		0	18 20kΩ PB-ON 77777 A09409	
		REC	2.5		
21 22 23 24	N.C				

Usage Notes

Control Pin Logic

• HA-SW (EP/SP mode switching): pin 3



GND < the pin 3 DC level < 1.5 V: SP mode 1.5 V < the pin 3 DC level < 5 V: EP mode

• H.SYNC input: pin 5



The pin 5 DC level > 1.5 V: The horizontal synchronization period

In record mode: Used as the REC-AGC-AMP synchronization block gate pulse.

• REC/REC-MUTE/PB switching: pin 11



GND < the pin 11 DC level < 1.0 V: Playback mode1.0 V < the pin 11 DC level < 3.0 V: Record mode with recording muted. 3.0 V < the pin 11 DC level < 5.0 V: Record mode

Envelope detection characteristics: pin 6

The LA70001 provides a built-in playback signal envelope detection circuit so that the tracking adjustment can be made automatic.



Envelope Detection Voltage Characteristics

Record Amplifier Gain Control

The LA70001 achieves an adjustment-free record current by adding an AGC circuit in the record amplifier block. The record current can be modified using the following method.



- Record current adjustment 2: When left open.
- Pin 12 DC level is set to $1/2 V_{CC}$ (approximately 2.5 V) by an internal bias, and the record current is determined by Ro1.
- Design value: When Ro1 is 1.5 k Ω , the record current will be 12.7 mA per channel.
- Record current adjustment 2: When used.

The gain can be varied by -6.0 dB to +3.5 dB relative to the value set by Ro1 by applying a control DC voltage of between 1 and 4 V to pin 12.

Record current (mAp-p) design value



Note: The technique shown in the figure below can be used to apply a DC level to pin 12. This allows a control voltage of between 1 and 4 V to be applied.



Block Diagram



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of January, 1998. Specifications and information herein are subject to change without notice.