Ordering number: EN4040

Monolithic Linear IC

No.4040

LA7282,7282M

VCR Audio Signal Recording/ Playback Processor

Overview

The LA7282 and 7282M are small package LSIs containing all functions necessary to record and playback VTR audio signal.

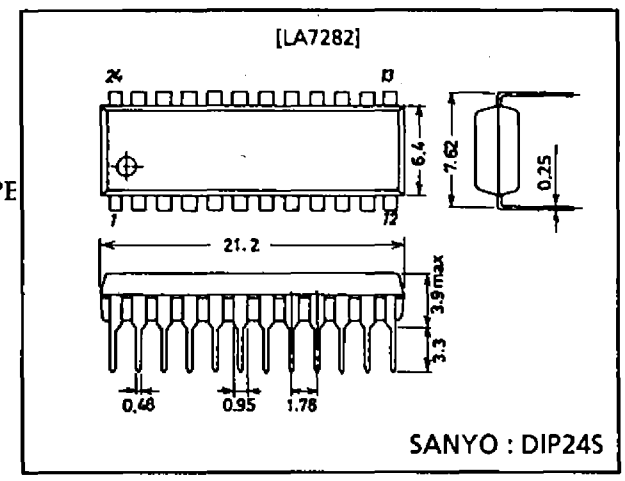
Features

- Smaller package leaves large space for other components.
- Delete of In and Output electrolysis capacitor.
- Low capacitor (0.1 μF)for the line amp inputs (PB IN and AUDIO IN)
- Non-Adjustment of PB Gain by less gain scatter

Package Dimensions

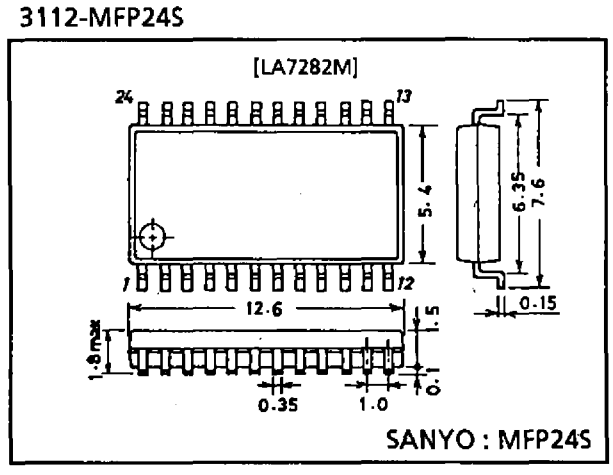
unit : mm

3067-DIP24S

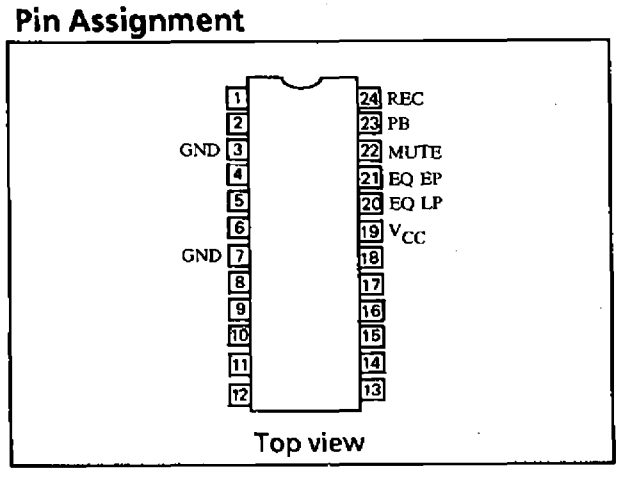


unit : mm

3112-MFP24S



Pin Assignment



SANYO Electric Co.,Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg.,1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Maximum Ratings at Ta = 25°C				unit
Maximum Supply Voltage	V_{CC} max		14	V
Pin 1 Input Voltage	V_{IN1}	Ta = 65°C, f = 80 kHz (sin), I_{LK} = 10 μA	90 (±45)	Vp-p
Pin 1 Input Current	I_{IN1}		±1.5	mA
Allowable Power Dissipation	Pd max	Ta≤65°C, when mounted on the recommended PCB	400	mW
Operating Temperature	Topr		-10 to +65	°C
Storage Temperature	Tstg		-55 to +125	°C

Operating Conditions at Ta = 25°C				unit
Recommended Supply Voltage	V_{CC}		12.0	V
Operating Voltage Range	V_{CC} op		11.25 to 12.75	V

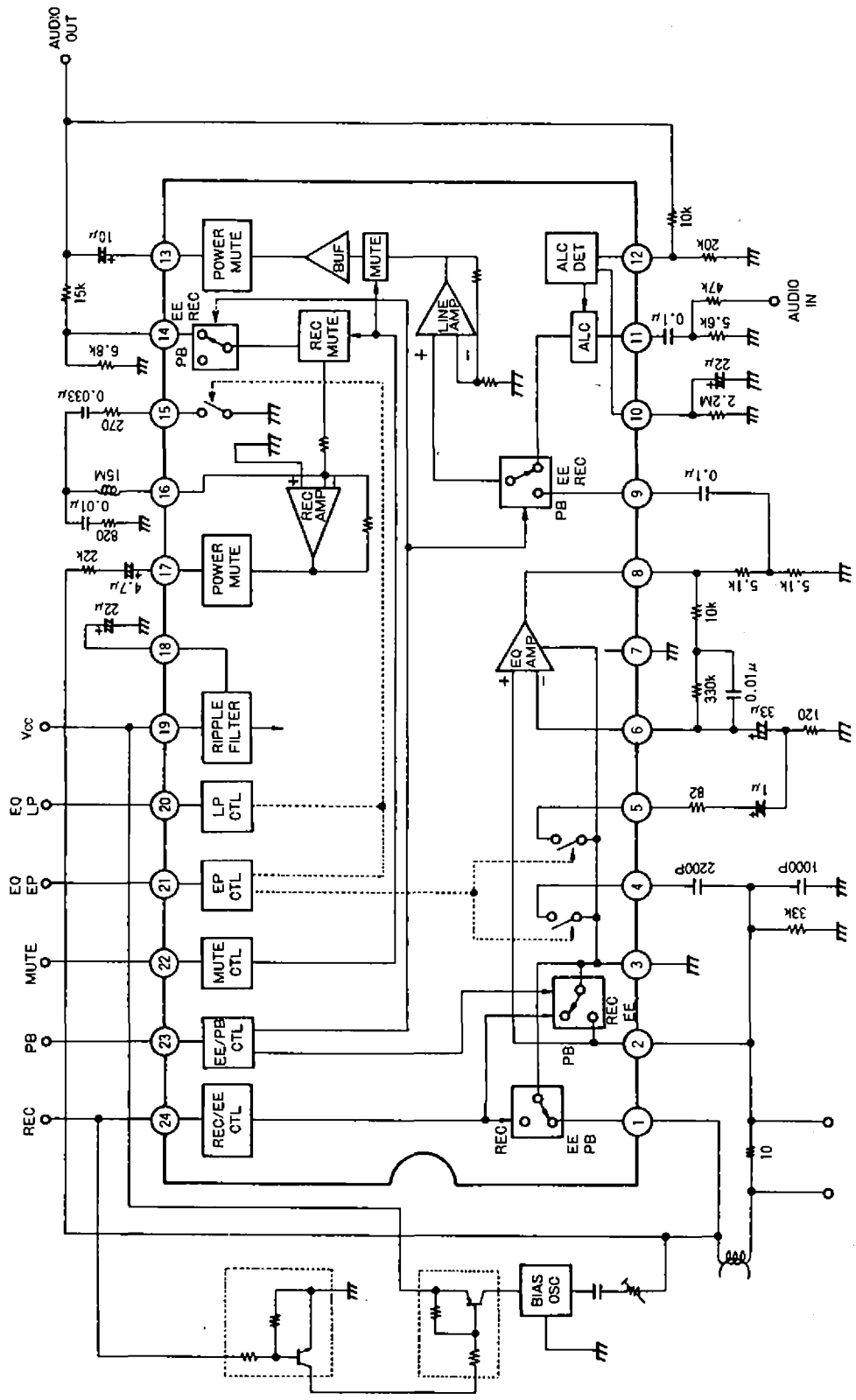
Operating Characteristics at Ta = 25°C, V_{CC} = 12 V, f = 1 kHz, OdBv = :1.0 Vrms

			min	typ	max	unit
Current Dissipation (EE)	I_{CCE}	Quiescent	8.0	12.0	17.0	mA
Current Dissipation (PB)	I_{CCP}	Quiescent	9.0	13.0	18.0	mA
Current Dissipation (REC)	I_{CCR}	Quiescent	7.0	10.0	14.0	mA
Overall Gain at PB Mode	VG_{PB}	EQ IN-LINE OUT, V_O = -5 dBv	59.0	59.5	60.0	dB
[Equalizing Amp]						
Open Loop Voltage Gain	VG_{OE}	V_O = -5 dBv	66.0	71.0		dB
Equivalent Input Noise Voltage	V_{NIE}	Rg = 2.2 kΩ, DIN Audio Filter		1.2	1.8	μVrms
Input Impedance	Z_{INE}			130		kΩ
[Line Amp]						
Voltage Gain (PB IN)	VG_{LP}	V_O = -5 dBv	21.0	21.5	22.0	dB
Voltage Gain (EE,REC IN)	VG_{LR}	V_O = -5 dBv	21.0	21.5	22.0	dB
Total Harmonic Distortion	THD_L	V_O = -5 dBv		0.3	0.5	%
Output Noise Voltage	V_{NOL}	DIN Audio Filter		-70.0	-64.0	dBv
Input Impedance (PB IN)	Z_{IN1}			120		kΩ
Input Impedance (EE,REC IN)	Z_{IN2}			120		kΩ
Maximum Output Voltage	V_{OML}	THD = 3%	1.5	2.1		Vrms
Output Voltage at ALC	V_{OA}	V_{IN} = -28 dBv	-9.0	-8.0	-7.0	dBv
ALC Effect	ALC	V_{IN} = -28 to -8 dBv		1.5	3.0	dB
Total Harmonic Distortion at ALC	THD_A	V_{IN} = -28 dBv		0.25	0.6	%
[Recording Amp]						
Voltage Gain (open loop)	VG_{OR}	V_O = -5 dBv	47.0	52.0		dB
Voltage Gain (closed loop)	VG_{CR}	V_O = -5 dBv	12.5	13.0	13.5	dB
Total Harmonic Distortion	THD_R	V_O = -5 dBv		0.1	0.3	%
Input Impedance	Z_{INR}			50		kΩ
Maximum Output Voltage	V_{OMR}	THD = 3%	1.5	2.0		Vrms
[Muting Circuit]						
On Voltage	V_{MON}	Pin 22, DC	3.8		6.0	V
Off Voltage	V_{MOFF}	Pin 22, DC	0		1.0	V
Mute Attenuation Level (PB,EE)	M_P, M_E		80.0	90.0		dB
Mute Attenuation Level (REC)	M_R		65.0	70.0		dB
[PB/EE Selector Circuit]						
PB Mode Hold Voltage	V_{PP}	Pin 23, DC	0		1.0	V
EE Mode Hold Voltage	V_{PE}	Pin 23, DC	3.3		6.0	V
[REC/EE Selector Circuit]						
REC Mode Hold Voltage	V_{RR}	Pin 24, DC	3.3		V_{CC}	V
EE Mode Hold Voltage	V_{RE}	Pin 24, DC	0		1.0	V

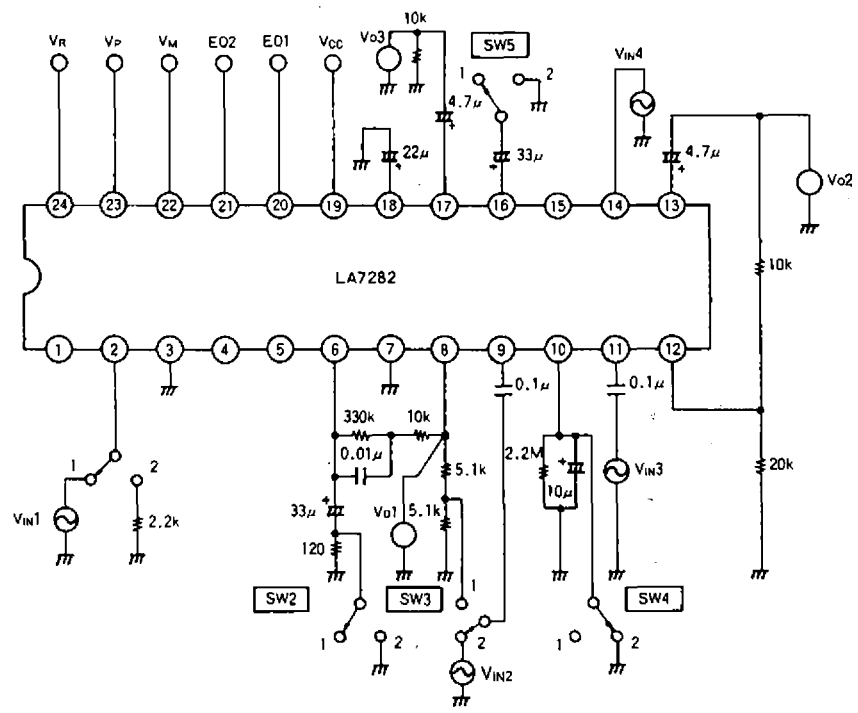
Continued on next page.

			min	typ	max	unit
[Equalizer Selector Circuit]						
Switch On Voltage	V_{EON}	Pin 20, 21, DC	3.5		6.0	V
Switch Off Voltage	V_{EOFF}	Pin 20, 21, DC	0		0.8	V
[Head Selector Switch]						
Pin 1 On Resistance	R_{ON1}	I1 = ±1 mA		15	30	Ω
Pin 2 On Resistance	R_{ON2}	I2 = ±1 mA		5	10	Ω
Pin 1 Input Voltage	V_{IN1}	Ta = 65°C, f = 80 kHz (sin), I_{LK} = 10 μA			±45	V

Block Diagram



Test Circuit

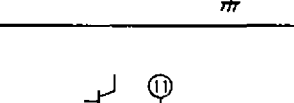
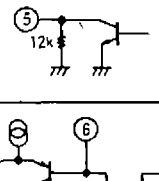
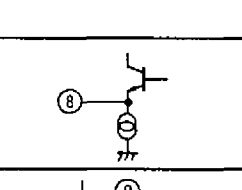
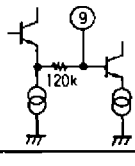
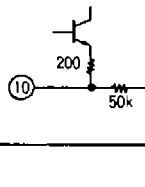
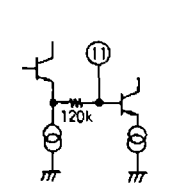
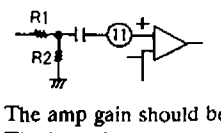
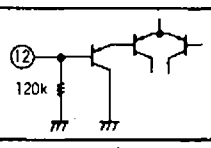
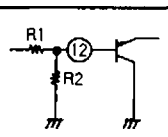
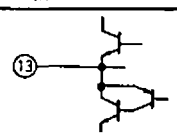


Unit (resistance : Ω, capacitance : F)

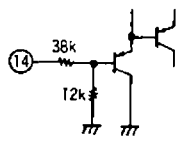
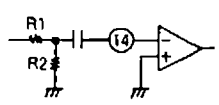
<Switch Setting Table>

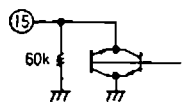
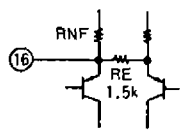
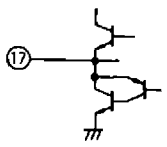
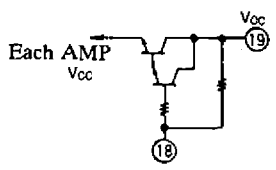
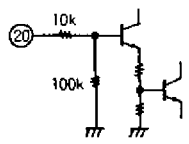
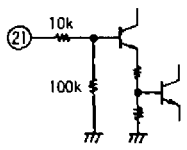
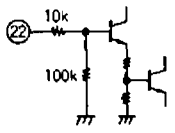
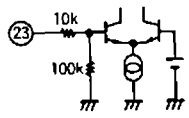
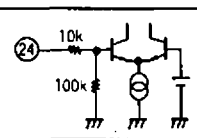
Parameter (Symbol)	SW1	SW2	SW3	SW4	SW5	V_M	V_P	V_R	Input	Measurement
I_{CCE}	2	1	1	2	1	GND	5V	GND	-	A
I_{CCP}	2	1	1	2	1	GND	GND	GND	-	A
I_{CCR}	2	1	1	2	1	GND	5V	5V	-	A
VG_{PB}	1	1	1	2	1	GND	GND	GND	$V_{IN}1$	V_O2
VG_{OE}	1	2	2	2	1	GND	GND	GND	$V_{IN}1$	V_O1
V_{NIE}	2	1	2	2	1	GND	GND	GND	-	V_O1
VG_{LP}, THD_L, V_{OML}	2	1	2	2	1	GND	GND	GND	$V_{IN}2$	V_O2
VG_{LR}	2	1	1	2	1	GND	5V	GND	$V_{IN}3$	V_O2
V_{NOL}	2	1	2	2	1	GND	5V	GND	-	V_O2
V_{OA}, ALC, THD_A	2	1	2	1	1	GND	5V	GND	$V_{IN}3$	V_O2
VG_{OR}	2	1	2	2	2	GND	5V	GND	$V_{IN}4$	V_O3
VG_{CR}, THD_R, V_{OMR}	2	1	2	2	1	GND	5V	GND	$V_{IN}4$	V_O3
M_P	1	1	1	2	1	5V	GND	GND	$V_{IN}1$	V_O2
M_R	2	1	1	2	1	5V	5V	GND	$V_{IN}4$	V_O3
M_E	2	1	2	2	1	5V	5V	GND	$V_{IN}2$	V_O2

Pin Functions

Pin No.	Function	Terminal Circuit	Description
1	Head Switch 1 (High voltage)		EE, PB: on; REC: off On resistance: 10 Ω, typ. With stand voltage during off: ±45 V (f = 80 kHz)
2	EQ AMP Input and Head Switch 2		Input playback signal to the head. Input impedance: 130 kΩ, typ. EE, REC: on; PB: off Switch on resistance: 5 Ω, typ.
3	GND		An exclusive GND for pin 1 head switch 1, EQ AMP and playback EP switch
4	EP Switch 1		Sets the tape head resonant frequency. On resistance: 15 Ω, typ. Input impedance: 120 kΩ, typ. (playback EP mode)
5	EP Switch 2		Increases the voltage gain at higher frequencies by reducing negative feedback amount of the PB EQ AMP. On resistance: 15 Ω, typ. Input impedance: 12 kΩ, typ. (playback EP mode)
6	EQ AMP NFB		Input of negative feedback of the EQ AMP to establish desired equalizing characteristics.
7	GND		Common return for all circuits except for EQ AMP and head switch 1.
8	EQ AMP Output		
9	LINE AMP PB Input		Input PB signal to the EQ AMP. The input impedance of pin 9 is high (120 kΩ) and requires a small coupling capacitor of 0.1 μF.
10	ALC FILTER		Connecting this pin to GND through a capacitor enables detection. The RC time constant sets attack recovery time.
11	LINE AMP Audio Input		Input EE, REC signal.  Select value of R_1 and R_2 so that the reference input is at the shoulder of the ALC. The amp gain should be set for 21.5 dB. The input impedance of pin 11 is high (120 kΩ) and requires a small coupling capacitor of 0.1 μF.
12	ALC Detect Input		 Accepts the output signal of LINE amp. The ALC level is determined by the voltage divider consisting of R_1 and R_2.
13	LINE AMP Output		Output impedance: 50 Ω, typ.

Unit (resistance : Ω)

<table>
<tr><th>Pin No.</th><th>Function</th><th>Terminal Circuit</th><th>Description</th></tr>
<tr><td>14</td><td>REC AMP Input</td><td> 
</td><td>Input recording signal from LINE AMP.
 

Input current is set by the divider consisting of R_1 and R_2.
Pin 14 requires no coupling capacitor since REC AMP is to operate at zero level and as inverting amp.</td></tr>
<tr><td>15</td><td>LP Switch</td><td> 
</td><td>Sets the high peaking point to the frequency suitable for LP.
On resistance: 15 Ω typ.
Input impedance: 60 kΩ typ.</td></tr>
<tr><td>16</td><td>REC AMP NFB</td><td> 
</td><td>Connecting an L, C, R network to this pin causes a peaking frequency to rise.</td></tr>
<tr><td>17</td><td>REC AMP Output</td><td> 
</td><td>Output impedance: 40 Ω typ.</td></tr>
<tr><td>18</td><td>Ripple Filter</td><td> 
</td><td>Connecting a electrolytic capacitor across this pin and GND smoothes ripples.</td></tr>
<tr><td>19</td><td>Supply Voltage (V_{CC})</td><td></td><td>V_{CC} = 15 V max
V_{CC} = 11.25 - 12.75 V typ.</td></tr>
<tr><td>20</td><td>LP Control</td><td> 
</td><td>Applying 3.5 V DC or more (6.0 V max.) to this pin turns on LP switch (pin 15). The switch turns off at 0.8 V or below.</td></tr>
<tr><td>21</td><td>EP Control</td><td> 
</td><td>Applying 3.5 V DC or more (6.0 V max.) to this pin turns on EP switch (pin 4,5) and LP switch (pin 15). The switches turn off at 0.8 V or below.</td></tr>
<tr><td>22</td><td>MUTE Control</td><td> 
</td><td>Applying 3.8 V DC or more (6.0 V max.) to this pin turns on mute circuit. The mute is disabled at 1.0 V or below.
[Control mode]
<table>
<tr><th rowspan="2">Mode</th><th colspan="2">MUTE "L"</th><th colspan="2">MUTE "H"</th></tr>
<tr><th>LINE AMP</th><th>REC AMP</th><th>LINE AMP</th><th>REC AMP</th></tr>
<tr><td>PB Mode</td><td>○</td><td>×</td><td>×</td><td>×</td></tr>
<tr><td>EE Mode</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
<tr><td>REC Mode</td><td>○</td><td>○</td><td>○</td><td>×</td></tr>
</table>
[O: Pass signal, x: Block signal]</td></tr>
<tr><td>23</td><td>PB Control</td><td> 
</td><td>Applying 3.3 V DC or more (6.0 V max.) to this pin enters EE mode and 1.0 V or below PB mode.</td></tr>
<tr><td>24</td><td>REC Control</td><td> 
</td><td>Applying 3.0 V DC or more (up to V_{CC}) to this pin enters REC mode and 1.0 V or below EE mode.</td></tr>
</table>

Unit (resistance : Ω)