BATTERY FEED

AN AT & T PRODUCT

- BASIC BATTERY FEED FUNCTION AT A LOW COST
- HIGH AC IMPEDANCE CHARACTERISTICS FOR BALANCED LINE, DIFFERENTIAL-MODE, VOICE-BAND SIGNALS
- FULL INTERNAL LIGHTNING SURGE PROTECTION UP TO 4 AMPS
- DC VOLTAGE DROPS CAN BE ADJUSTED TO ACCOMODATE DIFFERENT PEAK SIGNAL LEVELS

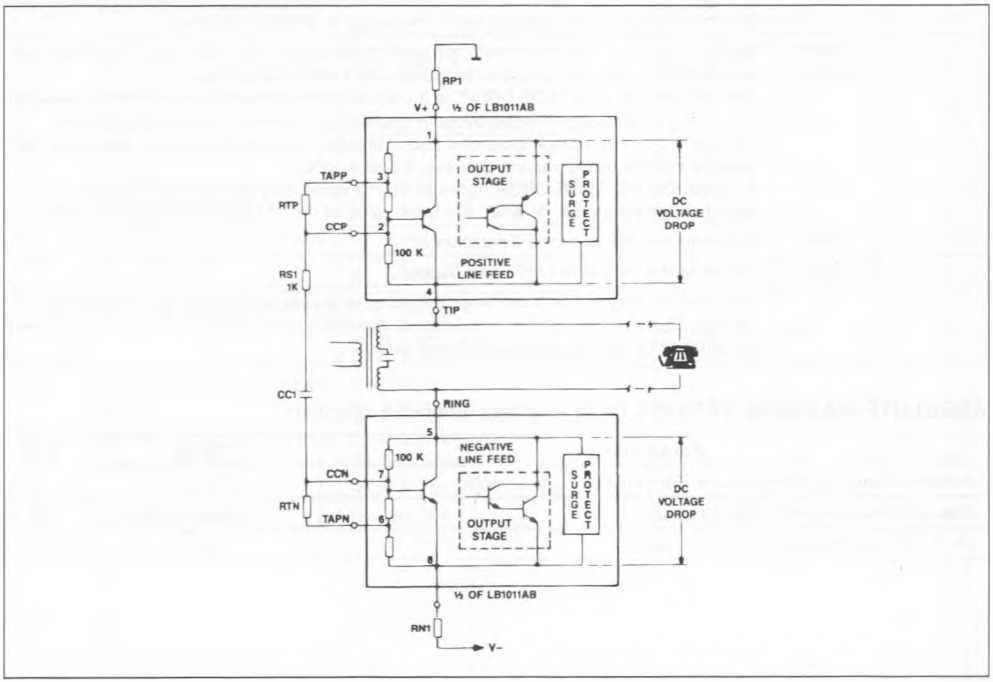
DESCRIPTION

The LB1011 is an electronic battery feed circuit which supplies DC currents to a telephone line with minimal loading on the AC signals. The LB1011 is integrated as two complementary chips to supply DC currents of both negative and positive polarities to either balanced or unbalanced lines. In the balanced line application, this device helps to suppress undesirable common-mode signals.

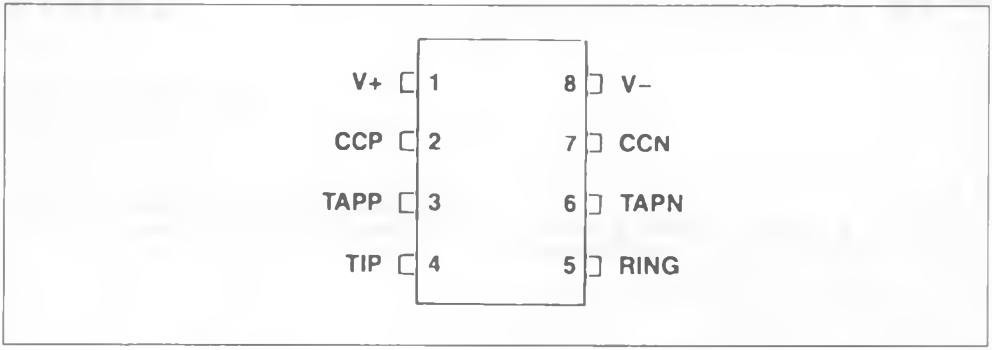
MINIDIP-A PLASTIC

ORDER CODE : LB1011AB

Figure 1 : Functional Diagram.



PIN CONNECTION



PIN DESCRIPTION

Pin	Name	Description
1	V+	This pin connects to the "most positive" external power supply (in some cases this is ground) through an external resistor. This external resistor is a factor in determining the amount of current which will be supplied by the "Positive Line Feed" output.
2 7	CCP CCN	"Cross-Coupling", Positive and Negative respectively. A capacitor between these two pins (for balanced line applications) creates a high AC impedance between TIP and RING. Since full Tip-to-ring voltage appears across these pins, it is recommended that a 1k ohm resistor be placed in series with the crosscoupling capacitor for surge protection purposes. Unbalanced line applications should connect the cross-coupling capacitor to ground so that the common-mode impedance of the output is greatly increased.
3 6	TAPP TAPN	Resistor tap pins. These terminals are used to adjust the "DC VOLTAGE DROP" across the "Positive Line Feed" and the "Negative Line Feed" respectively. The nominal "DC VOLTAGE DROP" is 3 volts when no resistors are connected between pins 2-to-3 or pins 6-to-7 respectively. A short circuit between these same pins will produce a nominal voltage drop of 4 volts. Resistors connected between these pins will produce voltage drops varying between 3 and 4 volts. A higher "DC VOLTAGE DROP" (greater than 3 volts) may be desirable for high operating temperatures, or when the peak value of the AC signals exceed 2.5 volts.
4	TIP	Output of the "Positive Line Feed Supply".
5	RING	Output of the "Negative Line Feed Supply".
8	V–	This pin connects to the "most negative" external power supply through an external resistor. This external resistor is a factor in determining the amount of current which will be supplied by the "Negative Line Feed" output.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	– 20 to + 70	°C
Storage Temperature Range	– 40 to + 125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C

ELECTRICAL CHARACTERISTICS : (T_A = 25°C unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC Voltage Drop. Positive Line Feed	I_{V+} = 50mA (See Fig. 3)	2.50		3.50	V
DC Voltage Drop. Positive Line Feed. High-level Mode	I_{V+} = 50mA TAPP shorted to CCP (See Fig. 4)	3.75		4.85	V
DC Voltage Drop. Negative Line Feed	I_{V-} = – 50mA (See Fig. 3)	– 2.50		– 3.50	V
DC Voltage Drop. Negative Line Feed. High-level Mode	I_{V-} = – 50mA TAPN shorted to CCN (See Fig. 4)	– 3.60		– 4.00	V
Shunt Impedance	(See Fig. 14)	18			KΩ
Common Mode (longitudinal) Rejection	V_{IN} = 1.0Vrms, f = 1kHz RP1 = RN1 (see fig. 5) (See Fig. 12)	45			dB
Common Mode (longitudinal) Rejection. High-Level Mode	TAP shorted to CC V_{IN} = 1.0Vrms, f = 1kHz (See Fig. 12) RP1 = RN1 (see fig. 5)	45			dB
Distortion	V(TIP to RING) = 1.0Vrms (See Fig. 13)			2.0	%
Distortion. High-Level-Mode	TAP shorted to CC (See Fig. 13) V(TIP to RING) = 2.0Vrms			2.0	%

TEST SPECIFICATION (T_A = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{BEP}	PNP Base-Emitter Voltage	I_{PNP} = 50mA (See Fig. 2)	– 2.0	– 1.0	V
ΔV_{BEP}	PNP Base-Emitter Voltage Change	(See Fig. 2) $\Delta V_{BEP} = V_{BEP}(100mA) - V_{BEP}(50mA)$	– 250	– 25	mV
V_{BEN}	NPN Base-Emitter Voltage	I_{NPN} = 50mA (See Fig. 2)	1.2	2.0	V
ΔV_{BEN}	PNP Base-Emitter Voltage Change	(See Fig. 2) $\Delta V_{BEN} = V_{BEN}(100mA) - V_{BEN}(50mA)$	+ 25	+ 250	mV
V_{CEP}	PNP Collector-Emitter Voltage	(See Fig. 3)	2.5	3.5	V
V_{CEN}	NPN Colletor-Emitter Voltage	(See Fig. 3)	– 3.5	– 2.5	V
V_{BF}	BF Total Volts	I_1 = 50mA S1, S2 open (See Fig. 4)	5.0	6.8	V
ΔV_{BF}	BF Total Voltage Difference	I_1 = 100mA S1, S2 open (See Fig. 4) $\Delta V_{BF} = V_{BF}(100mA) - V_{BF}(50mA)$	– 400	+ 600	mV
V_{BF}	BF Total Volts (High Level Mode)	I_1 = 50mA S1, S2 closed (See Fig. 4)	7.2	9.4	V
ΔV_{BF}	BF Total Voltage Difference (High Level Mode)	I_1 = 100mA S1, S2 closed (See Fig. 4) $\Delta V_{BF} = V_{BF}(100mA) - V_{BF}(50mA)$	– 400	+ 600	mV
V_F	Forward Voltage	I_T = 200mA (See Fig. 5)		1.4	V

TEST SPECIFICATION (Continued)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
VF	Forward Voltage	I_T = 200mA	(See Fig. 6)		1.4	V
		I_T = 75mA	(See Fig. 7)		1.4	
		I_T = 75mA	(See Fig. 8)		1.4	
		I_T = 75mA	(See Fig. 9)		1.4	
		I_T = 75mA	(See Fig. 10)		1.4	
V_{BO}	PNPN Breakdown Voltage	I_T = 35mA	(See Fig. 5)	– 10	– 8	
V_S	PNPN Sustain Voltage	I_T = 200mA S1 closed	(See Fig. 6)	– 5	– 2	
V_{BO}	PNPN Breakdown Voltage	I_T = – 35mA S1 closed	(See Fig. 6)	– 10	– 8	
V_S	PNPN Sustain Voltage	I_T – 200mA S1 closed	(See Fig. 6)	– 5	– 2	
Z_S	Shunt Impedance	S1, S2 open Z_S(in ohms) = 100/V_M(in volt)	(See Fig. 11)	18		KΩ
Z_S	Shunt Impedance	S1, S2 closed Z_S(in ohms) = 100/V_M(in volt)	(See Fig. 11)	18		KΩ
L_B	Longitudinal Balance	S1, S2 open L_B = Log[V_M/V_{IN}] (in dB)	(See Fig. 12)	– 45		dB
L_B	Longitudinal Balance	S1, S2 closed L_B = Log[V_M/V_{IN}] (in dB)	(See Fig. 12)	– 45		dB
T_{HD}	Distorsion Test	S1, S2 open V_{IN} = 1V rms	(See Fig. 13)		2	%
T_{HD}	Distorsion High	S1, S2 closed V_{IN} = 2V rms	(See Fig. 13)		2	%

TEST CIRCUITS

Figure 2.

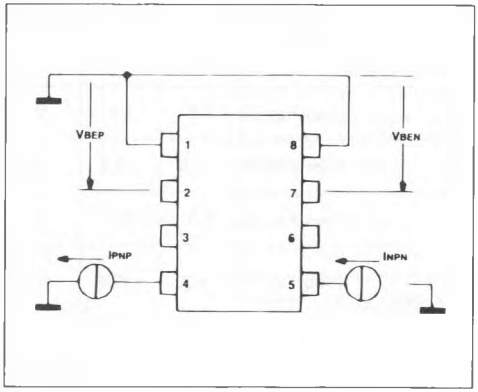


Figure 3.

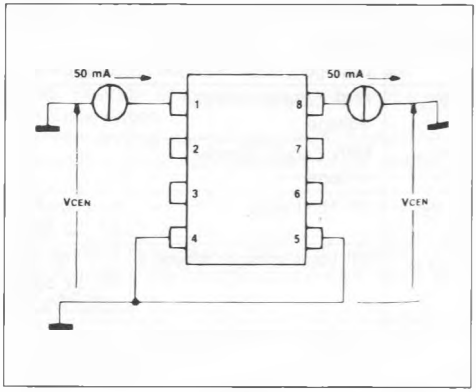


Figure 4 .

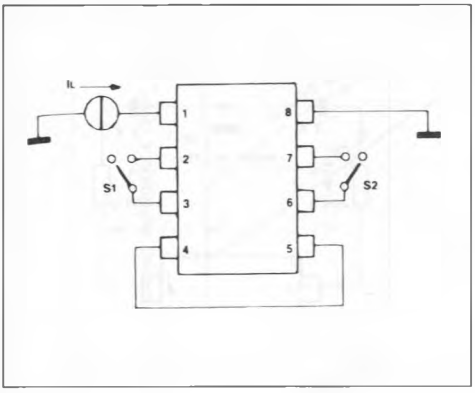
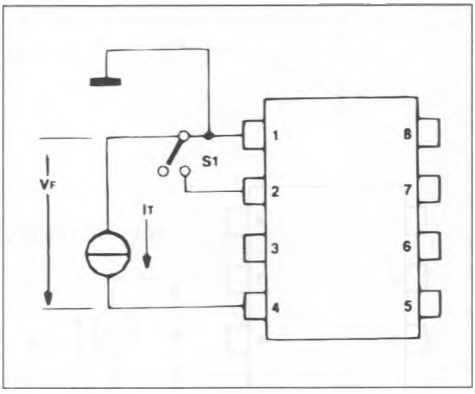


Figure 5.



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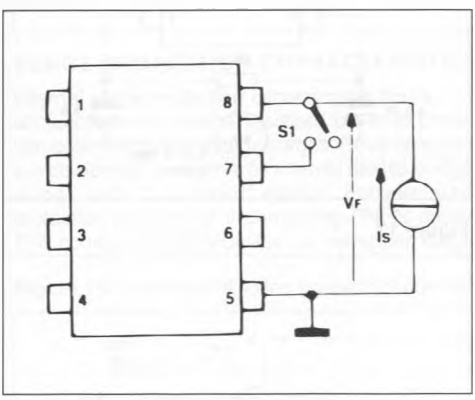


Figure 7.

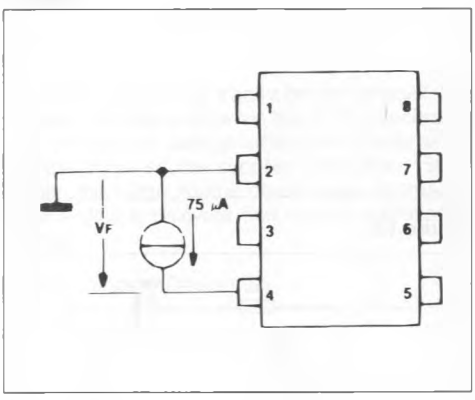


Figure 8.

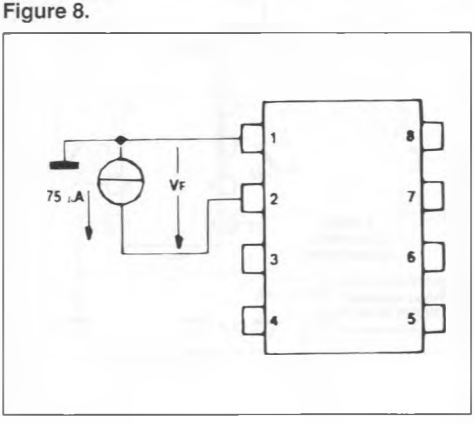


Figure 9.

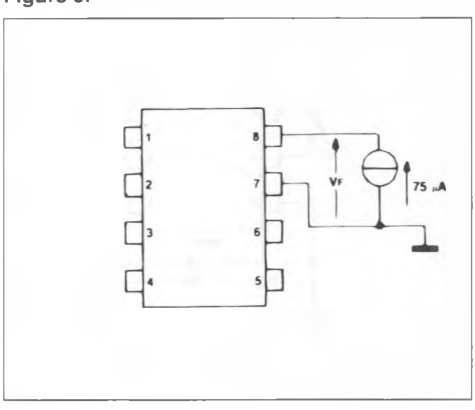


Figure 10.

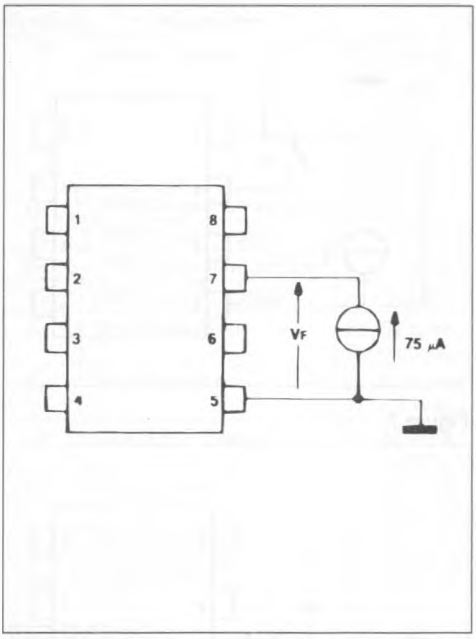


Figure 11.

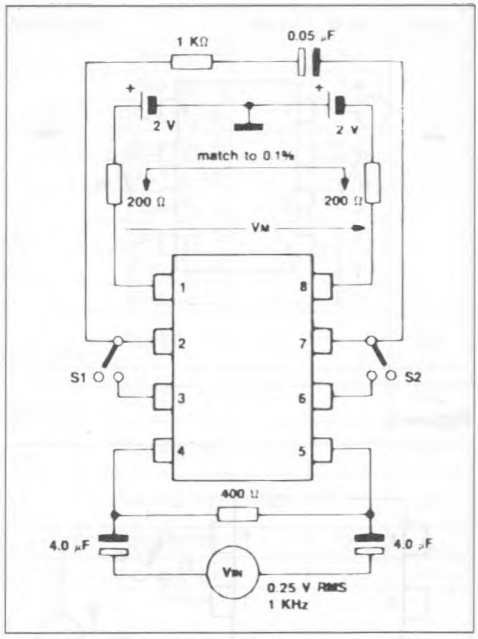


Figure 12.

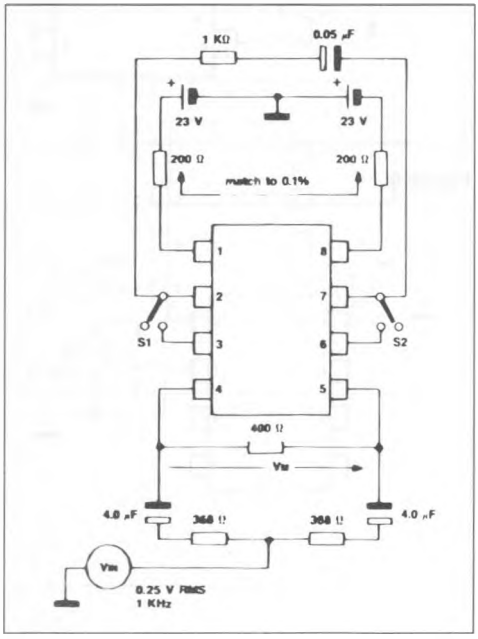


Figure 13.

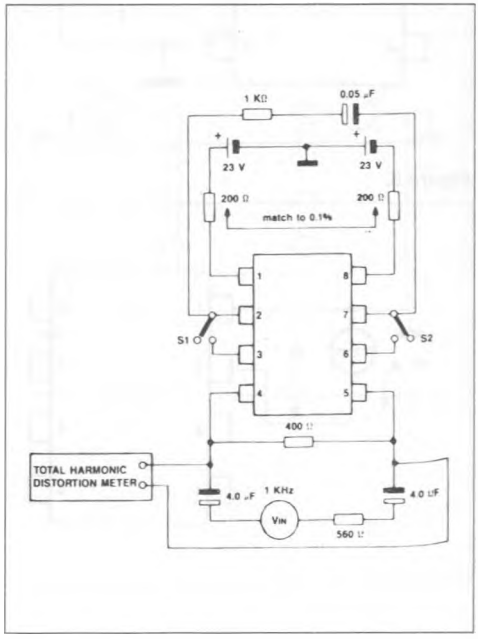
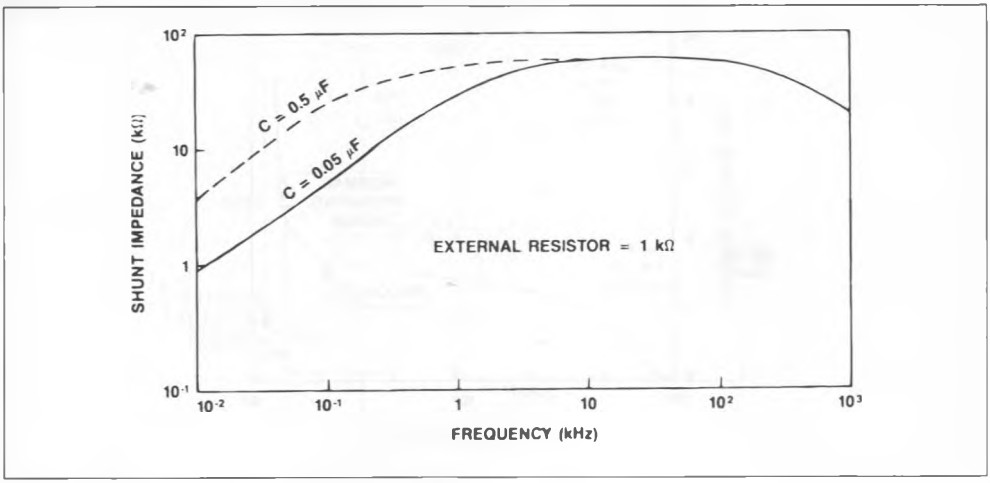


Figure 14.



SURGE PROTECTION CHARACTERISTICS

Internal surge protection circuitry (see figure 1) in conjunction with external resistors, provides protection against forward voltage surges. Reverse surges are dissipated through large internal diodes bridged across each "Line Feed" section. Forward surge protection consists of a composite PNPN device. This composite PNPN device can withstand surges as shown in figure 15. It has a breakover point (V_{BO}) of about 9 volts as shown in figure 16. After breakover, the output is clamped at less than 2 volts as long as the surge source supplies more than 150mA. When the surge source drops below 150mA, the PNPN device recovers and normal operation resumes.

Figure 15 : Maximum Applied Forward Surge Limits (PNPN Composite Device).

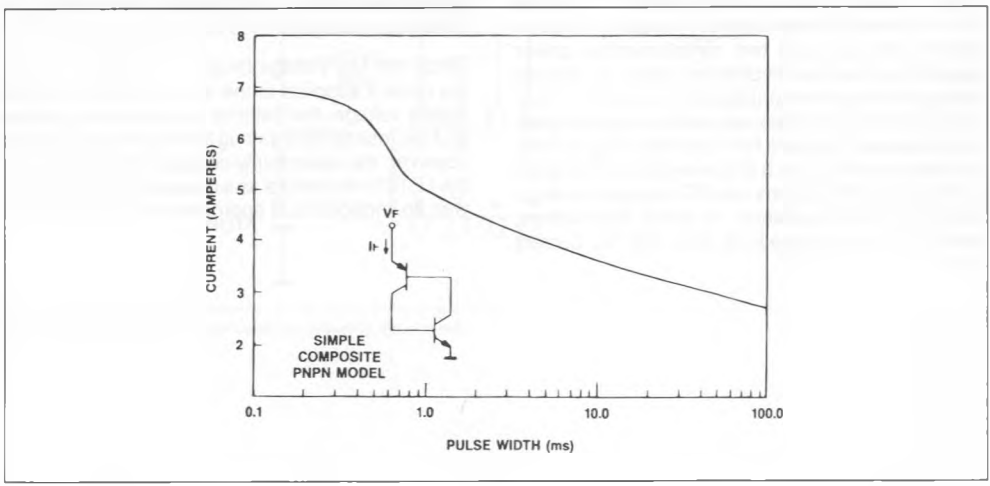
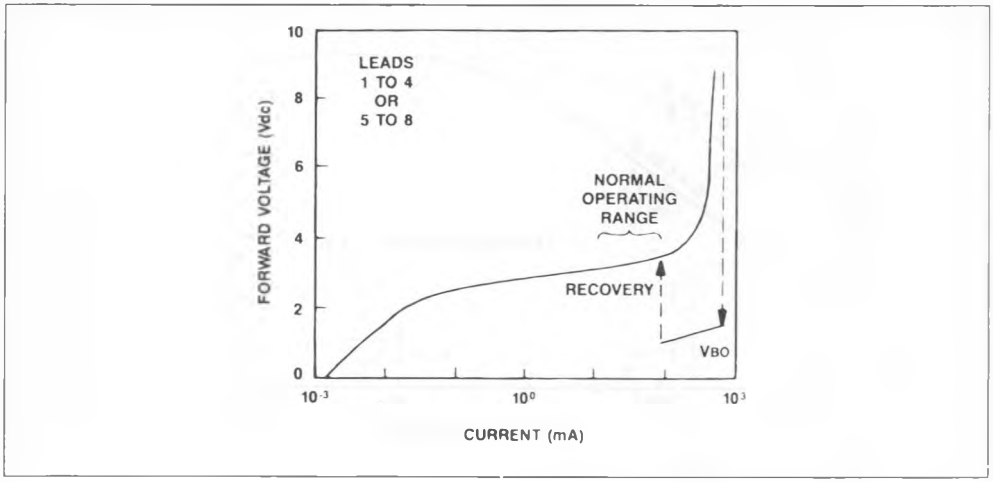


Figure 16 : Typical Voltage vs. Current (PNPN Composite).



APPLICATION

Figure 17 shows the LB1011 in a balanced line configuration. The complementary Positive and Negative Line Feeds are capacitively cross-coupled. Differential signals on the balanced line (TIP-RING) do not disturb the AC ground at the center of the cross-coupled connection. Therefore, both circuits act as constant current sources which present a high shunt impedance of approximately 50K ohms. The cross coupling does not affect feedback for either DC or common-mode signals. Therefore, for common-mode noise, the two complementary power supplies act as low impedance paths to ground through the resistors connected to V+ and V-. Common-mode rejection depends on the degree of matching between resistors RP1 and RN1. Figure 18 illustrates the LB1011 in a single-ended configuration in which it exhibits a very low DC impedance and a very high AC impedance. In some applications, where DC current needs to flow and AC Current should be blocked, this LB1011 configuration can replace an inductor. It does not, however, have the phase and amplitude vs frequency characteristics of a true inductor or RL network. The TAPP connection (pin 2) permits an external resistor (RTAP) to change the "DC Voltage Drop" (see figure 1). RTAP can be selected to raise the voltage from 3V (normal operating value) to as high as 4V. This voltage may be desirable for high operating temperature, or if the peak voltage of the AC signal exceeds 2.5V.

Since the "DC Voltage Drop" is relatively constant, the current supplied to the line is controlled by the supply voltage, the external resistor to the supply, and the resistance shunting the line. For AC signals, however, the capacitively-coupled "ground" causes the LB1011 to operate as a constant-current source with an impedance of approximately 25 Kohms.

Figure 17 : LB1011 Battery Feed Application Diagram (Balanced Configuration).

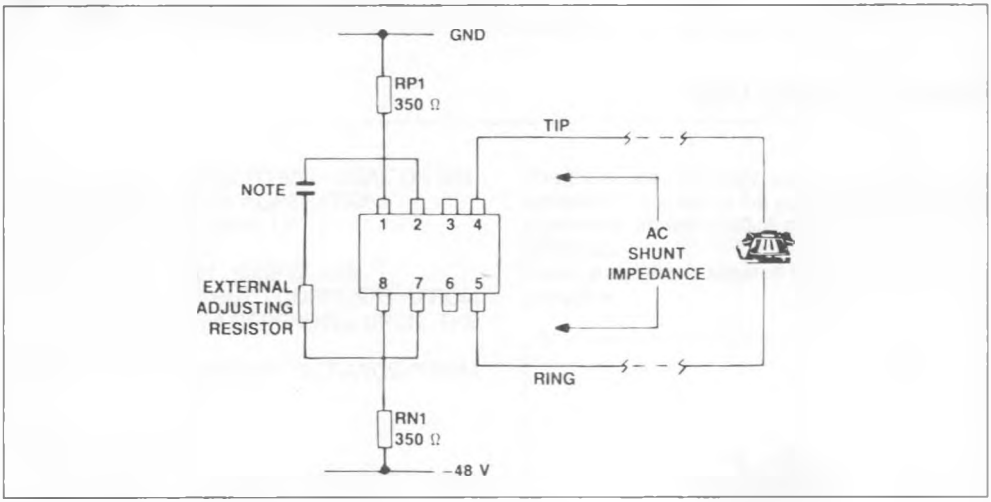
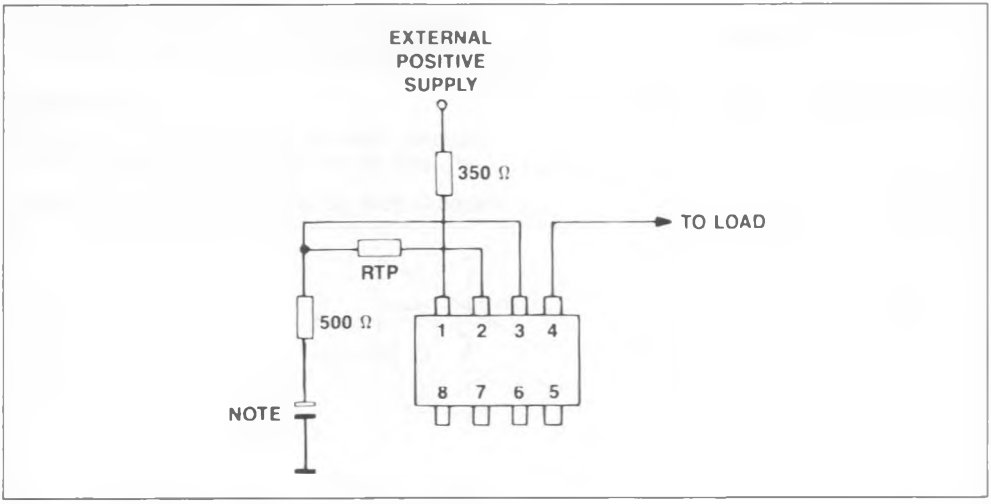


Figure 18 : LB1011 AC Blocking, DC Current Feed Application.



Note : 1. Value of capacitor selected based on frequency requirements