Ordering number:EN1571B

Monolithic Digital IC

LB1649

Dual Bidirectional Motor Driver

Overview

The LB1649 is a dual bidirectional motor driver. Since each channel has a 2-input logic circuit and performs bidirectional driving and braking functions, it is capable of direct driving 2pcs. of motor of various types rated at 6 to 24V.

The output voltage can be varied by using external zener diodes.

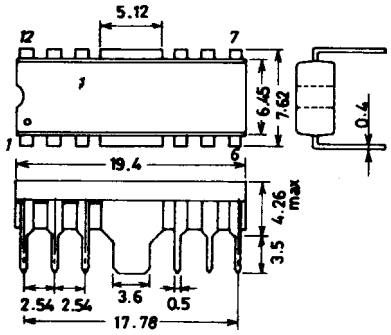
It is especially suited for dual motor drive (reel motor, loading motor, cassette motor in VCR) and for stepping motor drive.

Package Dimensions

unit:mm

3022A-DIP12F

[LB1649]



SANYO : DIP12F

Features

- With power transistor for motor drive contained, capable of withstanding dash current of 1A max.
- Performs braking function at the motor stop mode.
- Contains elements to absorb motor dash current.
- Input connectable dirct to MOS LSI.
- Minimun number of external parts required.
- Wide operating voltage range.

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		25	V
Input voltage	V_{IN}		25	V
Output current	I_O		±1	A
Allowable power dissipation	Pd max		1.9	W
Operating temperature	Topr		–25 to +75	˚C
Storage temperature	Tstg		–55 to +125	˚C

Allowable Operating Conditions at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		7 to +25	V

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquaters

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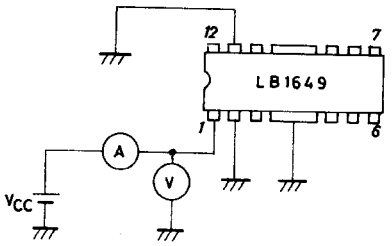
Electrical Characteristics at Ta = 25°C, V_{CC}=12V, per channel

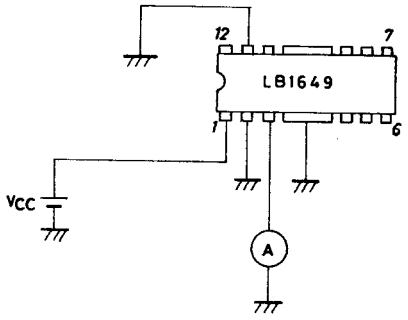
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	Braking mode, R_L=∞, per channel		7.0	10.0	mA
Output leakage current	I_{OL}	Braking mode, R_L=∞, per channel		40	120	μA
Input threshold voltage	V_{th}	R_L=∞	0.9	1.05	1.20	V
Output voltage	V_O	R_L=60Ω, V_Z=7.4V	6.5	7.2	7.5	V
Output transistor saturation voltage (upper)	V_{sat1}	I_{OUT}=300mA		1.9	2.3	V
		I_{OUT}=500mA		2.0	2.4	V
Output transistor saturation voltage (lower)	V_{sat2}	I_{OUT}=300mA		0.3	0.55	V
		I_{OUT}=500mA		0.5	0.7	V

Test Circuit (per channel)

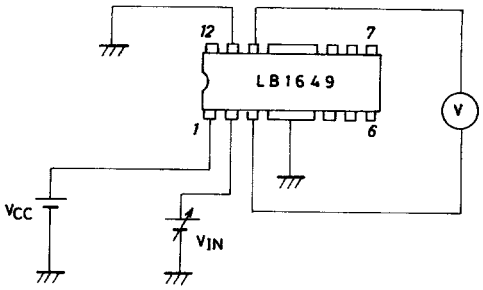
(1) I_{CC}



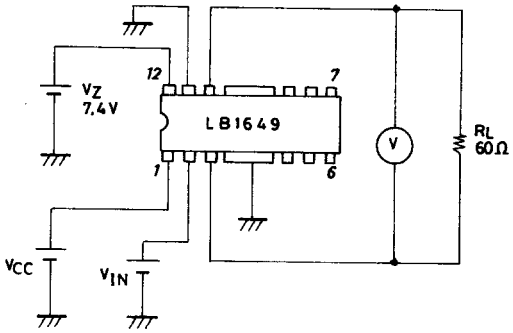
(2) I_{OL}



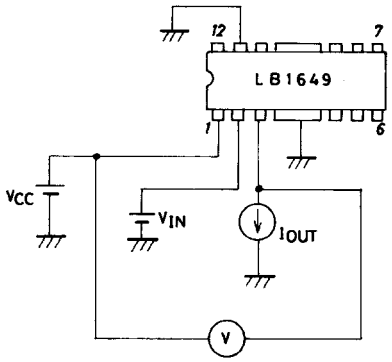
(3) V_{th}



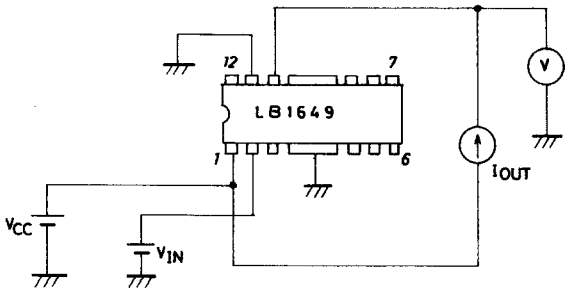
(4) V_O



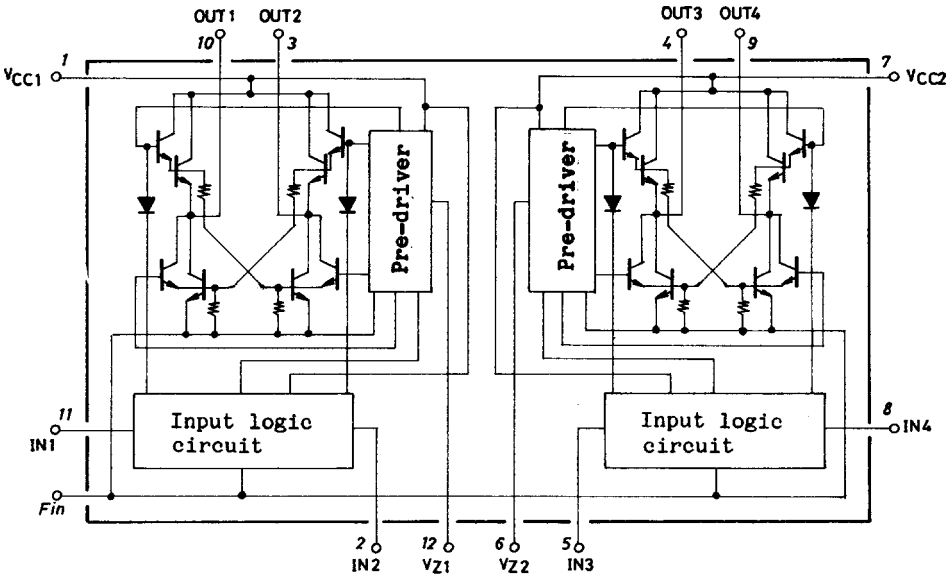
(5) V_{sat1}



(6) V_{sat2}



Equivalent Circuit Block Diagram



Truth Table of Logic Circuit

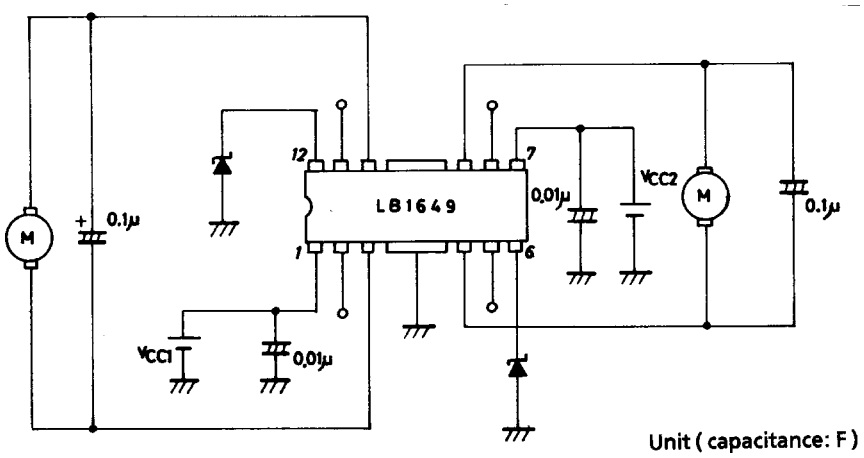
IN1	IN2	OUT1	OUT2	IN3	IN4	OUT3	OUT4
0	0	L	L	0	0	L	L
1	0	H	L	1	0	H	L
0	1	L	H	0	1	L	H
1	1	L	L	1	1	L	L

Note : A capacitor of 0.01μF or greater must be connected across V_{CC}1,2 and GND.

INPUT			OUTPUT				MODE	
IN1	IN2, 3	IN4	OUT1	OUT2	OUT3	OUT4	M1	M2
0	0	0	L	L	L	L	Brake	Brake
1	0	0	H	L	L	L	Forward/reverse	Brake
0	1	1	L	H	L	L	Reverse/forward	Brake
1	1	0	L	L	H	L	Brake	Forward/reverse
0	0	1	L	L	L	H	Brake	Reverse/forward
1	1	1	L	L	L	L	Brake	Brake

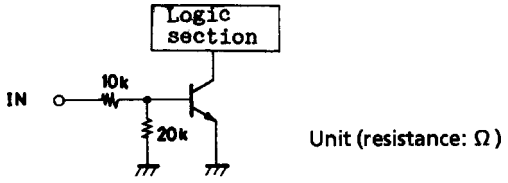
The remaining input states 1, 0, 1 and 0, 1, 0 are not inhibinted.

Sample Application Circuit



Input Circuit

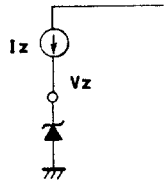
The input circuit is shown right



V_Z pin

Zener voltage	VZ pin voltage vaule
≥5.6V	small
<5.6V	large*

* Susceptible to V_Z pin flow-out current change.



I_Z----V_Z flow-out current