

**SANYO****LB1817W****FDD Spindle Motor Driver****Overview**

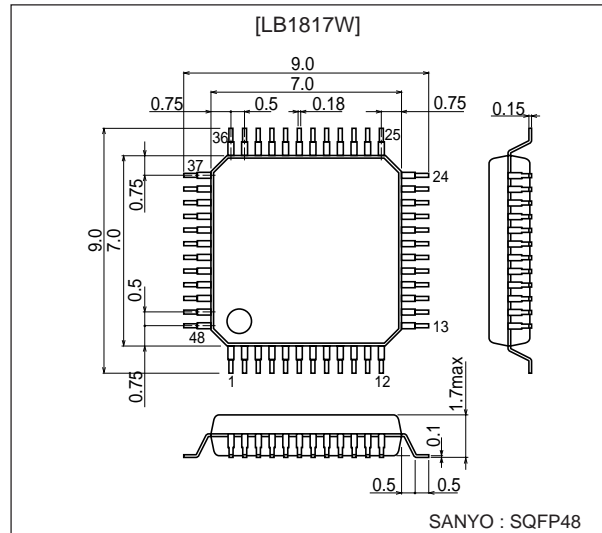
The LB1817W is a spindle motor driver for low-profile floppy disk drives.

**Functions and Features**

- Three-phase full-wave linear drive (with external PNP transistor)
- Low saturation voltage
- Built-in digital speed control
- Start/stop circuit (Low active)
- Switchable rotation speed
- Current limiter circuit
- Built-in index processing circuit
- Index timing adjustable by VR
- AGC circuit
- Thermal protection circuit

**Package Dimensions**

unit: mm

**3163A-SQFP48****Specifications****Absolute Maximum Ratings at Ta = 25°C**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		7.0	V
Maximum output current	$I_{CC}$ max1	$t \leq 0.5s$	1.5	A
Maximum constant output current	$I_O$ max2		1.0	A
Allowable power dissipation	$P_d$ max1	IC only	0.45	W
Operating temperature	$T_{opr}$		-20 to +80	°C
Storage temperature	$T_{stg}$		-40 to +150	°C

**Allowable Operating Ranges at Ta = 25°C**

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	$V_{CC}$		4.2 to 6.5	V

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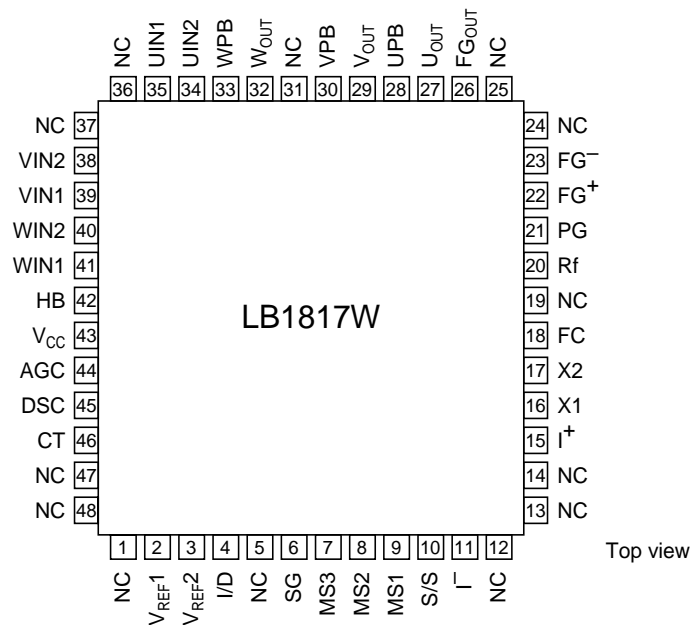
**Electrical Characteristics at Ta = 25°C, V<sub>CC</sub> = 5V**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I <sub>CCO</sub>	S/S = 5V (Standby)		70	100	μA
	I <sub>CC</sub>	S/S = 0V (Normal)		25	35	mA
MS1 bias current	I <sub>MS1</sub>	V <sub>MS1</sub> = 5V		180	270	μA
MS1 Low input voltage	V <sub>MS1L</sub>		0.0		0.8	V
MS1 High input voltage	V <sub>MS1H</sub>		2		V <sub>CC</sub>	V
MS2 bias current	I <sub>MS2</sub>	V <sub>MS2</sub> = 5V		90	135	μA
MS2 Low input voltage	V <sub>MS2L</sub>		0.0		0.8	V
MS2 High input voltage	V <sub>MS2H</sub>		2		V <sub>CC</sub>	V
MS3 bias current	I <sub>MS3</sub>	V <sub>MS3</sub> = 5V		90	135	μA
MS3 Low input voltage	V <sub>MS3L</sub>		0.0		0.8	V
MS3 High input voltage	V <sub>MS3H</sub>		2		V <sub>CC</sub>	V
S/S bias current	I <sub>S/S</sub>				20	μA
S/S Low voltage	V <sub>S/SL</sub>		0.0		0.8	V
S/S High voltage	V <sub>S/SH</sub>		2		V <sub>CC</sub>	V
Hall amplifier input bias current	I <sub>HB</sub>				15	μA
Common mode input voltage range	V <sub>H</sub>		2.0		V <sub>CC</sub> -0.7	V
Differential input voltage range	V <sub>dif</sub>		50		200	mVp-p
Input offset voltage	V <sub>ho</sub>	*			±10	mV
Hall bias output voltage	V <sub>H</sub>	I <sub>H</sub> = 5 mA	0.5	0.8	1.1	V
Leakage current	V <sub>HL</sub>	S/S = 5V			±10	μA
Output saturation voltage	V(sat)	I <sub>O</sub> = 0.8A		0.45	0.64	V
Output leakage current	I <sub>OL</sub>				1	mA
Current limiter	I <sub>lim</sub>	R <sub>F</sub> = 3 kΩ, R <sub>OUT</sub> = 100Ω	6.3	7.5	8.7	mA
Control amplifier voltage gain	G <sub>C</sub>		-7.5	-5.5	-3.5	dB
Voltage gain phase differential	ΔG <sub>C</sub>				±1	dB
V/I conversion source current	I <sup>+</sup>		19	28	37	μA
V/I conversion sink current	I <sup>-</sup>		-19	-28	-37	μA
V/I conversion current ratio	I <sup>+</sup> /I <sup>-</sup>		0.8	1.0	1.2	
DSC buffer input current	I <sub>DSC</sub>				1	μA
FG amplifier input voltage	V <sub>FG</sub>	f <sub>FG</sub> = 300 Hz	2		20	mVp-p
FG amplifier voltage gain	G <sub>FG</sub>	Open loop*		60		dB
FG amplifier input offset	V <sub>FGO</sub>	*			±10	mV
FG amplifier internal reference voltage	V <sub>FGB</sub>		2.2	2.5	2.8	V
FG Schmitt hysteresis width	ΔV <sub>sh1</sub>	High → Low*		25		mV
	ΔV <sub>sh2</sub>	Low → High*		25		mV
Speed discriminator count	N			1390/2		
Discriminator operating frequency	F <sub>D</sub>	*			1.1	MHz
Oscillator frequency	F <sub>OSC</sub>	*			1.1	MHz
Oscillator frequency tolerance	ΔF <sub>OSC</sub>				±0.2	%
Index output Low voltage	V <sub>IDL</sub>	I <sub>O</sub> = 2 mA			0.4	V
Index output leakage current	I <sub>IDL</sub>				±10	μA
Index amplifier common mode input voltage range	V <sub>I</sub>		0.2		V <sub>CC</sub> -0.7	V
Index amplifier differential input voltage range	V <sub>DIF</sub>	Hysteresis width < 25 mA	25		100	mV
Index amplifier hysteresis set current	I <sub>HYS</sub>		2.9	4.2	5.5	μA
Timing adjustment at High level	V <sub>TH</sub>	MS1 = L	1.15	1.26	1.35	V
Timing adjustment at Low level	V <sub>TL</sub>	MS1 = L	0.40	0.52	0.60	V
Timing adjustment ratio	T <sub>HL</sub>	V <sub>TH</sub> (MS1 = L) / V <sub>TH</sub> (MS1 = H)		1.148		
Reference voltage	V <sub>REF1</sub>		2.20	2.50	2.80	V
	V <sub>REF2</sub>		1.85	2.15	2.45	V
Thermal protection operating temperature	TSD	*	150	180		°C
Hysteresis width	ΔTSD	*		10		°C

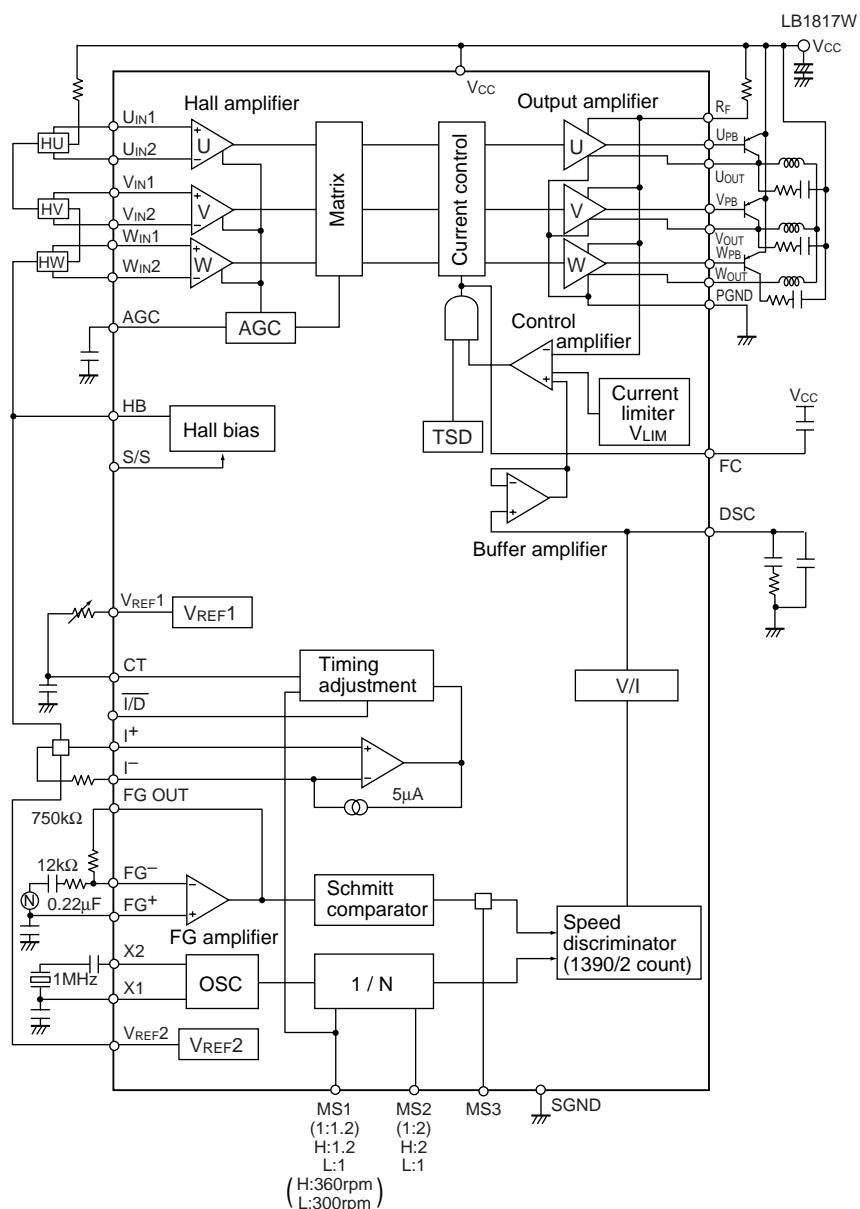
Note: Items shown to be "\*" are not measured.

# LB1817W

## Pin Assignment



## Block Diagram



# Pin Descriptions

Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
1, 5 12, 13 14, 19 24, 25 31, 36 37, 47 48	NC			<ul style="list-style-type: none"> <li>Pins not used</li> </ul>
2	V <sub>REF1</sub>	2.5V typ		<ul style="list-style-type: none"> <li>V<sub>REF1</sub> pin. Used as power supply for external CR serving for index timing adjustment.</li> </ul>
3	V <sub>REF2</sub>	2.15V typ		<ul style="list-style-type: none"> <li>V<sub>REF2</sub> pin. Used as bias pin for external index sensor.</li> </ul>
4	I/D			<ul style="list-style-type: none"> <li>Index pulse output pin.</li> </ul>
6	SG			<ul style="list-style-type: none"> <li>Signal ground pin. Connect to ground together with pin 21.</li> </ul>
7	MS3	H: 2.0V min L: 0.8V max		<ul style="list-style-type: none"> <li>FG switching pin. High: FG set to through Low: FG set to 1-stage division</li> </ul>
8	MS2	H: 2.0V min L: 0.8V max		<ul style="list-style-type: none"> <li>CLK switching pin. High: Clock set to through Low: Clock set to 1-stage division</li> </ul>

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
9	MS1	H: 2.0V min L: 0.8V max		<ul style="list-style-type: none"> <li>Rotation speed switching pin.</li> <li>High: 360 rpm</li> <li>Low: 300 rpm</li> <li>For details, see rotation speed switching table.</li> </ul>
10	S/S	H: 2.0V min L: 0.8V max		<ul style="list-style-type: none"> <li>Start/stop switching pin.</li> <li>Low: active</li> </ul>
11 15	I <sup>-</sup> I <sup>+</sup>			<ul style="list-style-type: none"> <li>External index – input pin.</li> <li>External index + input pin.</li> <li>When I<sup>-</sup> pin is High, constant current I<sub>1</sub> flows. When pin is Low, constant current I<sub>1</sub> is cut off.</li> <li>Resistor externally connected to I<sup>-</sup> pin determines hysteresis width.</li> </ul>
16	X1			<ul style="list-style-type: none"> <li>Reference clock generator pin.</li> </ul>
17	X2			
18	FC			<ul style="list-style-type: none"> <li>Frequency characteristics compensation pin.</li> <li>To prevent current control loop oscillation, insert a capacitor between this pin and V<sub>CC</sub>.</li> </ul>

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
20	RF			<ul style="list-style-type: none"> <li>Output current detection pin.</li> <li>To detect output current as a voltage, insert a resistor <math>R_f</math> between this pin and <math>V_{CC}</math>. The voltage is used for the current limiter. The detection level is about 1/50 of the output current.</li> </ul>
21	PG			<ul style="list-style-type: none"> <li>Output transistor ground pin.</li> <li>Connect to ground together with pin 6.</li> </ul>
22 23	FG <sup>+</sup> FG <sup>-</sup>	2.5V typ		<ul style="list-style-type: none"> <li>FG amplifier + pin</li> <li>FG amplifier – pin</li> </ul>
26	FGout			<ul style="list-style-type: none"> <li>FG amplifier output pin.</li> </ul>
27 28 29 30 32 33	U <sub>OUT</sub> U <sub>PB</sub> V <sub>OUT</sub> V <sub>PB</sub> W <sub>OUT</sub> W <sub>PB</sub>			<ul style="list-style-type: none"> <li>U phase output pin.</li> <li>U phase external PNP transistor base connection.</li> <li>V phase output pin.</li> <li>V phase external PNP transistor base connection.</li> <li>W phase output pin.</li> <li>W phase external PNP transistor base connection.</li> </ul>
34 35 38 39 40 41	U <sub>IN2</sub> U <sub>IN1</sub> V <sub>IN2</sub> V <sub>IN1</sub> W <sub>IN2</sub> W <sub>IN1</sub>			<ul style="list-style-type: none"> <li>U phase Hall input pin.</li> <li>Logic High means <math>U_{IN1} &gt; U_{IN2}</math>.</li> <li>V phase Hall input pin.</li> <li>Logic High means <math>V_{IN1} &gt; V_{IN2}</math>.</li> <li>W phase Hall input pin.</li> <li>Logic High means <math>W_{IN1} &gt; W_{IN2}</math>.</li> </ul>

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
42	HB			<ul style="list-style-type: none"> <li>Hall bias negative-side pin. In stop mode, the pin is open and Hall bias is cut off.</li> </ul>
43	V <sub>CC</sub>			<ul style="list-style-type: none"> <li>Power supply pin. The voltage supplied to this pin must be stabilized to prevent ripple noise or other noises from inputting to this pin.</li> </ul>
44	AGC			<ul style="list-style-type: none"> <li>AGC pin. Controls the Hall amplifier gain according to Hall input amplitude. An external capacitor is used.</li> </ul>
45	DSC			<ul style="list-style-type: none"> <li>Speed discriminator pin.</li> </ul>
46	CT			<ul style="list-style-type: none"> <li>Timing adjustment pin. External CR for time constant circuit is connected here.</li> </ul>

Truth Table

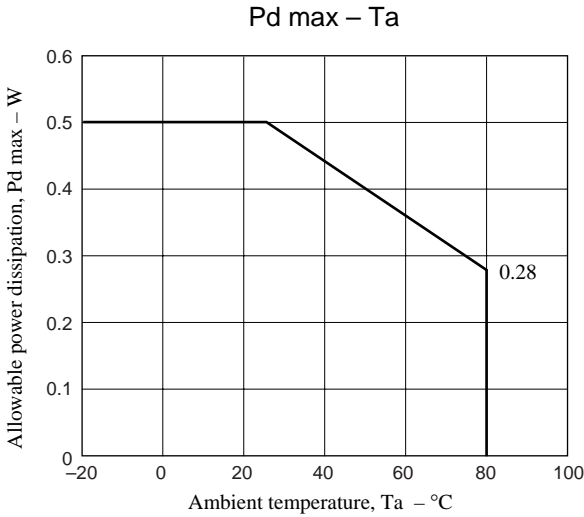
	Source → Sink	Hall input		
		U	V	W
1	V phase → W phase	H	H	L
2	V phase → U phase	L	H	L
3	W phase → U phase	L	H	H
4	W phase → V phase	L	L	H
5	U phase → V phase	H	L	H
6	U phase → W phase	H	L	L

Hall input pin High means  $U_{IN1} > U_{IN2}$   
 $V_{IN1} > V_{IN2}$   
 $W_{IN1} > W_{IN2}$

Rotation Speed Select Table

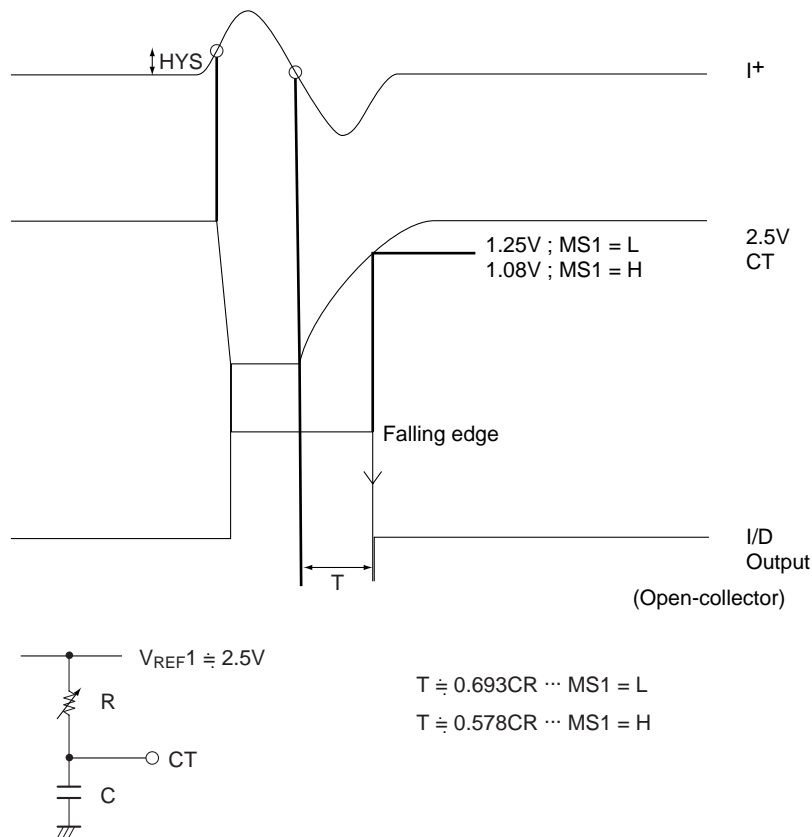
$f_{OSC} = 1\text{ MHz}$

MS1	H	L	H	L	H	L	H	L
MS2	H		L		H		L	
MS3	H		L		L		H	
$f_{FG} [\text{Hz}]$	720	600	720	600	1440	1200	360	300





## Index and Timing Chart



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