

Ordering number: EN 4945

Monolithic Digital IC

SANYO

No. 4945

LB1893

3-Phase Brushless Motor Driver for CD-ROM Spindle Motors

Overview

The LB1893 is a 3-phase brushless motor driver for use in CD-ROM spindle motors.

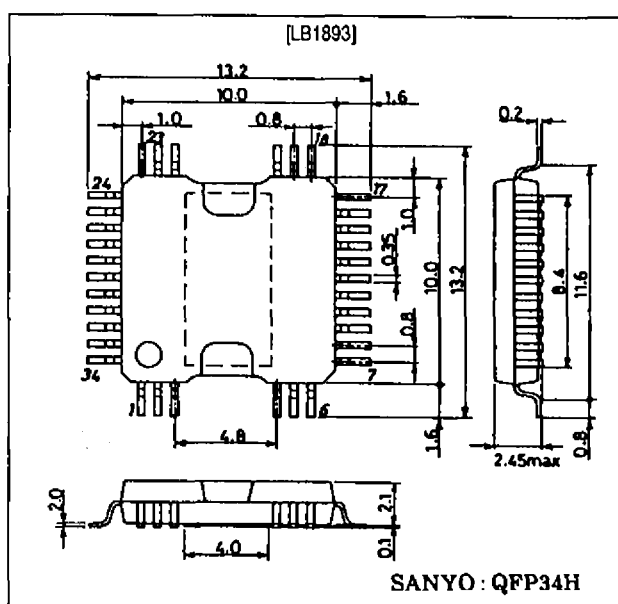
Functions and Features

- 120° voltage linear type
- V-type control voltage
- Switchable control gain
- Control, non-feedback, and speed increment/decrement control pin built-in
- Start/Stop pin built-in
- Hall device bias built-in

Package Dimensions

Unit: mm

3206-QFP34H



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51695TH (ID) No. 4945—1/8

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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------------------|-----------------------|--|-----------------|------------------|
| Maximum supply voltage | $V_{CC1 \text{ max}}$ | | 20 | V |
| | $V_{CC2 \text{ max}}$ | | 7.0 | V |
| Output transistor blocking voltage | $V_{O(sus)}$ | $I_{OUT} = 20\text{mA}$, design value | 20 | V |
| Output supply voltage | $V_{OU, v, w}$ | | 20 | V |
| Output current | I_{OUT} | | 1.2 | A |
| Allowable power dissipation | $P_d \text{ max}$ | Unmounted IC | 0.77 | W |
| Operating temperature | T_{opr} | | -20 to $+75$ | $^\circ\text{C}$ |
| Storage temperature | T_{slg} | | -55 to $+150$ | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------------|------------|------------------------|------------------------|------|
| Supply voltage | V_{CC1} | | 5 to 18 | V |
| | V_{CC2} | $V_{CC1} \geq V_{CC2}$ | 4.3 to 6.5 | V |
| V_{Cref} pin input voltage | V_{Cref} | | $V_{CC2}/2 \pm 1.0$ | V |
| V_{NS} pin input voltage | V_{NS} | | 0 to $V_{CC2}/2 - 1.0$ | V |

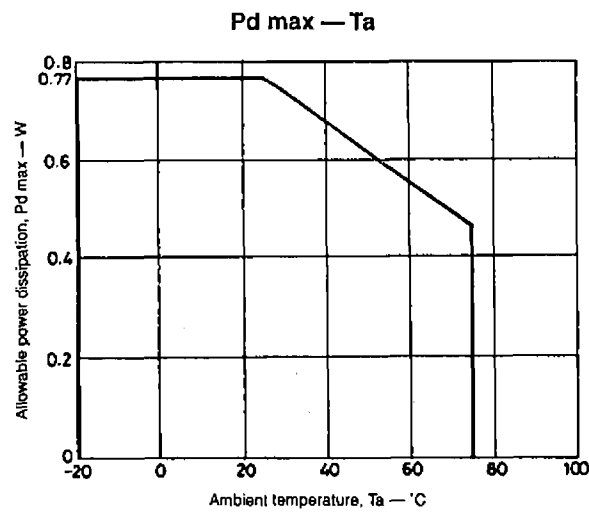
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC1} = 12\text{V}$, $V_{CC2} = 5\text{V}$, specified test circuit

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|------------------------|---|----------|----------|----------|---------------|
| | | | min | typ | max | |
| Supply current 1 | I_{CC1} | $V_C = \text{open}$, $V_{Cref} = \text{open}$, $R_L = \infty$, $V_{S/S} = 5\text{V}$ | – | 17 | 30 | mA |
| Supply current 2 | I_{CC2} | $V_C = \text{open}$, $V_{Cref} = \text{open}$ | – | 7.5 | 10.5 | mA |
| Supply current 3 | I_{CC3} | $V_C = \text{open}$, $V_{Cref} = \text{open}$, $R_L = \infty$, $V_{S/S} = 0\text{V}$ | – | 0.9 | 3 | mA |
| Output saturation voltage | $V_{O(sat)1}$ | $I_{OUT} = 0.4\text{A}$, sink + source | – | 1.6 | 2.2 | V |
| | $V_{O(sat)2}$ | $I_{OUT} = 0.8\text{A}$, sink + source | – | 2.0 | 3.0 | V |
| Output center voltage | V_{OQ} | $V_C = 2.5\text{V}$, $V_{Cref} = 2.5\text{V}$ | 5.7 | 6.0 | 6.3 | V |
| Hall amplifier input offset voltage | $V_{H \text{ offset}}$ | | –5 | – | +5 | mV |
| Hall amplifier input bias current | $I_{H \text{ bias}}$ | | – | 1 | 5 | μA |
| Hall amplifier common-mode input voltage range | V_{Hch} | | 1.3 | – | 2.2 | V |
| Hall amplifier input-output voltage gain | G_{VHO} | | 40 | 43 | 46 | dB |
| Control-output drive gain 1 | G_{VCO1} | $RZ1 = RZ2$, $GC1 = \text{LOW}$, $GC2 = \text{LOW}$ | 26 | 29 | – | dB |
| Control-output channel difference 1 | ΔG_{VCO1} | $RZ1 = RZ2$, $GC1 = \text{LOW}$, $GC2 = \text{LOW}$ | –1.5 | – | +1.5 | dB |
| Control-output drive gain 2 | G_{VCO2} | $RZ1 = RZ2$, $GC1 = \text{LOW}$, $GC2 = \text{HIGH}$ | 32 | 35 | – | dB |
| Control-output channel difference 2 | ΔG_{VCO2} | $RZ1 = RZ2$, $GC1 = \text{LOW}$, $GC2 = \text{HIGH}$ | –1.9 | – | +1.9 | dB |
| Input dead-zone voltage | V_{DZ} | $RZ1 = RZ2$, $GC1 = \text{LOW}$, $GC2 = \text{LOW}$ | ± 13 | ± 38 | ± 55 | mV |
| Input bias current 1 | $I_{B \text{ SERVO}}$ | $V_C = 1.0\text{V}$ | – | – | 500 | nA |
| Input bias current 2 | $I_{B \text{ NS}}$ | $V_{NS} = 1.0\text{V}$ | – | – | 500 | nA |

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| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|----------------|---|---------|------|-----|-------------|
| | | | min | typ | max | |
| S/S pin HIGH-level voltage | $V_{S/S\ H}$ | CMOS-level input. | 4.0 | — | — | V |
| S/S pin LOW-level voltage | $V_{S/S\ L}$ | S/S pin threshold $V_{th} = V_{CC}/2$ | — | — | 1.0 | V |
| Gain control 1 HIGH-level voltage | $V_{GC1\ H}$ | CMOS-level input. | 4.0 | — | — | V |
| Gain control 1 LOW-level voltage | $V_{GC1\ L}$ | GC1 pin threshold $V_{th} = 2.0V$ | — | — | 1.0 | V |
| Gain control 2 HIGH-level voltage | $V_{GC2\ H}$ | CMOS-level input. | 4.0 | — | — | V |
| Gain control 2 LOW-level voltage | $V_{GC2\ L}$ | GC2 pin threshold $V_{th} = 2.0V$ | — | — | 1.0 | V |
| S/S pin input current | $I_{S/S}$ | 5V input voltage | — | 50 | 100 | μA |
| Gain controls 1 and 2 current | I_{GC} | 5V input voltage | — | 53 | 110 | μA |
| Motor output saturation voltage | $V_{(sat)HFG}$ | $I_O = -5mA$ | — | 0.24 | 0.5 | V |
| Motor output saturation blocking voltage | $V_{(sus)HFG}$ | Design value | — | — | 7 | V |
| Hall bias voltage | $V_{H\pm}$ | $I_O = 5mA$, $R_H = 200\Omega$ | 0.7 | 0.97 | 1.2 | V |
| CTRL pin HIGH-level voltage | $V_{CTRL\ H}$ | CTRL ϕ and CTRL1 common, CMOS-level input. | 4.0 | — | — | V |
| CTRL pin LOW-level voltage | $V_{CTRL\ L}$ | CTRL pin threshold $V_{th} = 2.5V$ | — | — | 1.0 | V |
| CTRL input current | I_{CTRL} | 5V input voltage | — | 53 | 110 | μA |
| Thermal shutdown operating temperature | TSD | Design value | 150 | 180 | 210 | $^{\circ}C$ |
| TSD hysteresis | ΔTSD | Design value | — | 15 | — | $^{\circ}C$ |

Performance Characteristics



Mode Switching Truth Table

| CTRL ϕ ¹ | CTRL1 ¹ | Mode |
|--------------------------|--------------------|--------------|
| LOW | LOW | Control |
| LOW | HIGH | Non-feedback |
| HIGH | LOW | Increment |
| HIGH | HIGH | Decrement |

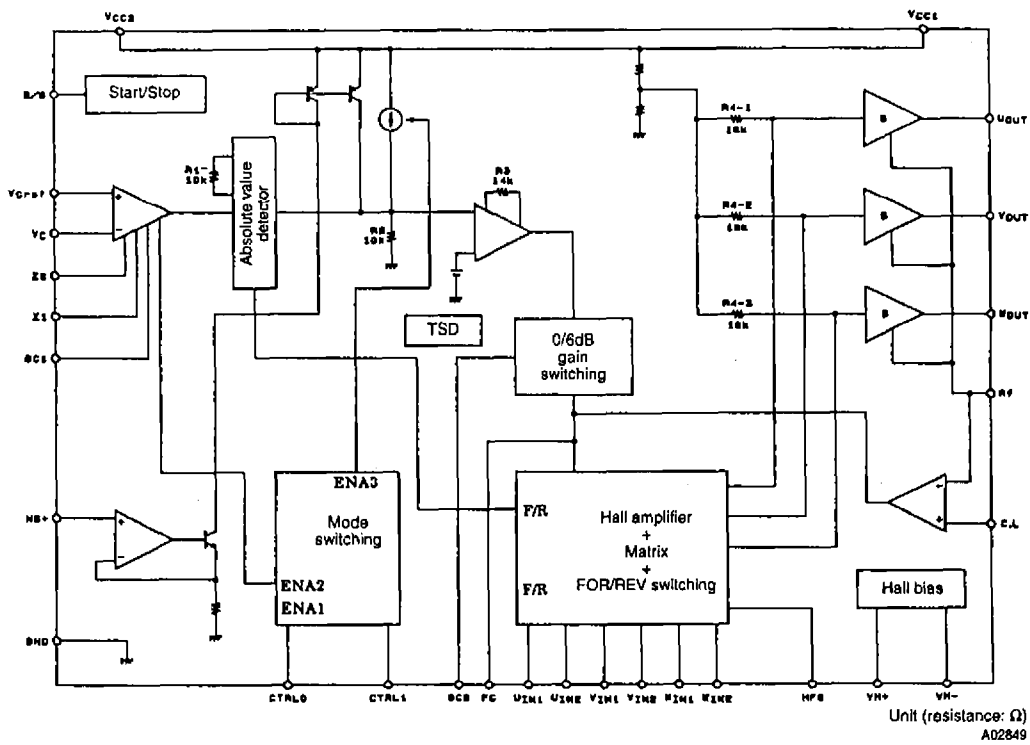
1. LOW = 0 to 1.0V, and HIGH $\geq 4.0V$.

Hall Element Logic Truth Table

| | Source → sink | Hall Input ¹ | | | Forward/Reverse control ² |
|---|-------------------|-------------------------|-----------------|-----------------|--------------------------------------|
| | | U _{IN} | V _{IN} | W _{IN} | |
| 1 | W phase → V phase | HIGH | HIGH | LOW | Forward |
| | V phase → W phase | | | | Reverse |
| 2 | W phase → U phase | HIGH | LOW | LOW | Forward |
| | U phase → W phase | | | | Reverse |
| 3 | V phase → W phase | LOW | LOW | HIGH | Forward |
| | W phase → V phase | | | | Reverse |
| 4 | U phase → V phase | LOW | HIGH | LOW | Forward |
| | V phase → U phase | | | | Reverse |
| 5 | V phase → U phase | HIGH | LOW | HIGH | Forward |
| | U phase → V phase | | | | Reverse |
| 6 | U phase → W phase | LOW | HIGH | HIGH | Forward |
| | W phase → U phase | | | | Reverse |

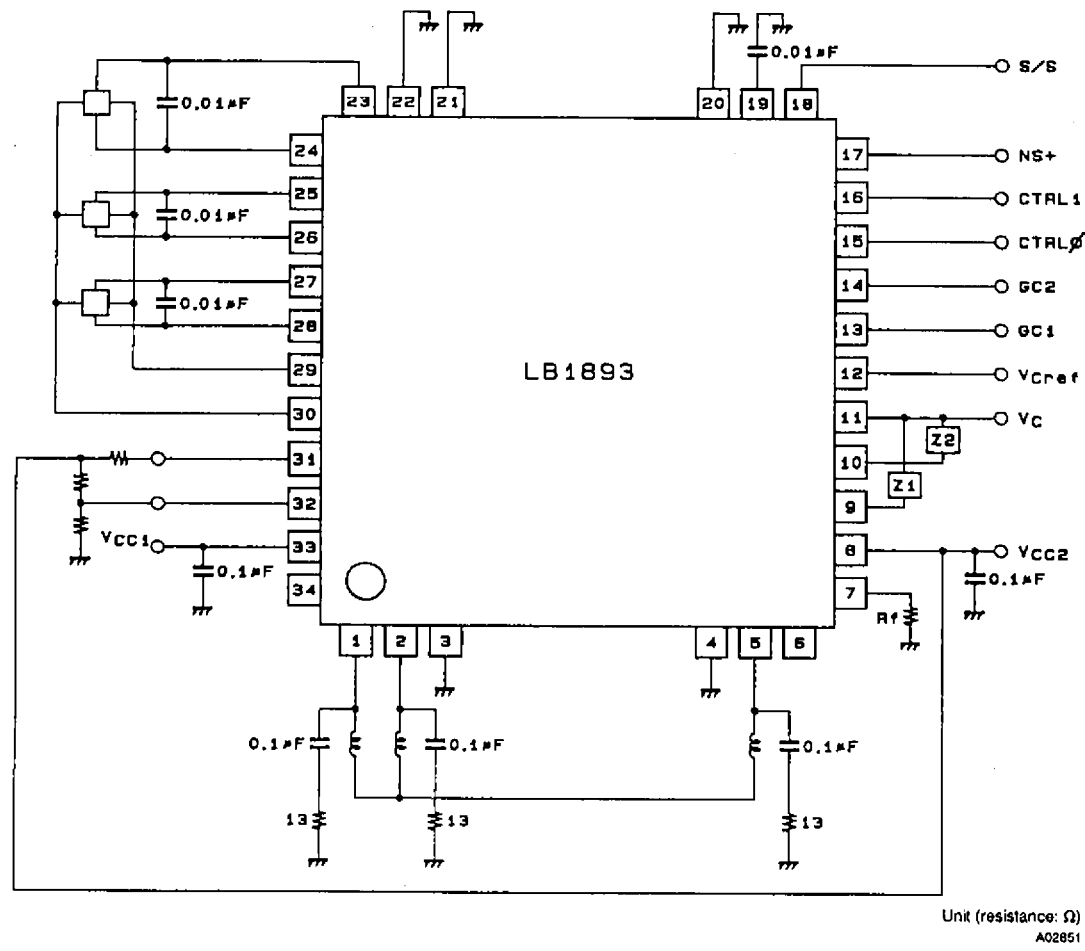
1. An input is considered to be HIGH when U_{IN1} > U_{IN2}, V_{IN1} > V_{IN2}, and W_{IN1} > W_{IN2} by 0.2V or more.
2. Forward is selected when V_C > V_{Cref}. Reverse is selected when V_C < V_{Cref}.

Block Diagram

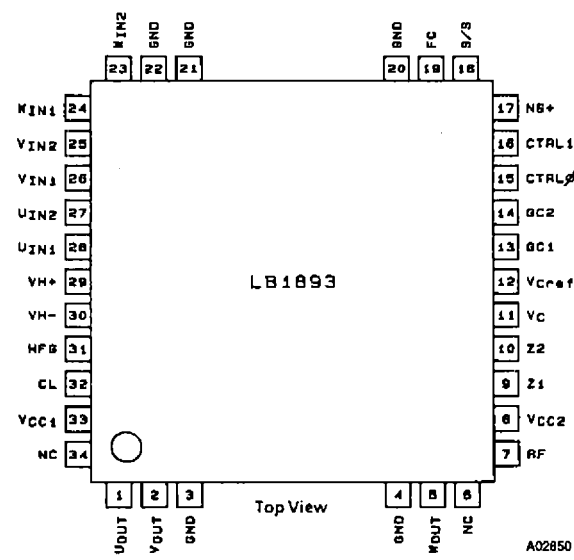


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Sample Peripheral Circuit



Pin Assignment

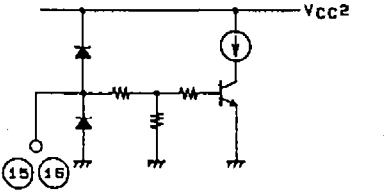
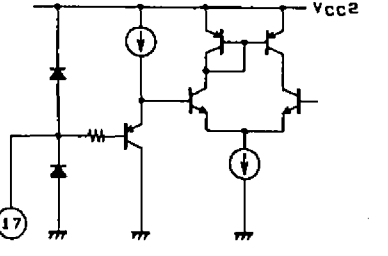
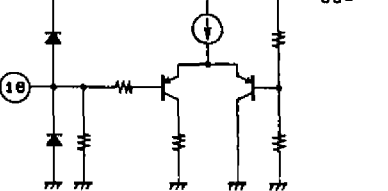
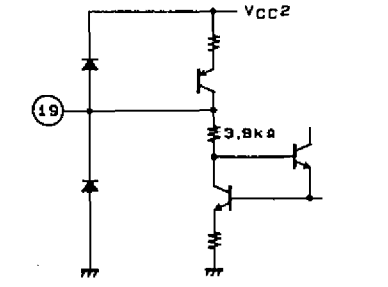
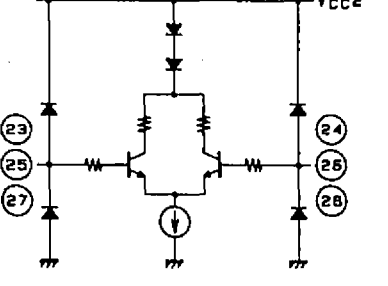
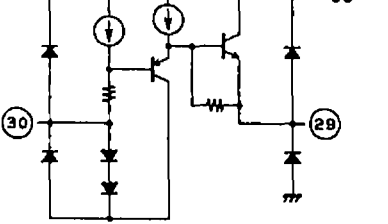


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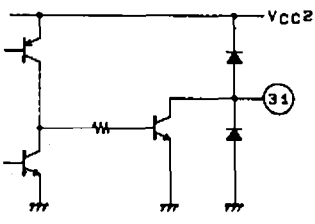
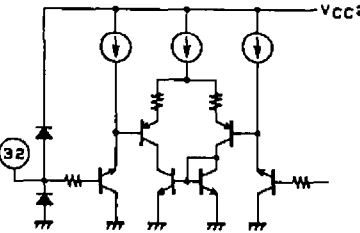
Pin Functions

| Number | Name | Pin voltage | Equivalent circuit | Function |
|--------------|-------------------------------------|---------------------|--------------------|---|
| 3, 4, 20, 21 | Frame GND | | | Frame ground. Connected to the common ground. |
| 22 | GND | | | Ground pin |
| 1 2 5 | U_{OUT} V_{OUT} W_{OUT} | | | Output pins. Connected to the motor. |
| 7 | Rf | | | Output transistor ground. A resistor can be connected between this pin and GND to sense the output current as a voltage drop to provide for overcurrent protection. |
| 6, 34 | NC | | | No connection |
| 8 | V_{CC2} | 4.3 to 6.5V | | Supply for all circuits except the output stage. This supply should be kept stable to prevent noise from entering this pin. |
| 9 10 | Z1 Z2 | | | First-stage amplifier gain setting impedance connection. Z1 and Z2 should be in the order of 30kΩ to several hundred kΩ. The gain should be in the order of 6dB. |
| 11 12 | V_C V_{Cref} | $V_{CC2}/2 \pm 1.0$ | | V_C is the speed control pin; forward when $V_C > V_{Cref}$ and reverse when $V_C < V_{Cref}$. The output voltage is controlled by the V_C voltage. V_{Cref} determines the motor control stop voltage, and is normally set to $V_{CC2}/2$. |
| 13 14 | GC1 GC2 | 0 to V_{CC2} | | Input gain control switching pin. GC1 switches the first-stage amplifier impedances Z1 and Z2. Z1 is selected when GC1 is LOW, and Z2 is selected when GC1 is HIGH. GC2 is the second-stage amplifier switching pin. |

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| Number | Name | Pin voltage | Equivalent circuit | Function |
|----------|--------------------------------------|----------------------------|--|--|
| 15 16 | CTRL ϕ CTRL1 | 0 to V _{CC2} |  A02857 | Operating mode switch pin. The mode switching truth table shows how to select control, non-feedback, and speed increment/decrement modes. |
| 17 | NS+ | 0 to V _{CC2} - 1V |  A02858 | Non-feedback mode input pin. Input-output gain is approximately 14dB (GC2 = LOW) Motor stops when V _{NS} = 0V. |
| 18 | S/S | 0 to V _{CC2} |  A02859 | Start/Stop pin. Start when HIGH, and stop when LOW. The threshold is V _{CC2} /2. |
| 19 | FC | |  A02860 | Connect a capacitor between this pin and ground to reduce the input-output gain frequency response and to prevent abnormal oscillation. |
| 23 24 | W _{IN2} W _{IN1} | 1.3 to 2.2V |  A02861 | W-phase Hall device input pins. Logic HIGH is represented by W _{IN1} > W _{IN2} . |
| 25 26 | V _{IN2} V _{IN1} | | | V-phase Hall device input pins. Logic HIGH is represented by V _{IN1} > V _{IN2} . |
| 27 28 | U _{IN2} U _{IN1} | | | U-phase Hall device input pins. Logic HIGH is represented by U _{IN1} > U _{IN2} . |
| 29 30 | VH+ VH- | 2.4V 1.4V |  A02862 | Hall device supply pins. The potential difference between VH+ and VH- is 1.0V. |

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| Number | Name | Pin voltage | Equivalent circuit | Function |
|--------|-----------|----------------|---|--|
| 31 | HFG | 0 to V_{CC2} |  | Hall device FG pin. The Hall device waveform is converted to a pulse and used as the FG pulse. |
| 32 | CL | 0 to V_{CC2} |  | When the voltage on Rf pin becomes equal to the voltage on CL, the current limiter operates. The CL voltage is determined externally. |
| 33 | V_{CC1} | 5 to 18V | | Output-stage supply pin. This supply should be kept stable to prevent noise from entering this pin. |

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