Monolithic Digital IC

LB1910N

FDD Spindle Motor Driver

Overview

The LB1910N is a 3-phase disc drive motor driver that is optimal for use as a 3.5-inch FDD spindle motor driver.

Functions and Features

- Three-phase full-wave linear driver
- Digital speed control circuit
- Start and stop circuits (active low)
- RPM switching   H: 300 rpm
                      L: 360 rpm
- Current limiter circuit
- Built-in index comparator
- Thermal shutdown circuit

Package Dimensions

unit: mm

3222-HSOP28

SANYO: HSOP28
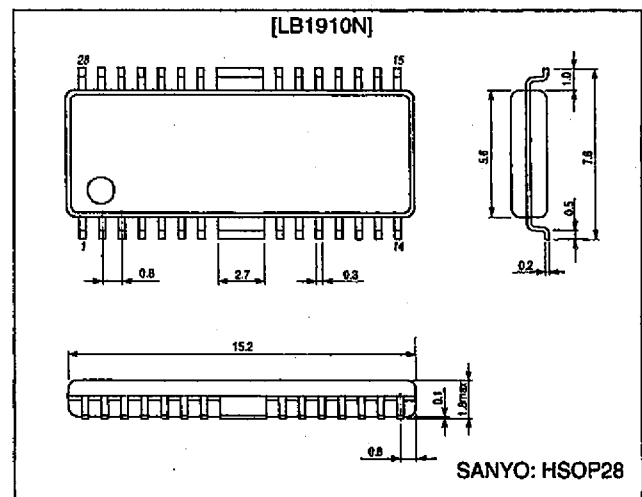
Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Maximum output current	I_O max1	$t \leq 0.5$ s	1.0	A
Maximum steady-state output current	I_O max2		0.7	A
Allowable power dissipation	Pd max	Independent IC	0.5	W
Operating temperature	Topr		−20 to +80	°C
Storage temperature	Tstg		−40 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		4.2 to 6.5	V

Electrical Characteristics at Ta = 25°C, V$_{CC}$ = 5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I$_{CCO}$	S/S = 5 V (standby)			10	μA
	I$_{CC}$	S/S = 0 V (steady state)		12	18	mA
SL bias current	I$_{SL}$	V$_{SL}$ = 0 V			10	μA
SL input low-level voltage	V$_{SLL}$		0		1.0	V
SL input high-level voltage	V$_{SLH}$		3.5		V$_{CC}$	V
S/S bias current	I$_{S/S}$			180	270	μA
S/S low-level voltage	V$_{S/SL}$		0		0.8	V
S/S high-level voltage	V$_{S/SH}$		3.5		V$_{CC}$	V
Hall amplifier input bias current	I$_{HB}$				10	μA
Common-mode input voltage range	Vh		1.5		V$_{CC}$ − 1.0	V
Differential input voltage range	Vdif		50		200	mVp-p
Hall bias output voltage	V$_H$	I$_H$ = 5 mA		0.8		V
Leakage current	I$_{HL}$	S/S = 5 V			±10	μA
Output saturation voltage	Vsat	I$_O$ = 0.7 A, sink + source		1.3	1.8	V
Output leakage current	I$_{OL}$				1.0	mA
Current limiter	Vlim		0.27	0.3	0.33	V
Control amplifier voltage gain	G$_C$			−7		dB
Voltage gain difference between phases	ΔG$_C$				±1	dB
V/I conversion source current	I+		9	14	19	μA
V/I conversion sink current	I−		−9	−14	−19	μA
V/I conversion current ratio	I+/I−		0.8	1.0	1.2	
DSC buffer input current	I$_{DSC}$				1.0	μA
FG Schmitt hysteresis	ΔVsh	*		50		mV
Speed discriminator counts	N			1041.5		
Discriminator operating frequency	F$_D$	*			1.1	MHz
Oscillator frequency range	F$_{OSC}$	*			1.1	MHz
Index input hysteresis	V$_{IDH}$		18	23	28	mV
Index input	V$_{IDO}$	I$_O$ = 2 mA	−5	0	+5	mV
Index output low-level voltage	V$_{IDL}$	I$_O$ = 2 mA			0.4	V
Index output leakage current	I$_{IDL}$				±10	μA
FG amplifier voltage gain	G$_{FG}$	*		48		dB
FG amplifier input offset	V$_{FG O}$				±10	mV
FG amplifier internal reference voltage	V$_{FG B}$		2.2	2.5	2.8	V
Thermal shutdown temperature	TSD	*	150	180		°C
Hysteresis	ΔTSD	*		40		°C

Note: * Items marked with an asterisk are design target values and are not measured.

Pin Assignment

Pin	Name		Pin	Name
1	L		28	I⁺
2	ID		27	FG_OUT
3	(NC)		26	FG_IN⁻
4	SS		25	FG_IN⁺
5	SL		24	HB
6	CLK		23	W_IN⁻
7	GND		22	W_IN⁺
RADIATION FRAME			RADIATION FRAME	
8	V_CC		21	V_IN⁻
9	Rf		20	V_IN⁺
10	D_O		19	U_IN⁻
11	FC		18	U_IN⁺
12	(NC)		17	(NC)
13	U_OUT		16	W_OUT
14	P_GND		15	V_OUT
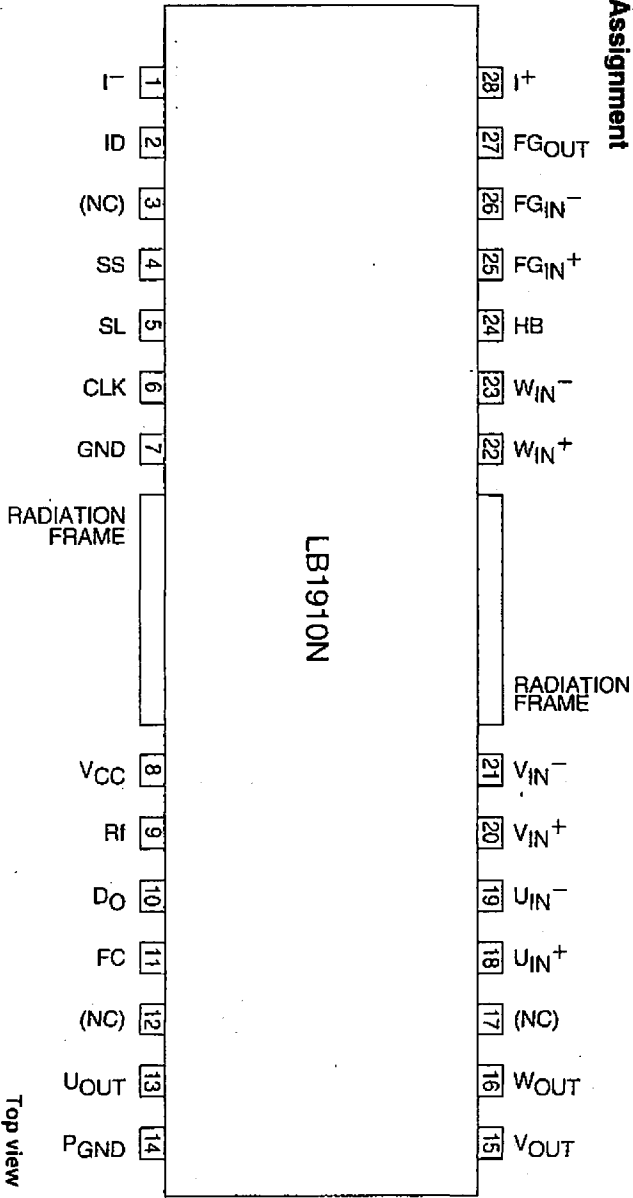
LB1910N

Top view

A06533

Truth Table

	Source → sink	Hall input		
		U	V	W
1	V phase → W phase	H	H	L
2	V phase → U phase	H	L	L
3	W phase → U phase	H	L	H
4	W phase → V phase	L	L	H
5	U phase → V phase	L	H	H
6	U phase → W phase	L	H	L

Note: Hall input high levels are defined as: $U_{IN}^+ > U_{IN}^-$
$V_{IN}^+ > V_{IN}^-$
$W_{IN}^+ > W_{IN}^-$

Index Pulse Timing Chart

A06534

Allowable power dissipation, Pdmax — W

Pd max — Ta

Independent IC

0.28

Ambient temperature, Ta — °C
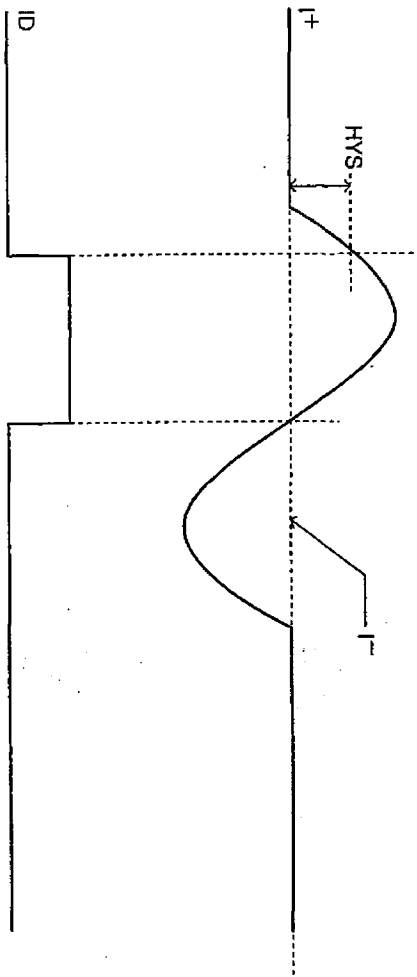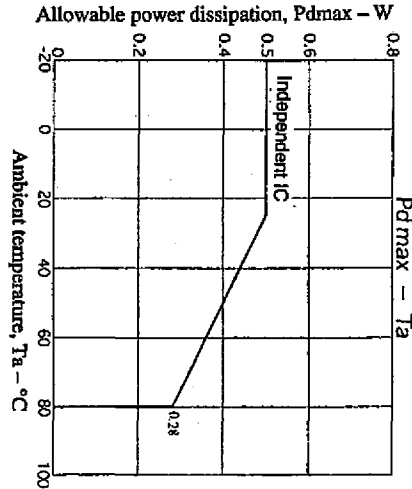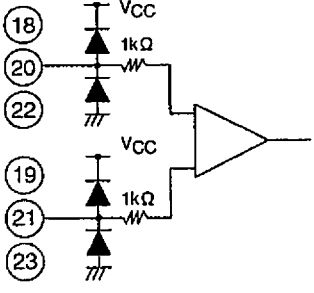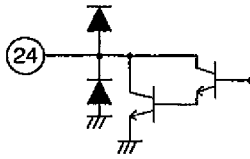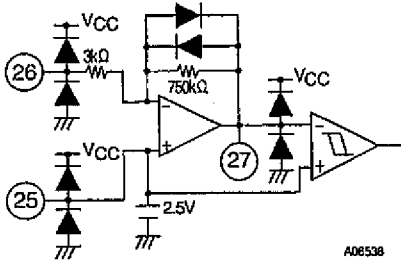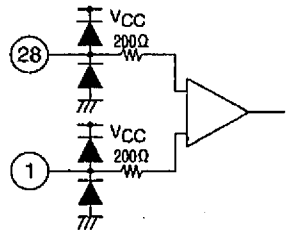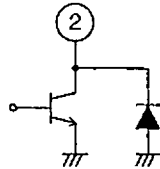
Block Diagram
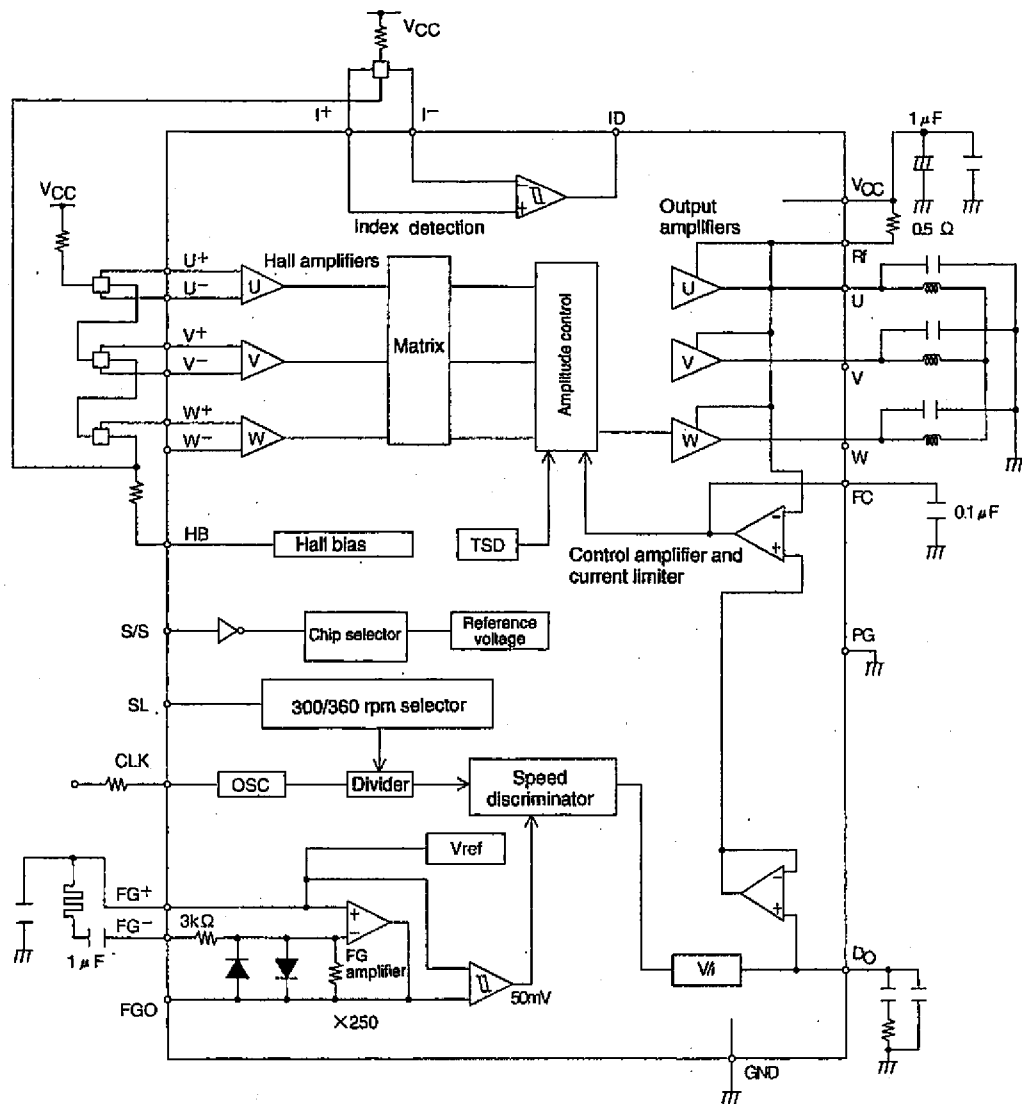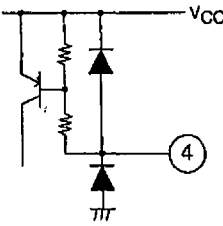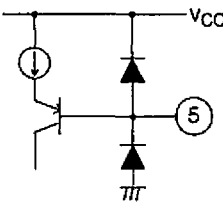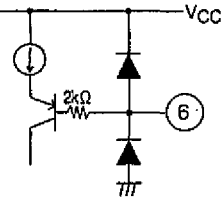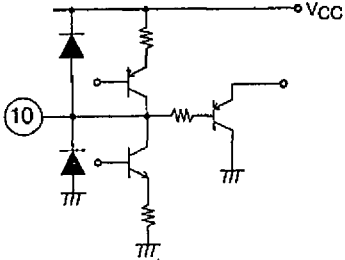
Pin Functions

Pin No.	Symbol	Pin voltage	Equivalent circuit diagram	Function
18 19 20 21 22 23	U_{IN}^+ U_{IN}^- V_{IN}^+ V_{IN}^- W_{IN}^+ W_{IN}^-	1.5 V min $V_{CC} - 1.0$ V max	A06536	U phase Hall element input V phase Hall element input W phase Hall element input
24	HB	0.8 V typ $(I_H = 5$ mA$)$	A06537	Minus side connection for providing the Hall bias current This pin becomes open in the stopped state, thus cutting the Hall bias current.
25 26 27	FG_{IN}^+ FG_{IN}^- FG_{OUT}	2.5 V	A06538	• FG amplifier plus input A 2.5-V reference voltage is generated internally. • FG amplifier minus input • FG amplifier output
28 1	I+ I-		A06539	Index input
2	ID	L: 0.4 V max H: 4.5 V min	A06540	Index output

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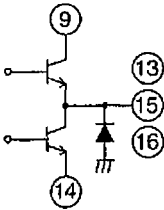
Pin No.	Symbol	Pin voltage	Equivalent circuit diagram	Function
4	SS	L: 0.8 V max H: 3.5 V min	*(circuit diagram — A06541)*	Start/stop mode switching This is an active-low input.
5	SL	L: 1.0 V max H: 3.5 V min	*(circuit diagram — A06542)*	Rotational speed switching
6	CLK	L: 1.0 V max H: V_{CC} − 1.0 V min	*(circuit diagram, 2kΩ — A06543)*	Reference clock input A 1-MHz input frequency corresponds to speeds of 300 and 360 rpm.
7	GND			• Ground • This pin, pin 14, and the frame must all be grounded together.
8	V_{CC}			Power supply This voltage must be stabilized so that ripple and noise do not enter the IC.
9	Rf			Output current detection The output current is detected as a voltage by connecting the resistor Rf between this pin and V_{CC}. The current limiter operates by detecting the voltage on this pin.
10	D_O		*(circuit diagram — A06544)*	Speed discriminator
11	F_C			Frequency characteristics compensation Current control system loop oscillation is prevented by connecting a capacitor between this pin and ground.

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Pin No.	Symbol	Pin voltage	Equivalent circuit diagram	Function
13 15 16	U_{OUT} V_{OUT} W_{OUT}		 A06545	U phase output V phase output W phase output
14	P_{GND}			Output transistor ground connection

This catalog provides information as of March, 1997. Specifications and information herein are subject to change without notice.