Ordering number: EN ※3966A

CMOS LSI

SANYO

No.※3966A

LC573404A, 573406A

4-bit Single Chip Microcomputer with LCD Driver

Preliminary

OVERVIEW

The LC573404A and LC573406A are low-power 4-bit microcontrollers with built-in 4- and 6-Kbyte ROMs, respectively.
They incorporate a 120-segment LCD driver, RAM, a 4-bit parallel-processing ALU, a 16-bit timer and a carrier output for infrared remote control applications.
The LC573404A and LC573406A are ideal for use in battery-operated measuring instruments, products that require timing functions, and LCD and remote controller applications.
The LC573404A and LC573406A operate from a 2.3 to 6.0 V supply and are available in 64-pin QFPs and as dice.

FEATURES

1) ROM 6 Kbytes (LC573406A)
4 Kbytes (LC573404A)
2) RAM 512-bit (128 × 4)
3) 4-bit parallel-processing ALU
4) 120-segment LCD controller/driver
- 30 segment outputs
- Four common outputs
  120-segment capability when using 1/4 duty
  90-segment capability when using 1/3 duty
  60-segment capability when using 1/2 duty
  30-segment capability when using static drive

SEG16 to SEG30 can be used as normal, p-channel open-drain output ports.

5) 16-bit software-controllable timer

6) 455 kHz ceramic resonator timebase
- Configurable as a 15-bit free-running timer
- 108 ms HALT-mode cancel signal output

7) HALT mode
- Reduces current consumption.
- Suspends program execution.
- Exited by a system reset or the HALT-mode cancel signal.

8) STOP mode
- Stops the ceramic resonator oscillator.
- Exited by a system reset or under program control.

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

9) HOLD mode
- Stops the ceramic resonator oscillator.
- Exited by a system reset or a HIGH level on ports S or M.

10) Two-level subroutine stack

11) Cycle Time
- 17.6 μs and 122 μs cycle times at f = 455 kHz and 32.768 kHz, respectively

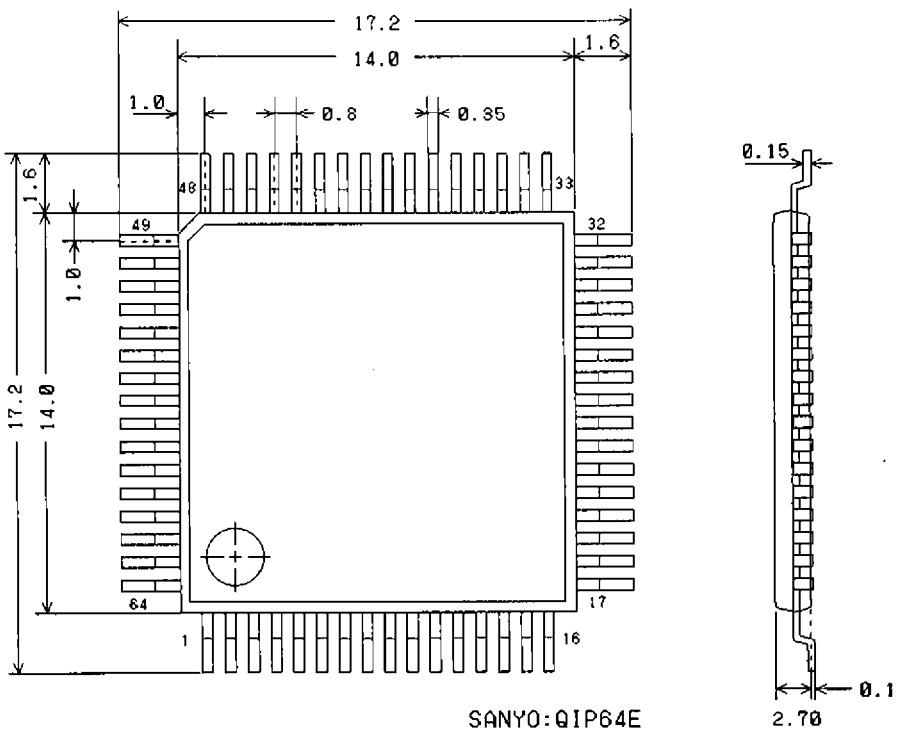
12) Software-controllable remote control carrier signal generator
- Software-controllable frequency and duty cycle
- 1 to 200 kHz
- Three fixed waveforms
  - 38 kHz with 1/3 duty
  - 38 kHz with 1/2 duty
  - 57 kHz with 1/2 duty

13) Built-in ceramic and crystal oscillators
14) Ports
- Two 4-bit keyscan input ports
- Two 4-bit keyscan output ports
- One 2-bit keyscan expansion or LED driver port

15) Voltage
- 2.3 to 6.0 V supply voltage

16) Factory shipment
- 64-pin QFP and 66-pad die

PINOUT

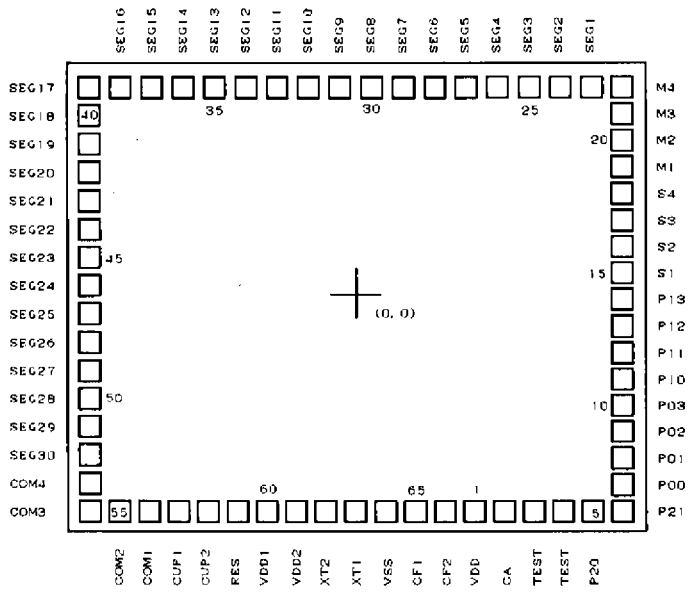


Do not use a soldering iron when mounting the package.

DIE SPECIFICATIONS

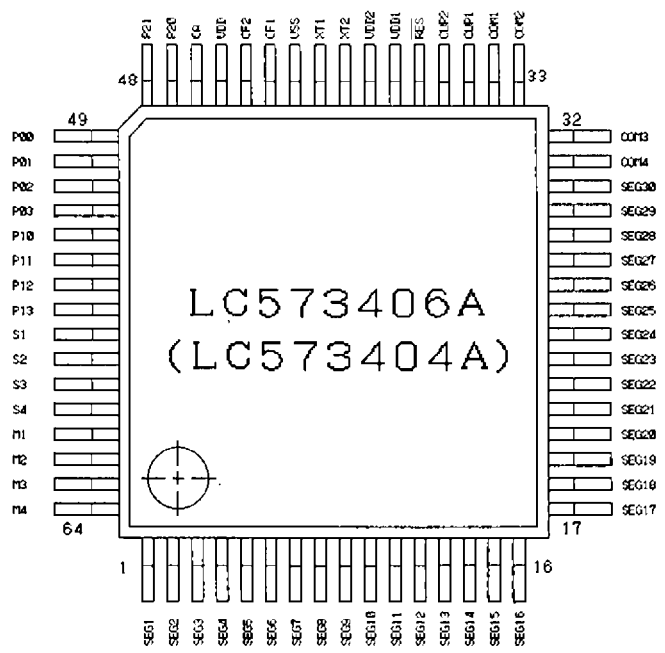
Chip size	: 3.89 mm × 3.59 mm
Pad size	: 120 μm × 120 μm
Chip thickness	: 480 μm

Pad Layout



Pin Assignment of Package

Chip thickness : 330 μm



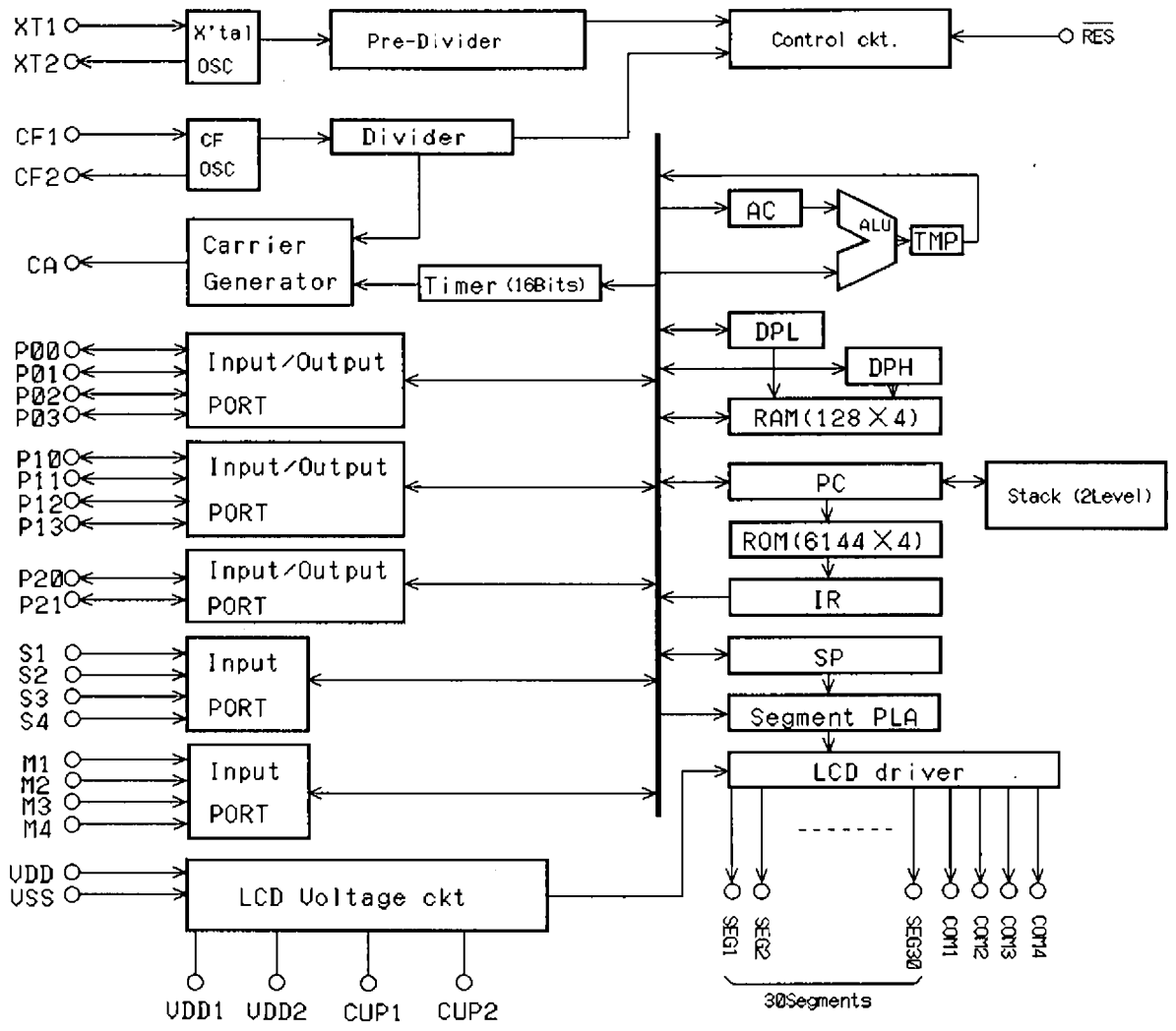
SANYO: QIP64E

Pad Coordinates

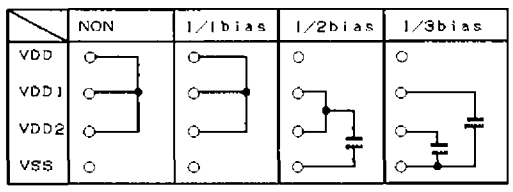
QFP64 Pin No	pad No.	Pad Name	X (μm)	Y (μm)
45	1	VDD	720	−1530
46	2	CA	975	−1530
−	3	TEST	1155	−1530
−	4	TEST	1335	−1530
47	5	P20	1515	−1530
48	6	P21	1700	−1530
49	7	P00	1690	−1170
50	8	P01	1690	− 990
51	9	P02	1690	− 810
52	10	P03	1690	− 630
53	11	P10	1690	− 450
54	12	P11	1690	− 270
55	13	P12	1690	− 90
56	14	P13	1690	90
57	15	S1	1690	310
58	16	S2	1690	490
59	17	S3	1690	670
60	18	S4	1690	850
61	19	M1	1690	1030
62	20	M2	1690	1210
63	21	M3	1690	1390
64	22	M4	1690	1570
1	23	SEG1	1130	1600
2	24	SEG2	950	1600
3	25	SEG3	770	1600
4	26	SEG4	590	1600
5	27	SEG5	410	1600
6	28	SEG6	230	1600
7	29	SEG7	50	1600
8	30	SEG8	− 130	1600
9	31	SEG9	− 310	1600
10	32	SEG10	− 490	1600
11	33	SEG11	− 670	1600
12	34	SEG12	− 850	1600
13	35	SEG13	−1030	1600

QFP64 Pin No	pad No.	Pad Name	X (μm)	Y (μm)
14	36	SEG14	−1210	1600
15	37	SEG15	−1390	1600
16	38	SEG16	−1570	1600
17	39	SEG17	−1750	1600
18	40	SEG18	−1750	1385
19	41	SEG19	−1750	1205
20	42	SEG20	−1750	1025
21	43	SEG21	−1750	845
22	44	SEG22	−1750	665
23	45	SEG23	−1750	485
24	46	SEG24	−1750	305
25	47	SEG25	−1750	125
26	48	SEG26	−1750	− 55
27	49	SEG27	−1750	− 235
28	50	SEG28	−1750	− 415
29	51	SEG29	−1750	− 595
30	52	SEG30	−1750	− 775
31	53	COM4	−1750	− 955
32	54	COM3	−1750	−1530
33	55	COM2	−1570	−1530
34	56	COM1	−1390	−1530
35	57	CUP1	−1160	−1530
36	58	CUP2	− 980	−1530
37	59	$\overline{\text{RES}}$	− 800	−1530
38	60	VDD1	− 620	−1530
39	61	VDD2	− 440	−1530
40	62	XT2	− 260	−1530
41	63	XT1	− 80	−1530
42	64	VSS	100	−1530
43	65	CF1	360	−1530
44	66	CF2	540	−1530

BLOCK DIAGRAM



PIN DESCRIPTION

Number		Name	Description
QFP64	Die		
45	1	VDD	Supply voltage. See figure 1.
42	64	VSS	Ground. See figure 1.
38 39	60 61	VDD1 VDD2	LCD driver supply voltage inputs. See figure 1. 
35 36	57 58	CUP1 CUP2	LCD driver external coupling capacitor. A non-polarized capacitor should be connected between CUP1 and CUP2 when using 1/2 or 1/3 bias.
43	65	CF1	455kHz ceramic resonator oscillator input
44	66	CF2	455kHz ceramic resonator oscillator output
41	63	XT1	32.768 kHz crystal oscillator input
40	62	XT2	32.768 kHz crystal oscillator output
57 to 60	15 to 18	S1 to S4	Input port S.
61 to 64	19 to 22	M1 to M4	Input port M
49 to 52	7 to 10	P00 to P03	Bidirectional port P0. P-channel open-drain outputs
53 to 56	11 to 14	P10 to P13	Bidirectional port P1. P-channel open-drain outputs
47 48	5 6	P20 P21	Bidirectional port P2. P-channel open-drain outputs. P20 and P21 can be used to directly drive a LED in remote control applications.

<table>
<tr><th colspan="2">Number</th><th rowspan="2">Name</th><th rowspan="2">Description</th></tr>
<tr><th>QFP64</th><th>Die</th></tr>
<tr><td>46</td><td>2</td><td>CA</td><td>Remote control carrier output</td></tr>
<tr><td>37</td><td>59</td><td>$\overline{\text{RES}}$</td><td>Reset input. Internal pull-up resistor</td></tr>
<tr><td>34
33
32
31</td><td>56
55
54
53</td><td>COM1
COM2
COM3
COM4</td><td>LCD common driver outputs. The pins required for the various operating modes are indicated in the following table.
<table>
<tr><th rowspan="2">Pin</th><th colspan="4">Duty</th></tr>
<tr><th>Static (64Hz)</th><th>1/2 (32Hz)</th><th>1/3 (42Hz)</th><th>1/4 (32Hz)</th></tr>
<tr><td>COM1</td><td>○</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>COM2</td><td>×</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>COM3</td><td>×</td><td>×</td><td>○</td><td>○</td></tr>
<tr><td>COM4</td><td>×</td><td>×</td><td>×</td><td>○</td></tr>
</table></td></tr>
<tr><td>1 to 15</td><td>23 to 37</td><td>SEG1 to SEG15</td><td>LCD segment driver outputs</td></tr>
<tr><td>16 to 30</td><td>38 to 52</td><td>SEG16 to SEG30</td><td>P-channel open-drain outputs. Configurable as either LCD segment drivers or normal output ports.</td></tr>
<tr><td rowspan="2">—</td><td>3</td><td rowspan="2">TEST</td><td rowspan="2">Test inputs. Leave open for normal operation.</td></tr>
<tr><td>4</td></tr>
</table>

Supply connections

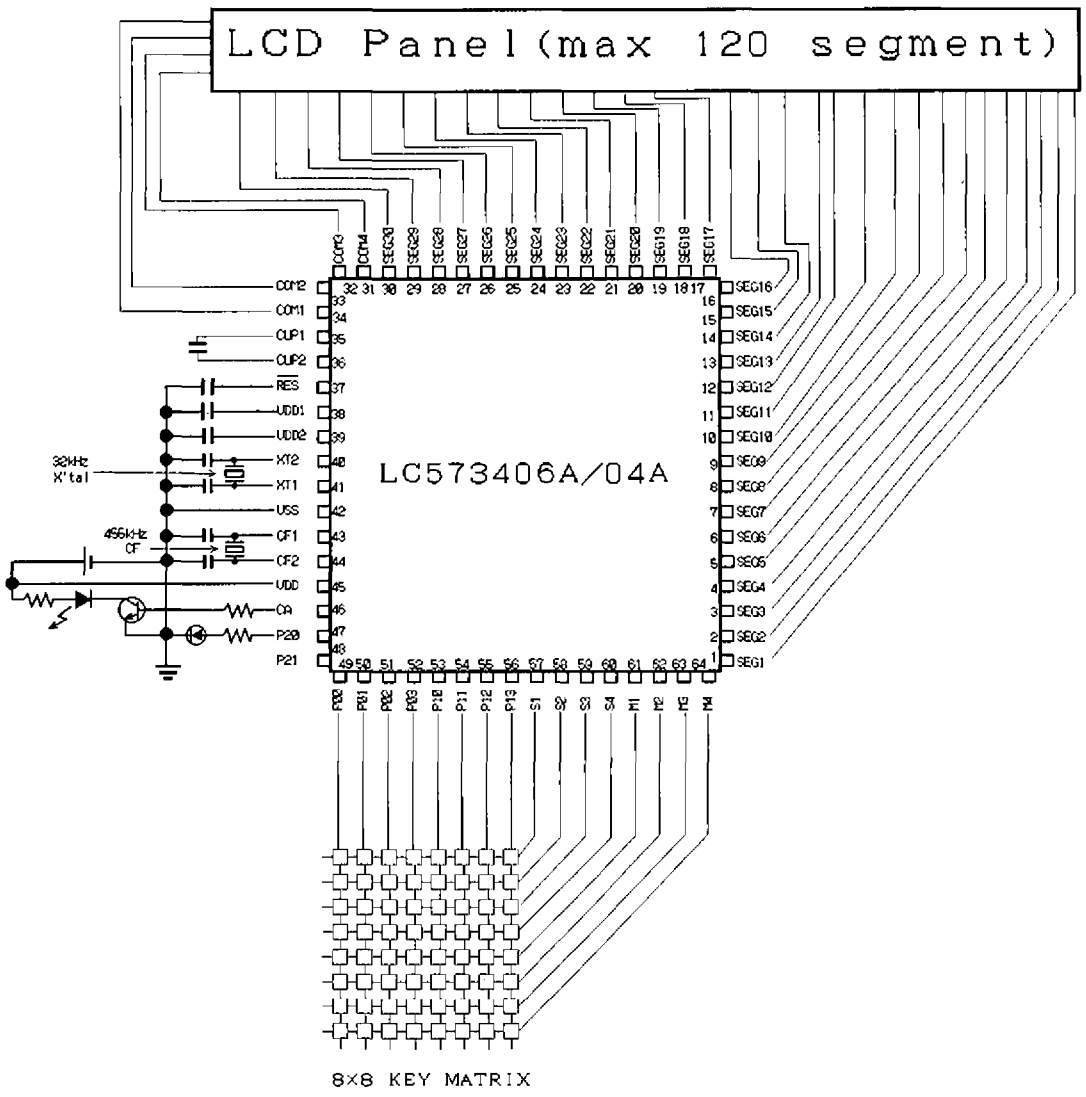


Figure 1. Supply Connections

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to 7.0	V
	V_{DD1}	-0.3 to V_{DD}	V
	V_{DD2}	-0.3 to V_{DD}	V
Input voltage range	V_I	-0.3 to V_{DD}+0.3	V
Output voltage range	V_O	-0.3 to V_{DD}+0.3	V
CA output current	I_{O1}	25	mA
Ports P0 and P1 output current	I_{O2}	0.5	mA
Port P2 output current	I_{O3}	10	mA
Output current for all other ports	I_{O4}	0.5	mA
Total output current of all pins except CA	I_{O5}	25	mA
Operating temperature range	Topr	-30 to 70	℃
Storage temperature range	Tstg	-40 to 125	℃

Recommended Operating Conditions
Vss = 0 V, Ta= 25 ℃

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	3	V
Supply voltage range	V_{DD}	2.3 to 6.0	V

Electrical Characteristics
Vss = 0 V, Ta= -30 to 70 ℃

Parameter	Symbol	Condition	VDD(V)	Rating min	Rating typ	Rating max	Unit
Operating Current	I_{DD}	f = 32.768 kHz, C1 = C2 = 0.1 μF, C_G = C_D = 20 pF, Ta ≦ 50 ℃, oscillator stopped. See note 3.	3.0	-	7	30	μA
			5.0	-	15	50	
		f = 455 kHz, C1 = C2 = 0.1 μF, C_{CD} = C_{CG} = 150 pF, Ta ≦ 50 ℃, oscillator stopped. See note 4.	3.0	-	150	500	
			5.0	-	400	500	

Notes
1. Configured as LCD driver outputs.
2. Configured as p-channel open-drain outputs.
3. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 6, 7 and 8, respectively.
4. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 9, 10 and 11, respectively.
5. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 5, 3 and 4, respectively.

Parameter	Symbol	Condition		Rating			Unit
			VDD(V)	min	typ	max	
HALT-mode supply Current	I_{DDH1}	f = 32.768 kHz, C1 = C2 = 0.1 μF, C_G = C_D = 20 pF, Ta ≦ 50 ℃, oscillator stopped. See note 3.	3.0	-	3	15	μA
			5.0	-	8	50	
		f = 455 kHz, C1 = C2 = 0.1 μF, C_{CD} = C_{CG} = 150 pF, Ta ≦ 50 ℃, oscillator stopped See note 4.	3.0	-	80	500	
			5.0	-	300	400	
	I_{DDH2}	f = 455 kHz, oscillator stopped	5.0	-	0.1	-	μA

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Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Instruction execution time	t_{cyc}	V_{DD} = 2.3 to 6.0, Ceramic resonator, f = 455 kHz	-	17.6	-	μS
		V_{DD} = 2.3 to 6.0, crystal oscillator f = 32.768 kHz	-	122	-	
Ports S, M, P0, P1 and P2 LOW-level input voltage	V_{IL1}	Ports P0, P1 and P2 configured as inputs	0	-	$0.3V_{DD}$	V
Ports S, M, P0, P1 and P2 HIGH-level input voltage	V_{IH1}	Ports P0, P1 and P2 configured as inputs	$0.7V_{DD}$	-	V_{DD}	V
RES LOW-level input voltage	V_{IL2}		0	-	$0.25V_{DD}$	V
RES HIGH-level input voltage	V_{IH2}		$0.75V_{DD}$	-	V_{DD}	V

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5. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 5, 3 and 4, respectively.

Parameter	Symbol	Condition		Rating			Unit
			V_{DD}(V)	min	typ	max	
Ports S and M input impedance	R_{I1}	V_{IL} = 0.4 V, LOW-level hold transistor ON. See figure 2.	2.9	150	300	1000	kΩ
			5.0	70	200	600	
	R_{I2}	V_{IL} = 0.4 V, LOW-level pull-down transistor ON See figure 2.	2.9	60	100	150	kΩ
			5.0	60	100	150	
RES input impedance	R_{I3}		2.9	10	-	300	kΩ
			5.0	10	-	300	
SEG1 to SEG30 MID-level output voltage	V_{OM1}	I_{OL} = 0.4 μA, I_{OH} = -0.4 μA, 1/3 bias	2.9	$2V_{DD}/3$ - 0.2	-	$2V_{DD}/3$ + 0.2	V
			5.0	$2V_{DD}/3$ - 0.2	-	$2V_{DD}/3$ + 0.2	
	V_{OM1-1}	See note 1.	2.9	$V_{DD}/3$ - 0.2	-	$V_{DD}/3$ + 0.2	V
			5.0	$V_{DD}/3$ - 0.2	-	$V_{DD}/3$ + 0.2	
	V_{OM1-2}	I_{OL} = 0.4 μA, See note 1.	2.9	-	-	0.2	V
			5.0	-	-	0.2	
SEG1 to SEG30 HIGH-level output voltage	V_{OH1}	I_{OH} = -0.4 μA, See note 1.	2.9	V_{DD}-0.2	-	-	V
			5.0	V_{DD}-0.2	-	-	
	V_{OH2}	I_{OH} = -45 μA, See note 2.	2.9	V_{DD}-0.45	-	-	V
		I_{OH} = -75 μA, See note 2.	5.0	V_{DD}-0.75	-	-	

Notes

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2. Configured as p-channel open-drain outputs.
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4. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 9, 10 and 11, respectively.
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Parameter	Symbol	Condition		Rating			Unit
			V_{DD}(V)	min	typ	max	
SEG1 to SEG30 LOW-level leakage current	I_{LL1}	$V_I = V_{SS}$, See note 2.	2.9	-	-	1	μA
			5.0	-	-	1	
SEG1 to SEG30 HIGH-level leakage current	I_{LH1}	$V_I = V_{DD}$, See note 2.	2.9	-1	-	-	μA
			5.0	-1	-	-	
COM1 to COM4 LOW-level output voltage	V_{OL1}	I_{OL} = 4 μA	2.9	-	-	0.2	V
			5.0	-	-	0.2	
COM1 to COM4 MID-level output voltage	V_{OM2-1}	1/2 bias	2.9	$V_{DD}/2$ - 0.2	-	$V_{DD}/2$ + 0.2	V
			5.0	$V_{DD}/2$ - 0.2	-	$V_{DD}/2$ + 0.2	
	V_{OM2-2}	1/3 bias, I_{OH} = - 4 μA	2.9	$2V_{DD}/3$ - 0.2	-	$2V_{DD}/3$ + 0.2	V
			5.0	$2V_{DD}/3$ - 0.2	-	$2V_{DD}/3$ + 0.2	
	V_{OM2-3}	1/3 bias, I_{OL} = - 4 μA	2.9	$V_{DD}/3$ - 0.2	-	$V_{DD}/3$ + 0.2	V
			5.0	$V_{DD}/3$ - 0.2		$V_{DD}/3$ + 0.2	
COM1 to COM4 HIGH-level output voltage	V_{OH3}	I_{OL} = - 4 μA	2.9	V_{DD}-0.2	-	-	V
			5.0	V_{DD}-0.2	-	-	
Ports P0 and P1 HIGH-level output voltage	V_{OH4}	I_{OH} = -450 μA,	2.9	V_{DD} - 0.45	-	-	V
		I_{OH} = -500 μA	5.0	V_{DD} - 0.50	-	-	

Notes

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2. Configured as p-channel open-drain outputs.
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5. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 5, 3 and 4, respectively.

Parameter	Symbol	Condition		Rating			Unit
			V_{DD}(V)	min	typ	max	
Ports P0 and P1 LOW-level leakage current	I_{LL2}	V_I = V_{SS},	2.9	–	–	1	μA
			5.0	–	–	1	
Ports P0 and P1 HIGH-LEVEL leakage current	I_{LH2}	V_I = V_{DD},	2.9	-1	–	–	μA
			5.0	-1	–	–	
Port P2 HIGH-level output voltage	V_{OH5}	I_{OH} = -1.0 mA,	2.9	V_{DD}-0.5	–	–	V
			5.0	V_{DD}-0.5	–	–	
Port P2 LOW-level leakage current	I_{LL3}	V_I = V_{SS},	2.9	–	–	1	μA
			5.0	–	–	1	
Port P2 HIGH-level leakage current	I_{LH3}	V_I = V_{DD},	2.9	-1	–	–	μA
			5.0	-1	–	–	
CA LOW-level output current	I_{OL1}	V_{OL} = 0.9 V,	3.0	2	5	–	mA
			5.0	2	5	–	
CA HIGH-level output current	I_{OH1}	V_{OH} = V_{DD} – 1.5 V,	3.0	6	12	–	mA
		V_{OH} = V_{DD} – 2.5 V,	5.0	10	20	–	
V_{DD1} output voltage	V_{DD1-1}	C1 =C2 = 0.1 μF, f =32.768 kHz, 1/2 bias. See figure 3	3.0	1.3	1.5	1.7	V
			5.0	2.4	2.5	2.6	
V_{DD1} – V_{DD2} voltage differential	V_{DD1-2}	C1 =C2 = 0.1 μF, f =32.768 kHz, 1/3 bias. See figure 4	3.0	1.8	2.0	2.2	V
			5.0	3.1	3.33	3.5	

Notes

1. Configured as LCD driver outputs.
2. Configured as p-channel open-drain outputs.
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5. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 5, 3 and 4, respectively.

Parameter	Symbol	Condition		Rating				Unit
				V_{DD} (V)	min	typ	max	
V_{DD2} output voltage	V_{DD2}	C1 =C2 = 0.1 μF, f =32.768 kHz, 1/3 bias. See figure 4		3.0	0.8	1.0	1.2	V
				5.0	1.4	1.67	1.8	
Power supply leakage current	I_{LK}	ceramic resonator	Ta = 25 ℃	3.0	-	0.2	1	μA
				5.0	-	0.2	1	
			Ta = 50 ℃	3.0	-	1	5	
				5.0	-	1	5	
Oscillator start-up voltage	V_{ST}	Crystal oscillator , f = 32.768 kHz, C_G= C_D= 20 pF, See note 5.			-	-	2.3	V
		Ceramic resonator, f = 455 kHz, C_{CD}= C_{CG}= 150 pF, See note 5.			-	-	2.3	
Oscillator sustaining voltage	V_{SUS}	Crystal oscillator , f = 32.768 kHz, C_G= C_D= 20 pF, See note 5.			2	-	-	V
		Ceramic resonator, f = 455 kHz, C_{CD}= C_{CG}= 150 pF, See note 5.			2	-	-	

Notes

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5. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 5, 3 and 4, respectively.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator start-up time	t_{ST}	V_{DD} = 2.3 V, crystal oscillator f = 32.768 kHz, C_G= C_D= 20 pF, See note 5.	–	–	5	s
		V_{DD} = 2 V, ceramic resonator, f = 455 kHz, C_{CG}= C_{CD}= 150 pF. See note 5.	–	–	30	ms
Oscillator operating frequency range	fopg	32.768 kHz crystal oscillator See figure 12.	32	32.768	33	kHz
		455 kHz ceramic resonator. See figure 13.	380	455	500	
Crystal oscillator external adjustment capacitor range	C_D		16	20	24	pF

Notes
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2. Configured as p-channel open-drain outputs.
3. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 6, 7 and 8, respectively.
4. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 9, 10 and 11, respectively.
5. The measurement circuit for static drive, 1/2 or 1/3 bias is shown in figures 5, 3 and 4, respectively.

Measurement Circuits
The following conditions apply to figures 3 to 5.
- Ports S and M have their hold transistors enabled.
- Bidirectional ports are in output mode and are all HIGH.
- LCD drivers are open-circuit.
- RESis open-circuit and is connected to an internal resistor.
- 32 kHz crystal oscillator frequency
- 455 kHz ceramic oscillator frequency

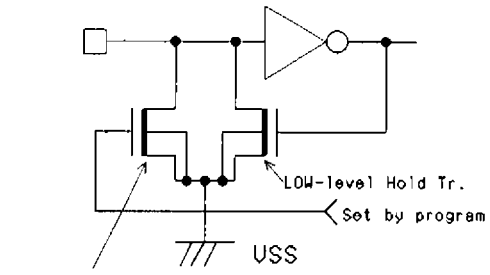


Figure 2. Input hold transistor

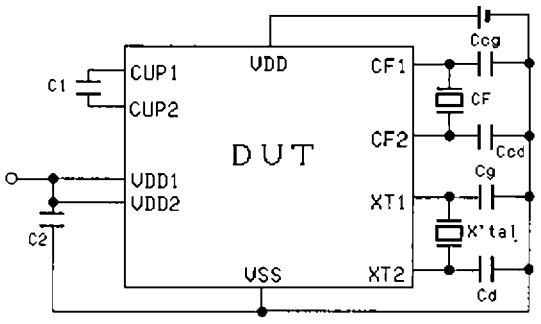


Figure 3. Oscillator characteristics 1

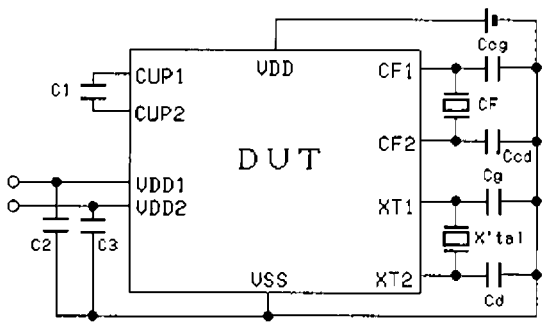


Figure 4. Oscillator characteristics 2

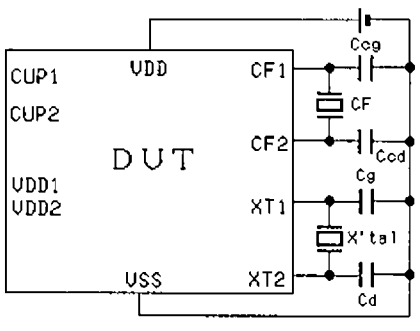


Figure 5. Oscillator characteristics 3

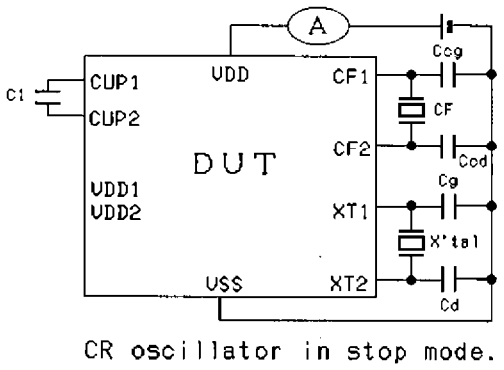


Figure 6. Supply current measurement 1

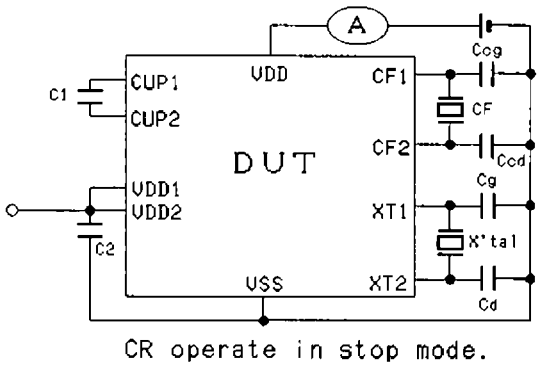
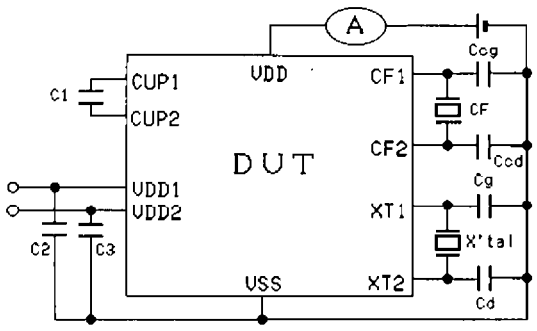


Figure 7. Supply current measurement 2



CR operate in stop mode.

Figure 8. Supply current measurement 3

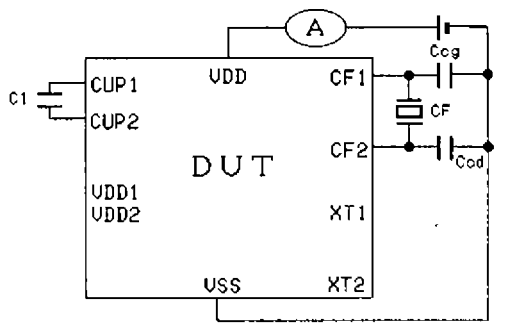


Figure 9. Supply current measurement 4

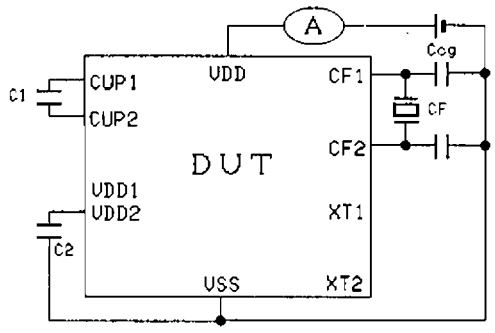


Figure 10. Supply current measurement 5

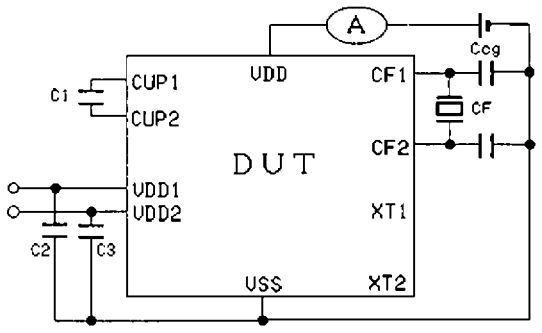


Figure 11. Supply current measurement 6

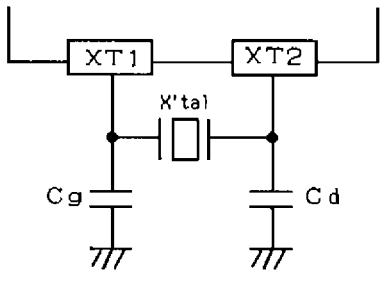


Figure 12. Crystal oscillator connections

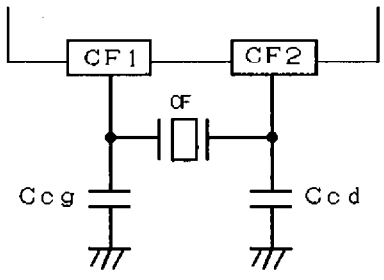


Figure 13. Ceramic oscillator connections

Recommended Oscillators

Oscillator	Manufacturer	Part number	CG/CCG(pF)	CD/CCD(pF)
32.768 kHz crystal oscillator	Kyocera	KF-38G	18	18
		KF-38Y	16	16
	Daishinku	DT-38	15	15
455 kHz ceramic resonator	Kyocera	KBR-455BK	150	150
	Murata	CSB455E	150	150

DEVELOPMENT TOOLS
Manuals

- LC573400 Series User's Manual
- LC573400 Series Development Tools

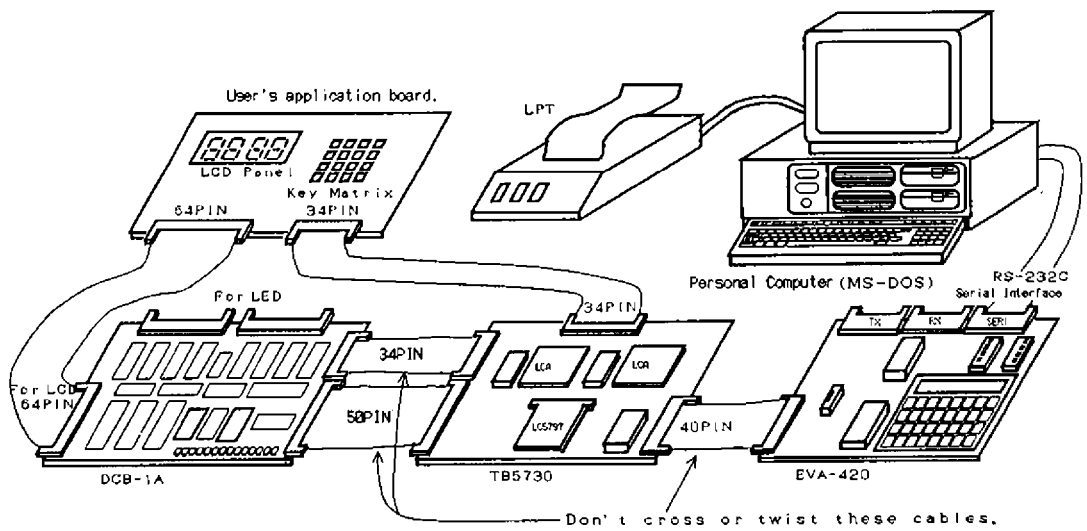
Hardware/Software
Software development tools
- Personal computer (MS-DOS based)
- Cross assembler
  LC573406.EXE (LC573406A)
  LC573404.EXE (LC573404A)
- Mask option generator (SU573400.EXE)

Hardware development tools

- LC5797 evaluation chip
- LC5797 evaluation board (TB5730)
- EVA420 evaluation board containing the SCR-5730 monitor ROM
- DCB-1 display and mask option control board (Rev. 3.5)
- User's application development board

Notes
1. The RAM capacity of the LC5797 is different to that of the LC573400 series. The LC5797 has a 256 × 4-bit RAM whereas the LC573400 series has a 128 × 4-bit RAM.
2. When developing software for the LC573400 series on the LC5797 evaluation chip, use only 0H to 7H as values for DPH.

LC573400 Series Development System



MASK OPTIONS

Combined ceramic resonator and crystal oscillator operation

The ceramic resonator and crystal oscillators can be combined in several ways as shown in figure 14.

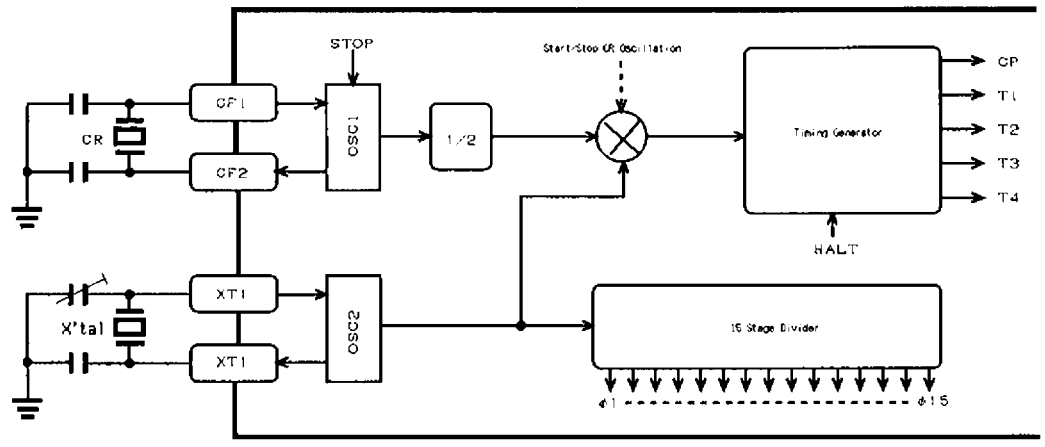


Figure 14. Oscillator configuration 1

In this configuration, the microprocessor cycle time is eight times the ceramic resonator frequency. When the ceramic resonator oscillator is stopped with the CF command, the cycle time is four times the crystal oscillator frequency.
The divider outputs $\phi 1$ to $\phi 15$ are used to generate the LCD drive waveforms and timing pulses.

Ceramic resonator-only operation

In this configuration, the clock circuitry becomes as shown in figure 15.

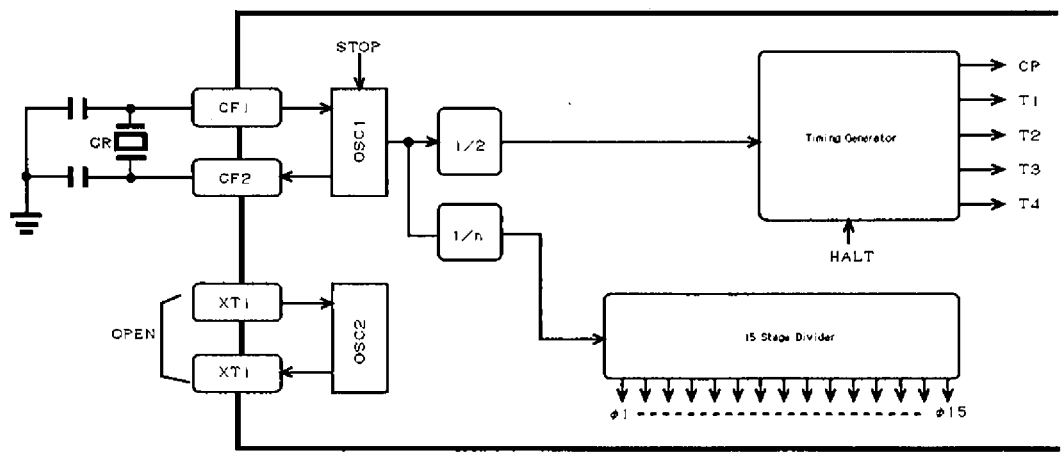


Figure 15. Oscillator configuration 2

This configuration offers the same features as the combined oscillator option with the exception that stopping the ceramic resonator oscillator also stops program execution.

Input port LOW-level latching

Ports S and M have a LOW-level input latching transistor mask option as shown in figure 16.

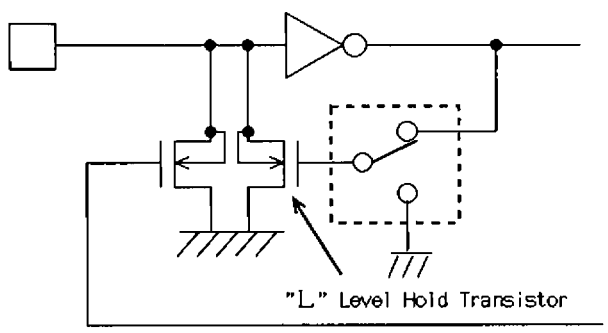


Figure 16. Input latching transistors

Remote control carrier generator

The remote control carrier generator circuitry is shown in figure 17.

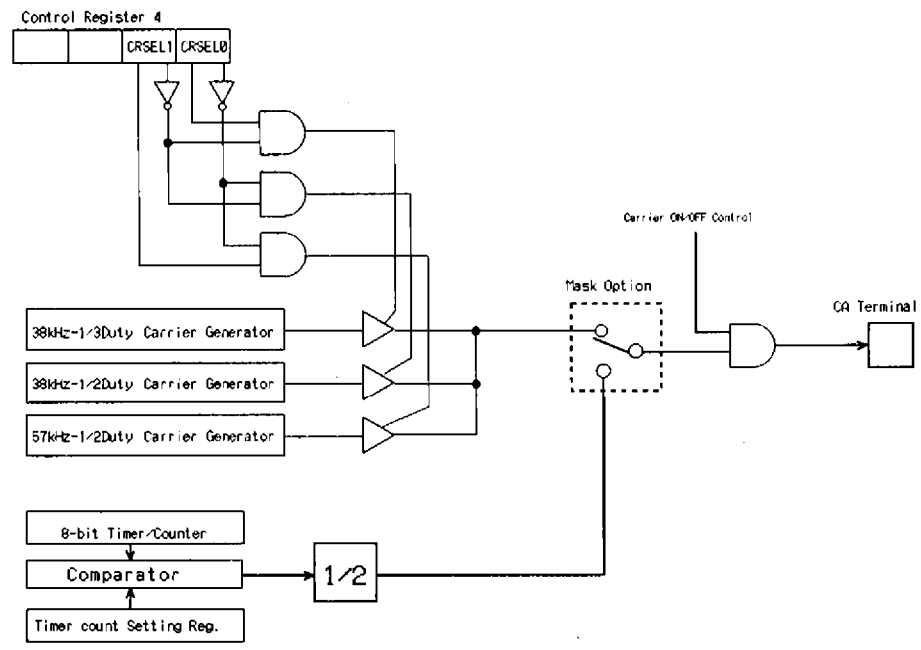


Figure 17. Carrier generator circuit

The carrier waveform can be either software selectable from one of the three fixed waveforms 38 kHz with 1/3 duty, 38 kHz with 1/2 duty and 57 kHz with 1/2 duty-or programmable using the overflow from the 8-bit timer.

LCD drive method

Any drive method can be selected from the following list.
1. Static drive
2. 1/2 bias, 1/2 duty
3. 1/2 bias, 1/3 duty
4. 1/2 bias, 1/4 duty
5. 1/3 bias, 1/3 duty
6. 1/3 bias, 1/4 duty

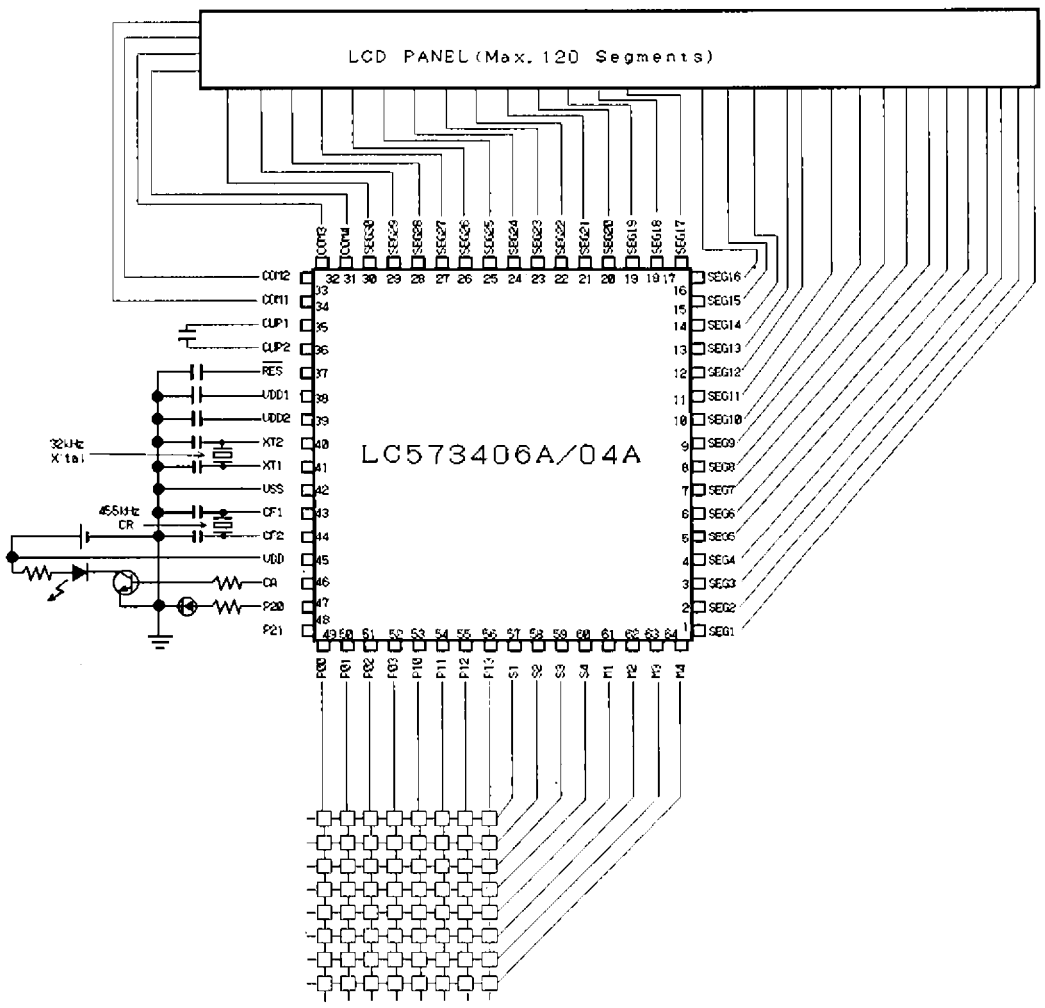
OPERATING INFORMATION

Reset

The LC573404A/LC573406A can be reset by taking $\overline{RES}$ LOW or S1 to S4 HIGH.
When the LC573404A/LC573406A is reset, the following take place.

- The pull-down resistors of ports S and M are enabled.
- CA outputs a 38 kHz, ⅓-duty signal.
- All LCD segments and commons turn ON, and static drive is selected.
- Segment outputs configured as normal p-channel open-drain outputs go HIGH

TYPICAL APPLICATION



INSTRUCTION SET

The instruction set uses the following abbreviations and symbols.

AC:	Accumulator	ACn:	Accumulator bit n
CF:	Carry flag	DP :	Data pointer
DPL:	Data pointer low nibble	DPH:	Data pointer high nibble
EDP:	Data pointer save register	EDPL:	Data pointer save register low nibble
EDPH:	Data pointer save register high nibble	SP:	Strobe pointer
TREG:	Temporary register	SCFn:	Start condition flag n
CTLn:	Control register n	L(SP):	LCD latch specified by SP
HEFn:	HALT cancel inhibit flag n	ROM:	ROM data
CFCN:	Ceramic resonator oscillator control flag	M:	Memory
M(DP):	Memory addressed by DP	[M(DP)]:	Contents of memory addressed by DP
PC:	Program counter	PCn:	Program counter bit n
PAGE:	Page latch	STSn:	Status register n
[P( )]:	Contents of port n	X:	Immediate data
Xn:	Immediate data bit n	PDF:	Input port pull-down flag
SFR:	Special function register	(SFR):	Contents of special function register
CSTF:	Chrono start flag.	SPC:	Strobe pointer control bit
CCF:	Carrier output control flag	( ):	Contents
[ ]:	Contents	$\overline{( )}$:	Complement of contents
$\overline{[\ ]}$:	Complement of contents	ϕn:	Output from stage n of the 15-stage divider
+:	Logical OR	+ :	Logical exclusive-OR
· :	Logical AND	←:	Transfer direction or result

The special function registers are abbreviated as follows.

TCON:	Timer control register	TLOW:	Timer/counter register low byte
THIGH:	Timer/counter register high byte	CTL4:	Control register 4
P0:	Port P0	P1:	Port P1
P2:	Port P2		

Mnemonic	Instruction code	Operation	Bytes	Cycles	Description	Flags
	Accumulator					
TAAT	0 0 0 0 0 0 0 1	AC, TREG←ROM	1	2	Transfers the data from the memory location in the current page, pointed to by the lower 8 bits of PC, to the accumulator and to TREG.	
MTR	0 0 0 1 0 0 1 0	M(DP)←TREG	1	1	Stores the contents of TREG in the memory location pointed to by DP.	
ASR0	0 0 0 1 1 0 0 0	$AC_n \leftarrow AC_{n+1}$, $AC_3 \leftarrow 0$	1	1	Shifts the contents of the accumulator right and enters 0 into the msb.	
ASR1	0 0 0 1 1 0 0 1	$AC_n \leftarrow AC_{n+1}$, $AC_3 \leftarrow 1$	1	1	Shifts the contents of the accumulator right and enters 1 into the msb.	
ASL0	0 0 0 1 1 0 1 0	$AC_n \leftarrow AC_{n-1}$, $AC_0 \leftarrow 0$	1	1	Shifts the contents of the accumulator left and enters 0 into the lsb.	
ASL1	0 0 0 1 1 0 1 1	$AC_n \leftarrow AC_{n-1}$, $AC_0 \leftarrow 1$	1	1	Shifts the contents of the accumulator left and enters 1 into the lsb.	
INC	1 0 0 1 1 0 0 0	AC, M(DP)←M(DP)+1	1	1	Increments the contents of M(DP) and stores it in the accumulator and in M(DP).	
DEC	1 0 0 1 1 0 0 1	AC, M(DP)←M(DP)-1	1	1	Decrements the contents of M(DP) and stores it in the accumulator and in M(DP).	
	Arithmetic					
ADC	1 0 0 0 0 0 0 0	AC←(AC)+[M(DP)]+CF	1	1	Adds the contents of the accumulator to M(DP) with carry and stores the result in the accumulator.	CF
ADC*	1 0 0 0 1 0 0 0	AC, M(DP)←(AC)+[M(DP)]+CF	1	1	Adds the contents of the accumulator to M(DP) with carry and stores the result in the accumulator and M(DP).	CF
ADCI X	1 0 0 1 0 0 0 0 - - - - $X_3X_2X_1X_0$	AC←(AC)+X+CF	2	2	Adds the contents of the accumulator to the immediate data with carry and stores the result in the accumulator.	CF

Mnemonic	Instruction code	Operation	Bytes	Cycles	Description	Flags
SBC	1 0 0 0 0 0 0 1	AC←(AC)+[$\overline{M(DP)}$]+CF	1	1	Subtracts the contents of M(DP) from the accumulator with carry and stores the result in the accumulator.	CF
SBC*	1 0 0 0 1 0 0 1	AC, M(DP)←(AC)+[$\overline{M(DP)}$]+CF	1	1	Subtracts the contents of M(DP) from the accumulator with carry and stores the result in the accumulator and M(DP).	CF
SBCI X	1 0 0 1 0 0 0 1 - - - - $X_3X_2X_1X_0$	AC←(AC)+$\overline{X}$+CF	2	2	Subtracts the immediate data from the accumulator with carry and stores the result in the accumulator.	CF
ADD	1 0 0 0 0 0 1 0	AC←(AC)+[M(DP)]	1	1	Adds the contents of the accumulator to the contents of M(DP) and stores the result in the accumulator.	CF
ADD*	1 0 0 0 1 0 1 0	AC, M(DP)←(AC)+[M(DP)]	1	1	Adds the contents of the accumulator to the contents of M(DP) and stores the result in the accumulator and M(DP).	CF
ADDI X	1 0 0 1 0 0 1 0 - - - - $X_3X_2X_1X_0$	AC←(AC)+X	2	2	Adds the contents of the accumulator to the immediate data and stores the result in the accumulator.	CF
SUB	1 0 0 0 0 0 1 1	AC←(AC)+[$\overline{M(DP)}$]+1	1	1	Subtracts the contents of M(DP) from the accumulator and stores the result in the accumulator.	CF
SBC*	1 0 0 0 1 0 1 1	AC, M(DP)←(AC)+[$\overline{M(DP)}$]+1	1	1	Subtracts the contents of M(DP) from the accumulator and stores the result in the accumulator and M(DP).	CF
SBCI X	1 0 0 1 0 0 1 1 - - - - $X_3X_2X_1X_0$	AC←(AC)+$\overline{X}$+1	2	2	Subtracts the immediate data from the accumulator and stores the result in the accumulator.	CF
ADN	1 0 0 0 0 1 0 0	AC←(AC)+[M(DP)]	1	1	Adds the contents of the accumulator to the contents of M(DP) and stores the result in the accumulator.	
ADN*	1 0 0 0 1 1 0 0	AC, M(DP)←(AC)+[M(DP)]	1	1	Adds the contents of the accumulator to the contents of M(DP) and stores the result in the accumulator and M(DP).	
ADNI X	1 0 0 1 0 1 0 0 - - - - $X_3X_2X_1X_0$	AC←(AC)+X	2	2	Adds the contents of the accumulator to the immediate data and stores the result in the accumulator.	
	Logical					
AND	1 0 0 0 0 1 0 1	AC←(AC)∧[M(DP)]	1	1	Takes the logical AND of the contents of the accumulator and the contents of M(DP) and stores the result in the accumulator.	
AND*	1 0 0 0 1 1 0 1	AC, M(DP)←(AC)∧[M(DP)]	1	1	Takes the logical AND of the contents of the accumulator and the contents of M(DP) and stores the result in the accumulator and in M(DP).	
ANDI X	1 0 0 1 0 1 0 1 - - - - $X_3X_2X_1X_0$	AC←(AC)∧X	2	2	Takes the logical AND of the contents of the accumulator and the immediate data and stores the result in the accumulator.	
EOR	1 0 0 0 0 1 1 0	AC←(AC)⊽[M(DP)]	1	1	Takes the logical exclusive-OR of the contents of the accumulator and the contents of M(DP) and stores the result in the accumulator.	
EOR*	1 0 0 0 1 1 1 0	AC, M(DP)←(AC)⊽[M(DP)]	1	1	Takes the logical exclusive-OR of the contents of the accumulator and the contents of M(DP) and stores the result in the accumulator and in M(DP).	
EORI X	1 0 0 1 0 1 1 0 - - - - $X_3X_2X_1X_0$	AC←(AC)⊽X	2	2	Takes the logical exclusive-OR of the contents of the accumulator and the immediate data and stores the result in the accumulator.	
OR	1 0 0 0 0 1 1 1	AC←(AC)∨[M(DP)]	1	1	Takes the logical OR of the contents of M(DP) and the accumulator and stores the result in the accumulator.	
OR*	1 0 0 0 1 1 1 1	AC, M(DP)←(AC)∨[M(DP)]	1	1	Takes the logical OR of the contents of M(DP) and the accumulator and stores the result in the accumulator and in M(DP).	
ORI X	1 0 0 1 0 1 1 1 - - - - $X_3X_2X_1X_0$	AC←(AC)∨X	2	2	Takes the logical OR of the contents of the accumulator and the immediate data and stores the result in the accumulator.	

Mnemonic	Instructuion code	Operation	Bytes	Cycles	Description	Flags
	Data pointer					
SDPL	0 0 0 1 1 1 0 0	DPL←(AC)	1	1	Stores the contents of the accumulator in DPL.	
SDPH	0 0 0 1 1 1 0 1	DPH←(AC)	1	1	Stores the contents of the accumulator in DPH.	
LDPL	1 1 1 1 1 1 0 1	AC←(DPL)	1	1	Loads the contents of DPL into the accumulator.	
LDPH	1 1 1 1 1 1 1 0	AC←(DPH)	1	1	Loads the contents of DPH into the accumulator.	
MDPL X	1 0 1 1 $X_3X_2X_1X_0$	DPL←X	1	1	Stores the immediate data in DPL.	
MDPH X	1 1 0 0 $X_3X_2X_1X_0$	DPH←X	1	1	Stores the immediate data in DPH.	
EDPL	0 0 0 1 1 1 1 0	(DPL) ⟷ (EDPL)	1	1	Swaps the contents of DPL and EDPL.	
EDPH	0 0 0 1 1 1 1 1	(DPH) ⟷ (EDPH)	1	1	Swaps the contents of DPH and EDPH.	
IDPL	1 0 0 1 1 0 1 0	DPL←(DPL)+1	1	1	Increments the contents of DPL and stores the result in DPL.	
IDPH	1 0 0 1 1 1 0 0	DPH←(DPH)+1	1	1	Increments the contents of DPH and stores the result in DPH.	
DDPL	1 0 0 1 1 0 1 1	DPL←(DPL)-1	1	1	Decrements the contents of DPL and stores the result in DPL.	
DDPH	1 0 0 1 1 1 0 1	DPH←(DPH)-1	1	1	Decrements the contents of DPH and stores the result in DPH.	
SSP	1 0 1 0 1 1 1 0	SP←(AC)	1	1	Stores the contents of the accumulator in SP.	
LSP	1 0 1 0 1 0 1 0	AC←(SP)	1	1	Loads the contents of SP into the accumulator.	
MSP X	1 1 1 0 $X_3X_2X_1X_0$	SP←X	1	1	Stores the immediate data in SP.	
ISP	1 0 0 1 1 1 1 0	SP←(SP)+1	1	1	Increments the contents of SP and stores the result in SP.	
DSP	1 0 0 1 1 1 1 1	SP←(SP)-1	1	1	Decrements the contents of SP and stores the result in SP.	
	Flag					
LHLT	1 0 1 0 1 0 1 1	AC←(STS2), STS2←0	1	1	Loads the contents of STS2 into the accumulator and clears STS2.	SCF1～4
L500	1 0 1 0 1 1 0 0	AC←(STS1), SCF0←0	1	1	Loads the contents of STS1 into the accumulator and clears SCF0.	SCF0
CSP	0 0 0 0 0 1 0 0	CSTF←0	1	1	Clears CSTF.	CSTF
CST	0 0 0 0 0 1 0 1	CSTF←1	1	1	Sets CSTF.	CSTF
RC5	0 0 0 0 0 1 1 0	HEF0←0	1	1	Clears HEF0 to prevent HALT-mode cancellation when the divider overflows.	HEF0
SC5	0 0 0 0 0 1 1 1	HEF0←1	1	1	Sets HEF0 to enable HALT-mode cancellation when the divider overflows.	HEF0
RCF	1 1 1 1 0 0 0 0	CF←0	1	1	Clears CF.	CF
SCF	1 1 1 1 0 0 0 1	CF←1	1	1	Sets CF.	CF
	Data transfer					
LDA	1 0 1 0 1 0 0 1	AC←[M(DP)]	1	1	Loads the contents of M(DP) into the accumulator.	
STA	1 0 1 0 1 1 0 0	M(DP)←(AC)	1	1	Stores the contents of the accumulator in M(DP).	CF
LDI X	0 0 1 1 $X_3X_2X_1X_0$	AC←X	1	1	Loads the immediate data into the accumulator.	
MVI X	0 0 1 0 $X_3X_2X_1X_0$	M(DP)←X	1	1	Loads the immediate data into M(DP).	

Mnemo-nic	Instruction code	Operation	Bytes	Cycles	Description	Flag
	CPU control					
HALT	0 0 0 0 0 0 0 0	CPU halted	1	1	Stops the CPU. HALT mode is cancelled by the interaction of the SIC X and SC5 commands.	
					Stores the immediate data in CTL2. The lower 4 bits of the instruction code control the HALT mode cancellation. The functions of these bits, X0 to X3, are described below.	
					X_0: This bit sets HEF1, cancelling HALT mode with the divider overflow signal.	
					X_1: This bit sets HEF2, cancelling HALT mode with a rising edge on port S.	
					X_2: This bit sets HEF3, cancelling HALT mode with a rising edge on port M.	
					X_3: This bit sets HEF4, cancelling HALT mode with the 10 Hz timing pulse.	
NOP	1 1 1 1 1 1 1 1	NO OPERATION.	1	1	No Operation.	
	Input/output					
IPS	1 0 1 0 1 1 1 1	AC←[P(S)]	1	1	Loads the input data on port S into the accumulator.	
IPM	1 0 1 0 1 0 0 0	AC←[P(M)]	1	1	Loads the input data on port M into the accumulator.	
SPDR X	1 1 1 1 0 1X_1X_0	PDF←X	1	1	Stores the immediate data in PDF. PDF controls the internal pull-down resistors on ports S and M. The functions of bits X0 and X1 are described below.	PDF
					X0: The pull-down resistors on port S are enabled when X0 is set and disabled when X0 is cleared.	
					X1: The pull-down resistors on port M are enabled when X1 is set and disabled when X0 is cleared.	
OUT	1 1 1 1 1 1 0 0	When SPC = 0 and SP = 0H to CH, EH or FH, L(SP) ←(AC) and [M(DP)]	1	1	Transfers the contents of M(DP) and the accumulator to the LCD driver specified by SP.	
		When SPC = 0 and SP = DH, CTL3 ← (AC)			Stores the contents of the accumulator in CTL3.	CFCF CCF
		When SPC = 1, SFR ←(AC)			Stores the contents of the accumulator in SFR.	
TWRT	0 0 0 0 0 0 1 0	When SPC = 0 and SP = 0H to CH, EH or FH, L(SP) ← ROM	1	2	Transfers the lower eight bits of PC in the current page to the accumulator, and the ROM data, pointed to by the accumulator and M(DP), to the LCD driver specified by SP.	
		When SPC = 0 and SP = DH, CTL3 ←(AC)			Transfers the lower eight bits of PC in the current page to the accumulator, and the upper eight bits of the ROM data, pointed to by the accumulator and M(DP), to CTL3.	CFCF CCF
		When SPC = 1, SFR ← (AC)			Transfers the lower eight bits of PC in the current page to the accumulator, and the upper four or eight bits of the ROM data, pointed to by the accumulator and M(DP), to SFR.	
IN	0 0 0 1 0 1 1 1	When SPC = 0 and SP = 0H to CH, EH or FH, this instruction is invalid.	1	1	The execution of the IN comand when SPC = 1 and SP = 0H to CH, EH or FH will result in the device malfunctioning and so should not be used.	
		When SPC = 0, and SP = DH, AC ← (STS3)			Loads the contents of STS3 into the accumulator.	
		When SPC = 1, AC ← (SFR)			Loads the contents of SFR into the accumulator.	
	Branching/subroutine					

Mnemonic	Instruction code	Operation	Bytes	Cycles	Description	Flags
JMP X	0 0 0 0 $1X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	$(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	Transfers the data specified by X0 to X10 to the program counter and makes an unconditional jump.	
BAB0 X	0 1 0 0 $1X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if AC_0=1 THEN $(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	If bit 0 of the accumulator is set, transfers the data specified by X0 to X10 to the program counter and jumps to that address. If the bit is not set, the program counter is incremented.	
BAB1 X	0 1 0 1 $1X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if AC_1=1 THEN $(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	If bit 1 of the accumulator is set, transfers the data specified by X0 to X10 to the program counter and jumps to that address. If the bit is not set, the program counter is incremented.	
BAB2 X	0 1 1 0 $1X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if AC_2=1 THEN $(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	If bit 2 of the accumulator is set, transfers the data specified by X0 to X10 to the program counter and jumps to that address. If the bit is not set, the program counter is incremented.	
BAB3 X	0 1 1 1 $1X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if AC_3=1 THEN $(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	If bit 3 of the accumulator is set, transfers the data specified by X0 to X10 to the program counter and jumps to that address. If the bit is not set, the program counter is incremented.	
BAZ X	0 1 0 0 $0X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if AC=0 THEN $(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	If the accumulator is zero, transfers the data specified by X0 to X10 to the program counter and jumps to that adress. If the accumulator is not zero, the program counter is incremented.	
BANZ X	0 1 0 1 $0X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if AC≠0 THEN $(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	If the accumulator is not zero, transfers the data specified by X0 to X10 to the program counter and jumps to that address. If the accumulator is zero, the program counter is incremented.	
BCNH X	0 1 1 0 $0X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if CF≠1 THEN $(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	If CF is cleared, transfers the data specified by X0 to X10 to the program counter and jumps made to that address. If CF is set, the program counter is incremented.	
BCH X	0 1 1 1 $0X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	if CF=1 THEN $(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	If CF is set, transfers the data specified by X0 to X10 to the program counter and jumps to that address. If CF is cleared, the program counter is incremented.	
PAGE	0 0 0 1 0 0 0 1	PAGE←[M(DP)]	1	1	Transfers the contents of M(DP) to the data page latch.	
JMP*	0 0 0 1 0 0 0 0	$PC_{10}\sim PC_8\leftarrow$(PAGE) $PC_7\sim PC_4\leftarrow$(AC) $PC_3\sim PC_0\leftarrow$[M(DP)]	1	1	Transfers the data from the accumulator, page latch and the contents of M(DP) to the program counter and jumps to that address.	
ROM0	1 1 0 0 1 0 0 0 0 0 1 0 0 0 0 0	$PC_{12}\sim PC_{11}\leftarrow 0$	2	2	Selects ROM bank 0.	
ROM1	1 1 0 0 1 0 0 0 0 0 1 0 0 0 0 1	$PC_{12}\sim PC_{11}\leftarrow 1$	2	2	Selects ROM bank 1.	
ROM2	1 1 0 0 1 0 0 0 0 0 1 0 0 0 1 0	$PC_{12}\sim PC_{11}\leftarrow 2$	2	2	Selects ROM bank 2.	
JSR X	0 0 0 0 $1X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	STACK←(PC)+2 $(PC_{10}\sim PC_0)\leftarrow X_{10}\sim X_0$	2	2	Pushes PC + 2 onto the stack, transfers the data specified by X0 to X10 to the program counter and calls the subroutine at that address.	
RTS	0 0 0 1 0 0 1 1	PC←(STACK)	1	1	Recovers the program counter from the stack and returns from the subroutine.	
	Miscellaneous					
SPC0	1 1 0 0 1 0 0 1 0 0 1 0 0 0 0 0	SPC←0	2	2	Clears the SPC flag.	SPC
SPC1	1 1 0 0 1 0 0 1 0 0 1 0 0 0 0 1	SPC←1	2	2	Sets the SPC flag.	SPC
CSEC	1 1 1 1 1 0 1 1	$\phi 11\sim\phi 15\leftarrow 0$	1	1	Clears the upper four bits of the programmable divider and flags SCF0 and SCF4.	SCF0 SCF4

Instruction Set Summary

Lower / Upper	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	HALT	TAAT	TWRT	-	CSP	CST	RC5	SC5	JMP X							
1	JMP*	PAGE	MTR	RTS	-	-	-	IN	ASR0	ASR1	ASL0	ASL1	SDPL	SDPH	EDPL	EDPH
2	MVI X															
3	LDI X															
4	BAZ X								BAB0 X							
5	BANZ X								BAB1 X							
6	BCNH X								BAB2 X							
7	BCH X								BAB3 X							
8	ADC	SBC	ADD	SUB	ADN	AND	EOR	OR	ADC*	SBC*	ADD*	SUB*	ADN*	AND*	EOR*	OR*
9	ADCI	SBCI	ADDI	SUBI	ADNI	ANDI	EORI	ORI	INC	DEC	IDPL	DDPL	IDPH	DDPH	ISP	DSP
A	JSR X								IPM	LDA	LSP	LHLT	L500	STA	SSP	IPS
B	MDPL X															
C	MDPH X								ROMX	SPCX						
D	SIC X															
E	MSP X															
F	RCF	SCF	NOP	NOP	SPDR X				-	-	-	CSEC	OUT	LDPL	LDPH	NOP

XXX :1 Byte, 1 Cycle command

XXX :2 Byte, 2 Cycle command

XXX :1 Byte, 2 Cycle command

ROMX is the first byte of the ROM0(C820H), ROM1(C821H) and ROM2(C822H) commands.

SPCX is the first byte of the SPC0(C920H) and SPC1(C921H) commands.