Ordering number:ENN4789

CMOS IC

LC7074, 7074M

Synchronous Error Correction IC for RDS Applications

Overview

The LC7074 and the LC7074M are ICs for the RDS (radio data system) implemented by the EBU (European Broadcasting Union) and the RDBS (radio broadcast data system) implemented by the NRSC (National Radio System Committee) in the USA.

RDS and RBDS are standards that allow data to be broadcast multiplexed with other FM broadcasts. When combined with an IC in the LA2230 series, the LC7074/M synchronizes with data multiplexed in an FM broadcast and detects and corrects errors in that data. The synchronized data is output as a serial signal which can then be decoded and processed on the system control microprocessor.

Functions

- Group synchronization.
  RDS group synchronization.
  MMBS/RDS group synchronization.
- Error detection and correction.
- Error detection function enable/disable selection.
- Serial data output.
- Serial data clock polarity selection.
- Data block start signal output.

Features

- System that decode, synchronize and detect and correct errors can easily be constructed by combining the LC7074/M with an LA2230 series product.
- Reduces overhead in the microprocessor that decodes and processes the RDS or MMBS/RDS data.

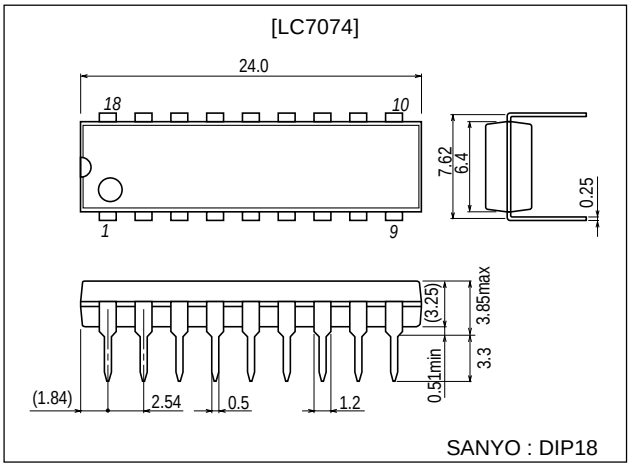
Product-Package Relationship

Product No.	Package
LC7074	DIP18
LC7074M	MFP18

Package Dimensions

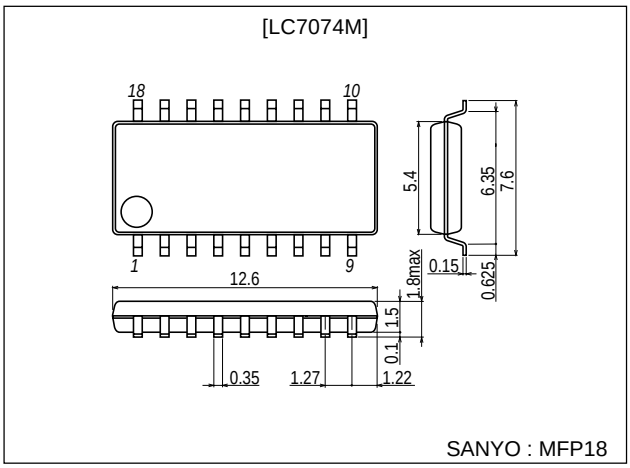
unit:mm

3007B-DIP18



unit:mm

3095-MFP18



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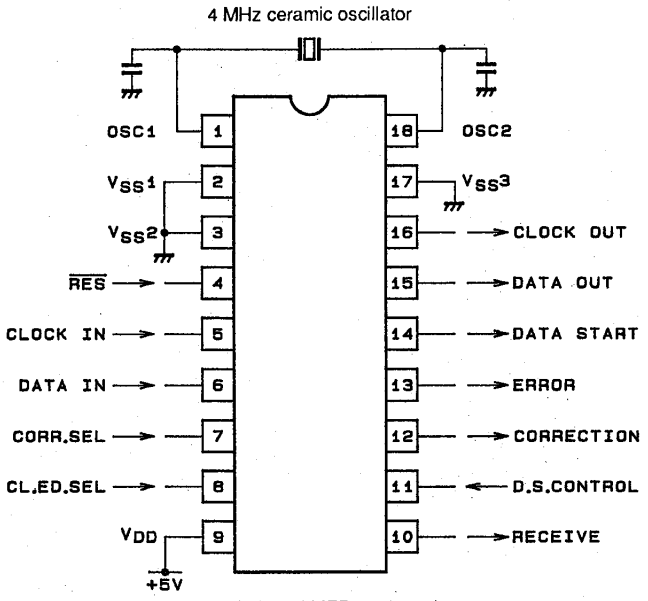
Pin Assignment



The DIP and MFP product pin assignments are identical.

The LC7070 Series

This section describes the differences between the different products in the LC7070 series

Usage Notes

This basic functions, including the pin functions and I/O timing, are identical in all products in the series. However, some pin circuits and function operation details differ.

- LC7070NM…While the LC7074M is pin compatible with this product, the circuit type of the three output pins differs as shown in table, Package and Output Driver Type Comparison. These products can be interchanged to match the output interface. However, since the data output method following synchronization detection differs as shown in table, Comparison of Functional Differences, care is required in writing programs that receive, decode and process the output data for the control microprocessor.
- LC7070N……While the LC7074 is pin compatible with this product, the circuit type of the three output pins differs as shown in table, Package and Output Driver Type Comparison. These products can be interchanged to match the output interface. However, since the data output method following synchronization detection differs as shown in table, Comparison of Functional Differences, care is required in writing programs that receive, decode and process the output data for the control microprocessor.
- LC7071NM…The LC7074M is pin compatible with this product, and the pin circuit types, pin functions, and signal timings are identical. In principle, these products are interchangeable. However, since the data output method following synchronization detection differs as shown in table, Comparison of Functional Differences, care is required in writing programs that receive, decode and process the output data for the control microprocessor.
- LC7073……The LC7074 is pin compatible with this product, and the pin circuit types, pin functions, and signal timings are identical. Furthermore, the synchronization detection method and the post-synchronization data output method are also identical. In principle, these products are interchangeable. However, since these products handle the block offset words E and F differently, and also handle MMBS/RDS data differently as shown in table, Comparison of Functional Differences, care is required in writing programs that receive, decode and process the output data for the control microprocessor.
- LC7073M……The LC7074M is pin compatible with this product, and the pin circuit types, pin functions, and signal timings are identical. Furthermore, the synchronization detection method and the post-synchronization data output method are also identical. In principle, these products are interchangeable. However, since these products handle the block offset words E and F differently, and also handle MMBS/RDS data differently as shown in table, Comparison of Functional Differences, care is required in writing programs that receive, decode and process the output data for the control microprocessor.

Package and Output Driver Type Comparison

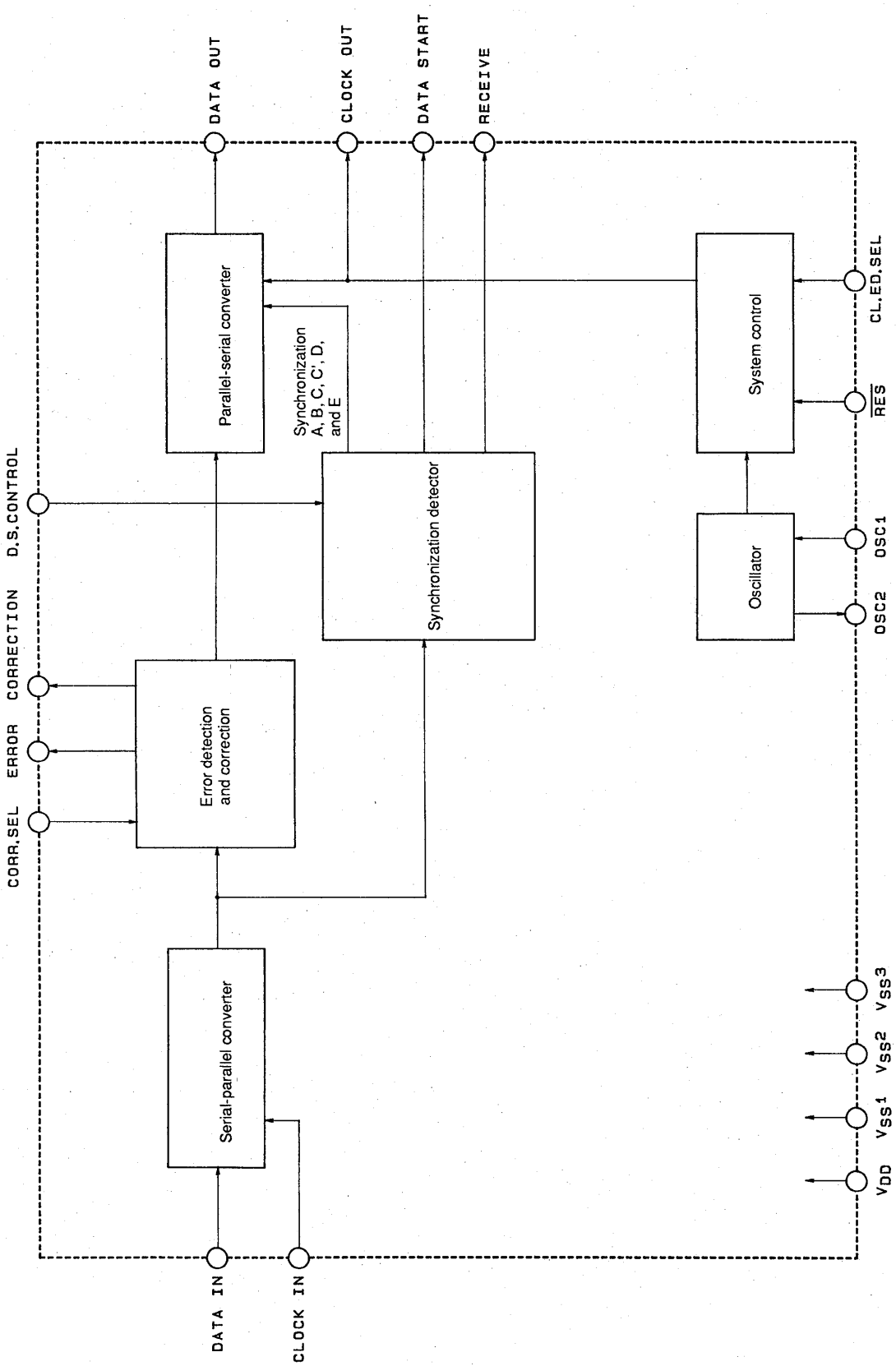
Product No.	Package	Output driver type difference*	Function
LC7070N	DIP18	Open drain type	Identical functions
LC7070NM	MFP18		
LC7071NM	MFP18	Pull-up MOS transistor (CMOS type)	
LC7073	DIP18	Pull-up MOS transistor (CMOS type)	See table, Comparison of Functional Differences.
LC7073M	MFP18		
LC7074	DIP18	Pull-up MOS transistor (CMOS type)	See table, Comparison of Functional Differences.
LC7074M	MFP18		

Note: *Only applies to the three pins DATA START, DATA OUT and CLOCK OUT.

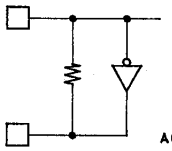
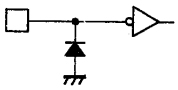
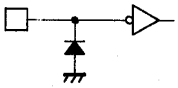
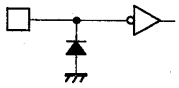
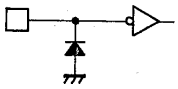
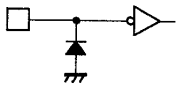
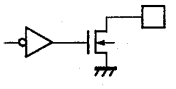
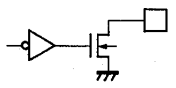
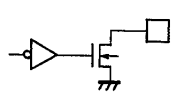
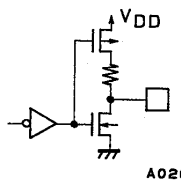
Comparison of Functional Differences

Item	LC7070N LC7070NM LC7071NM	LC7073 LC7073M	LC7074 LC7074M
Offset word E Offset word F	These are taken to be offset words and a group synchronization detection operation is performed.	These are not seen as offset words. Only offset words A, B, C, C' and D are detected.	Offset words A, B, C, C', D and E are detected. Offset word F is not detected.
All zero data (corresponding to offset E)	All zero data is taken to be an offset word E block. Accordingly, an offset word E block synchronization operation is performed.	All zero data is not seen as being an offset word E block. Rather, all zero data is taken to mean that there is no input, and synchronization detection is not performed. If all zero data is input, these products decide that data input has stopped, and they stop outputting data and enter the pull-out sequence.	All zero data is seen as an offset word E block. Accordingly, an offset word E block synchronization operation is performed.
MMBS/RDS compound data	For the transition from an RDS group (ABCD) to an MMBS group (EEEE) or the reverse transition, these are taken to be the pull-out and resynchronization sequences. During transitions, data errors can occur and data output can be interrupted.	Since these products do not synchronize on an offset word E block, each time an RDS group is inserted in an MMBS group, they repeat the pull-out and resynchronization sequences.	MMBS/RDS data is correctly output with no pull-out and no errors.
Synchronization detection method	Synchronization is achieved when the offset words in five out of 12 blocks are detected in the correct order.	Synchronization is achieved when the offset words in two out of three blocks are detected in the correct order.	
Post-synchronization detection data output	Data output starts with the data from the first block (the offset word A block) in the group following the group for which synchronization detection was completed.	When synchronization detection completes with an offset word A block, output starts with the data in the second block (the offset word B block) from the same group. When synchronization detection completes with an offset word B, C or D block, output starts with the data in the first block (the offset word A block) from the same group.	
Pull-out determination method	When the offset words from five or more consecutive blocks were not detected.		
Error correction	In modes where error correction is enabled, up to five error bits are corrected for distances of 5 bits or less.		

Block Diagram



Pin Functions

Pin	I/O	Internal equivalent circuit	Function	Value at reset
V_{DD}, V_{SS1} V_{SS2}, V_{SS3}			Power supply	
OSC1 OSC2	I O		Clock oscillator Connect the external ceramic oscillator and capacitor at these pins.	
CLOCK IN	I		RDS demodulation clock input Connect to the clock output from the LA2230 series demodulation IC.	
DATA IN	I		RDS demodulation data input Connect to the data output from the LA2230 series demodulation IC.	
CORR.SEL	I		Error correction selection input This pin selects whether the IC corrects errors in the RDS demodulated data. Input=0: No correction performed* Input=1: Error correction performed In modes where error correction is enabled, up to five error bits are corrected for distances of 5 bits or less.	
CL.ED.SEL	I		Serial data clock output polarity selection input Input=0: Serial data output is valid on the rising edge of the output clock. (Data output changes on the falling edge of the clock.) Input=1: Serial data output is valid on the falling edge of the output clock. (Data output changes on the rising edge of the clock.)	
D.S.CONTROL	I		Block data start signal control input Input=0: Output the DATA START signal for all blocks. Input=1: Output the DATA START signal for only the second block.	
RECEIVE	O		RDS data reception in progress output Outputs a low level while serial data is being output following completion of synchronization detection. Outputs a high level at all other times. Open drain output	High level (high impedance)
CORRECTION	O		Error correction operation output Outputs a low level when the serial data output data has been error corrected, or could not be corrected. Outputs a high level (high impedance) when correction is disabled. Open drain output	High level (high impedance)
ERROR	O		Error output Outputs a low level when there were errors in the input data and those errors could not be corrected. Outputs a high level (high impedance) when there were no errors or the errors were corrected. Open drain output	High level (high impedance)
DATA START	O		Serial data output block data start signal The output type is controlled by the D.S.CONTOL input. Pull-up MOS transistor (CMOS) output	High level

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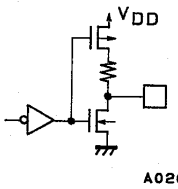
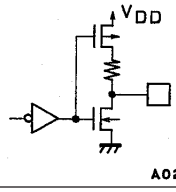
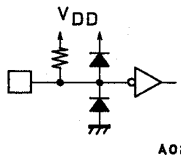
Pin	I/O	Internal equivalent circuit	Function	Value at reset
DATA OUT	O		Serial data output data output Pull-up MOS transistor (CMOS) output	High level
CLOCK OUT	O		Serial data output clock output Pull-up MOS transistor (CMOS) output	High level
$\overline{RES}$	I		Reset input Input a low level pulse with a length of at least 4 clock cycles to reset and restart IC operation. Note that when a 4 MHz oscillator is used, since a single clock cycle is 0.25µs, four clock cycles is 1 µs. Schmitt type input. Built-in pull-up resistor	

Note: *0: Low level input
1: High level input

Specifications

Electrical Characteristics at Ta = 25˚C, V_{SS1}, V_{SS2}, V_{SS3} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD} max	V_{DD}	−0.3 to +7.0	V
Output voltage	V_{O1}	OSC2, DATA START, DATA OUT, CLOCK OUT	−0.3 to V_{DD}+0.3	V
	V_{O2}	RECEIVE, CORRECTION, ERROR	−0.3 to +15	V
Input voltage	V_{I1}	$\overline{RES}$, OSC1: *	−0.3 to V_{DD}+0.3	V
	V_{I2}	CLOCK IN, DATA IN, CORR.SEL, CL.ED.SEL, D.S.CONTROL	−0.3 to +15	V
Output current	I_{O1}	RECEIVE, CORRECTION, ERROR: The output current per pin	20	mA
	I_{O2}	DATA START, DATA OUT, CLOCK OUT: The output current per pin	−2 to +20	mA
	I_O	All output pins: Total value	−14 to +90	mA
Allowable power dissipation	Pd max	DIP package product: Ta=–40 to +85˚C	Up to 250	mW
		MFP package product: Ta=–40 to +85˚C	Up to 150	mW
Operating temperature	Topr		−40 to +85	˚C
Storage temperature	Tstg		−55 to +125	˚C

Note: *When driving the oscillator with the recommended constants shown in figure 1, values up to the oscillation amplitude that occurs are allowed.

Allowable Operating Ranges at Ta = –40 to +85˚C, V_{SS1}, V_{SS2}, V_{SS3} = 0V, V_{DD} = 4.5 to 6.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	V_{DD}	V_{DD}	4.5		6.0	V
Input high-level voltage	V_{IH1}	CLOCK IN, DATA IN, CORR.SEL. CL.ED.SEL, D.S.CONTROL	0.7V_{DD}		13.5	V
	V_{IH2}	$\overline{RES}$	0.8V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL1}	CLOCK IN, DATA IN, CORR.SEL. CL.ED.SEL, D.S.CONTROL	V_{SS}		0.3V_{DD}	V
	V_{IL2}	$\overline{RES}$	V_{SS}		0.25V_{DD}	V
Ceramic oscillator guarantee		OSC1, OSC2: See figure 1	See the ceramic oscillator guaranteed constants table.			

Electrical Characteristics at Ta = –40 to +85˚C, V_{SS1}, V_{SS2}, V_{SS3} = 0V, V_{DD} = 4.5 to 6.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	I_{IH}	CLOCK IN, DATA IN, CORR.SEL, CL.ED.SEL, D.S.CONTROL: V_{IN}=13.5V			5.0	µA
Input low-level current	I_{IL1}	CLOCK IN, DATA IN, CORR.SEL, CL.ED.SEL, D.S.CONTROL: V_{IN}=V_{SS}	–1.0			µA
	I_{IL2}	$\overline{RES}$: V_{IN}=V_{SS}	–45	–10		µA
Output high-level voltage	V_{OH}	DATA START, DATA OUT, CLOCK OUT: I_{OH}=–50µA	V_{DD}–1.2			V
		DATA START, DATA OUT, CLOCK OUT: I_{OH}=–10µA	V_{DD}–0.5			
Output low-level voltage	V_{OL}	RECEIVE, CORRECTION, ERROR, DATA START, DATA OUT, CLOCK OUT: I_{OL}=10mA			1.5	V
		RECEIVE, CORRECTION, ERROR, DATA START, DATA OUT, CLOCK OUT: I_{OL}=1.8mA*1			0.4	
Output off leakage current	I_{OFF}	RECEIVE, CORRECTION, ERROR: V_O=13.5V			5.0	µA
		RECEIVE, CORRECTION, ERROR: V_O=V_{SS}	–1.0			
Hysteresis voltage	V_{HIS}	$\overline{RES}$		0.1V_{DD}		V
Supply current	I_{DD}	V_{DD}: *2		1.5	3.5	mA
Ceramic oscillator stabilization time	t_{CFS}	OSC1, OSC2: See figure 2			10	ms
Reset time	t_{RST}		See figure 3			

Note: 1 When the I_{OL} values for the remaining output pins (when an arbitrary 4 output pins are excluded) are all under 1 mA.

2 Using the oscillator circuit in figure 1, when there is no power dissipation in the output pins, and when the input pins are at the V_{DD} level.

Ceramic Oscillator Guaranteed Constants

4 MHz ceramic oscillator	C1, C2
CSA4. 00MG (Murata Mfg. Co., Ltd.)	30 pF ±10%
KBR4. 0M (Kyocera, Ltd.)	30 pF ±10%

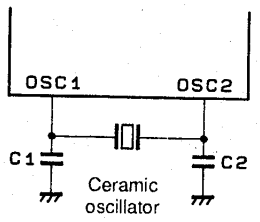


Figure 1. Oscillator Circuit

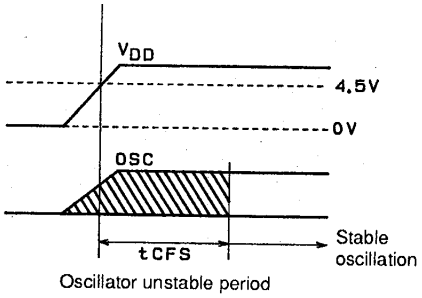
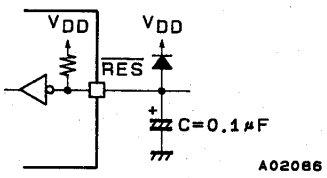
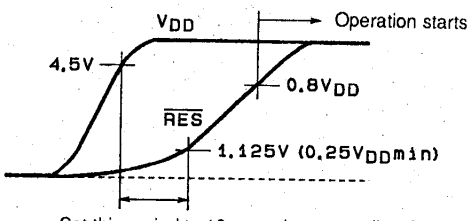


Figure 2. Oscillator Stabilization Period



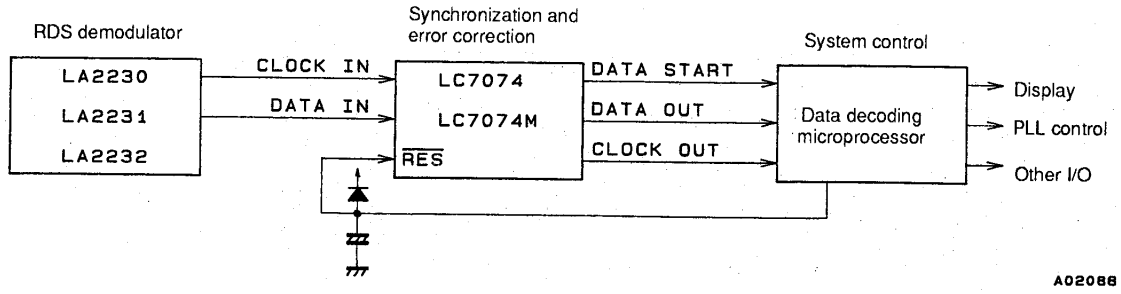
This example shows a simplified reset circuit.
In actual applications, we recommend that the circuit be designed so that the reset signal can be applied from the control microprocessor to handle cases where IC operation becomes unstable due to power supply noise or other causes.



Set this period to 10 ms or longer to allow for the oscillator stabilization period.
10 to 100 ms when C = 0.1 µF.
However, adjust the value of C in application circuits in which the power supply has a slow rise time.

Figure 3. Reset Circuit

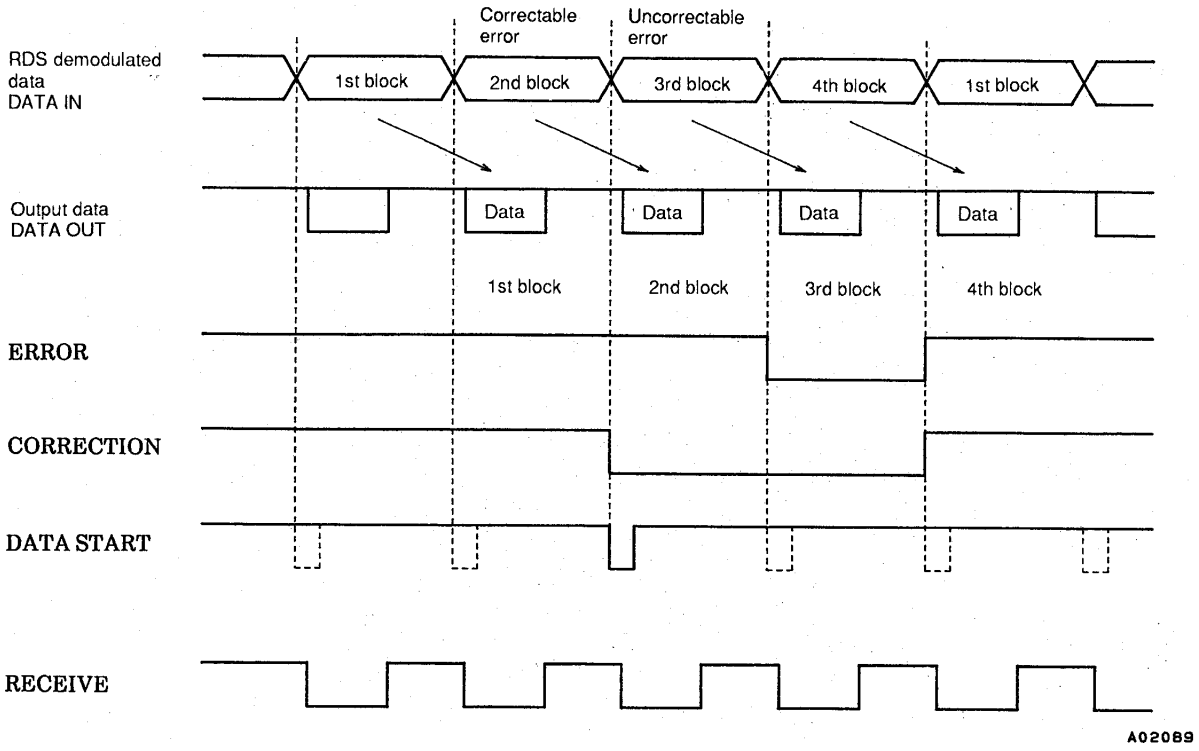
RDS Data Processing System Organization Example



System Organization Example

System Operation

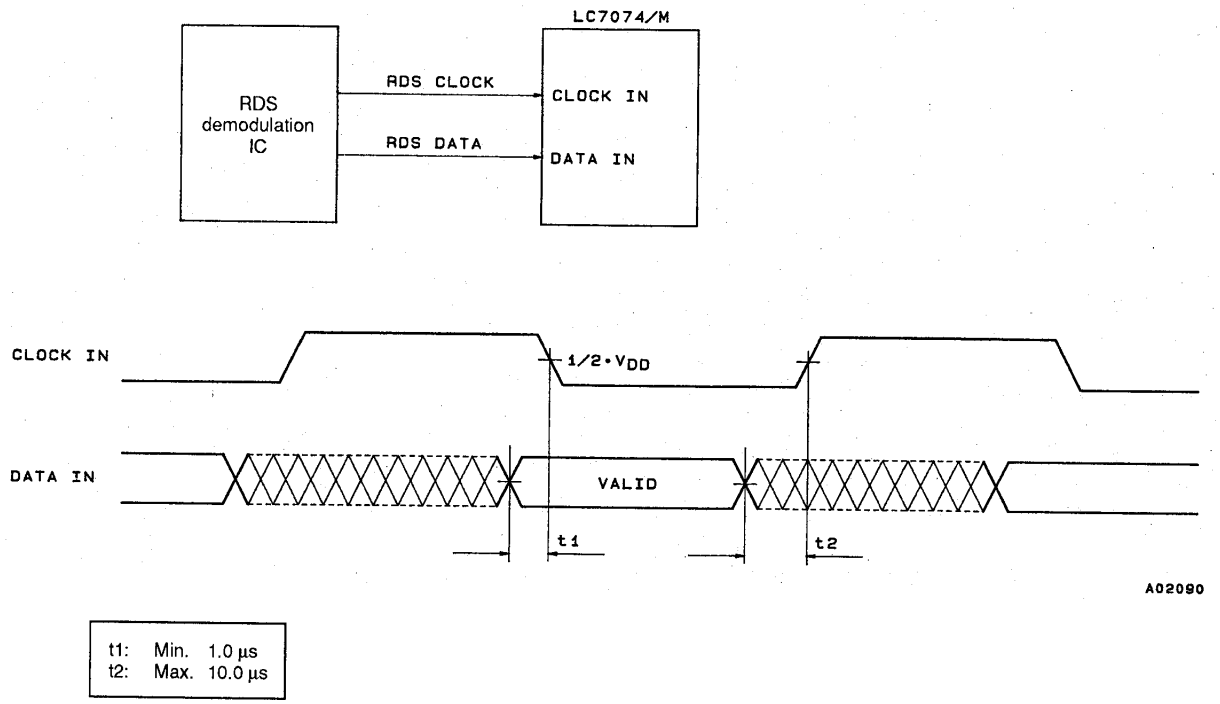
1. Relationship between RDS Demodulated Data (LA2230 series IC output) and LC7074/M Output Data



- The DATA START signal indicated with broken lines is the signal when the D.S.CONTROL input is low level.
- The serial data output (DATA OUT) from the LC7074/M is data that is delayed by one block with respect to the data received from the LA2230 series IC.
- The ERROR and CORRECTION signals are output continuously when consecutive errors are detected.
- The RECEIVE output signal is output only in periods when output data is being output from the DATA OUT pin.

Relationship between the Demodulated Data and the Output Data

2. Input Data Timing



t1: Min. 1.0 µs
t2: Max. 10.0 µs

- Input data is acquired on the falling edge of the input clock.
- Input data must be stable just before and just after the falling edge of the input clock. This means that it is desirable that the input data change state on the rising edge of the input clock.

Input Data Timing

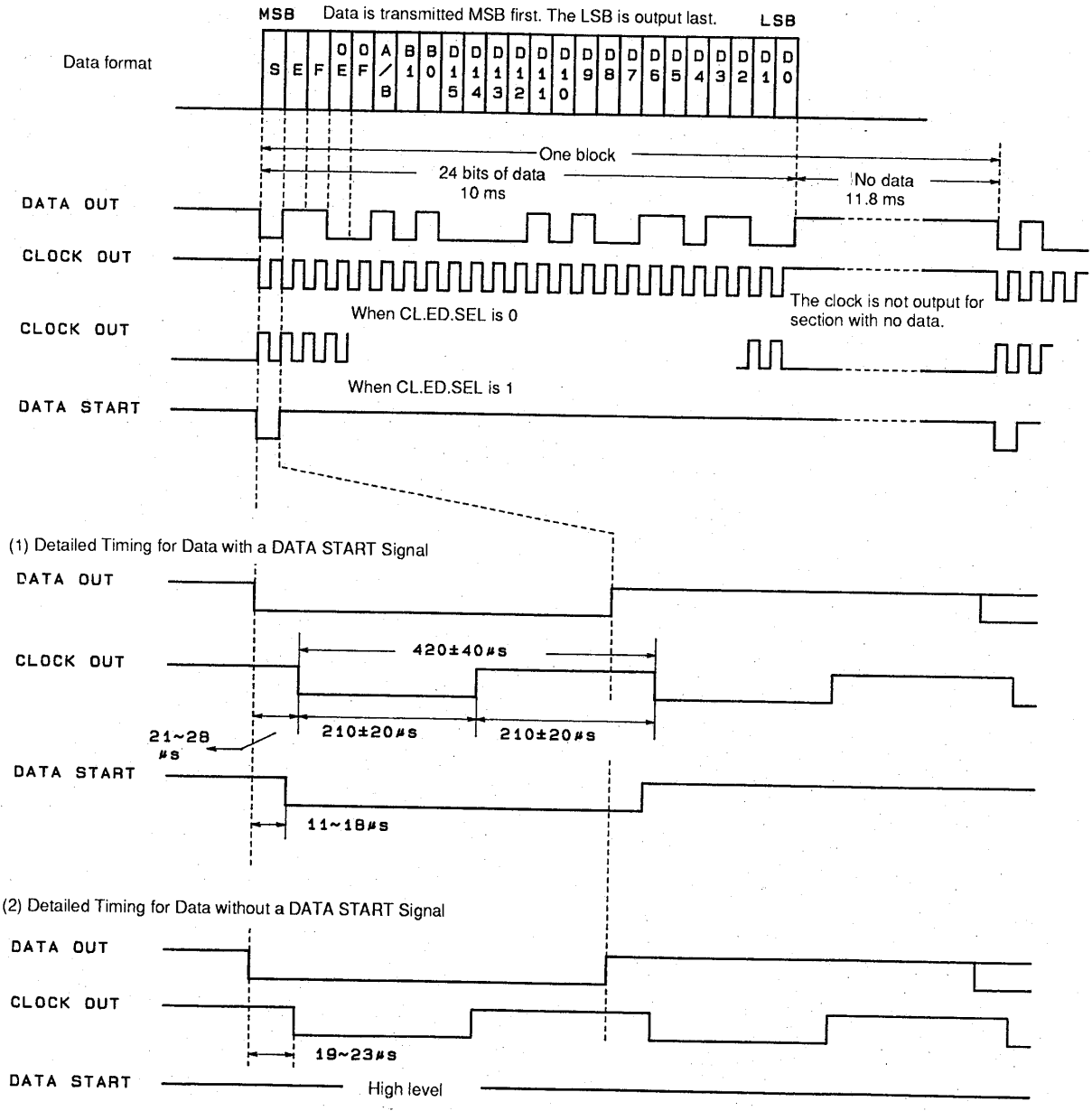
3. Serial Data Output Format and Timing

S : Start bit (always “0”)
E : Error flag } See table
F : Correction flag
OE : Offset E
OF : Offset F (always “0” : reserved for future expansion)
A/B : Group type version 0: Version A
1: Version B
B1, B0 : Block number 00 : First block
01 : Second block
10 : Third block
11 : Fourth block
D0 to D15 : RDS data

E and F Flags

	E	F
No errors	0	0
Errors corrected	0	1
Uncorrectable errors	1	1

Note: When the CORR.SEL input pin is high level.



Serial Data Output Format and Timing

4. Informative Bits in the Serial Data Output

• Error Flag (E) and Correction Flag (F)

The error flag (E) and the correction flag (F) in the serial data output are identical to the ERROR and CORRECTION output pins, except that the logical levels are inverted.
The meaning of the error and correction flags differ slightly depending on the setting that determines whether input data error correction is to be performed (the CORR.SEL pin). The tables below show the relations between the output value combinations of the error and correction flags.

– When the CORR.SEL pin is high: Error correction enabled

	Error flag (E)	Correction flag (F)	ERROR pin	CORRECTION pin
No errors	0	0	1	1
Errors corrected	0	1	1	0
Uncorrectable errors	1	1	0	0

The value combination where E is 1 and F is 0 (or equivalently, where the ERROR pin is 0 and the CORRECTION pin is 1) cannot occur.

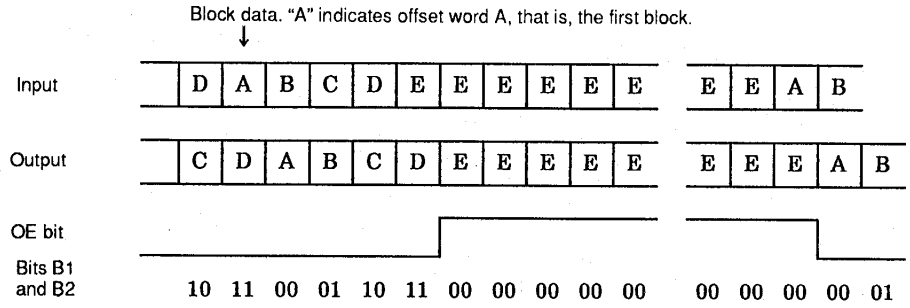
– When the CORR.SEL pin is high: Error correction disabled

	Error flag (E)	Correction flag (F)	ERROR pin	CORRECTION pin
No errors	0	0	1	1
Uncorrectable errors	1	1	0	0

The value combination where E is 1 and F is 0 (or equivalently, where the ERROR pin is 0 and the CORRECTION pin is 1) and where E is 0 and F is 1 (or equivalently, where the ERROR pin is 1 and the CORRECTION pin is 0) cannot occur.
In this case, the combination indicating no errors is output if there were no errors in the data, and the combination indicating uncorrectable errors is output when there are errors in the data whether or not those errors are correctable.

• Offset E (OE) and Offset F (OF)

When the IC has synchronized with the offset word E block data, the OE bit in the output data goes to “1”. At this point the bits B1 and B0, which express the RDS block number, will be “00”, i.e., both will be zero.
The LC7074/M does not recognize an offset word F block as a correct offset word. Therefore, the OF bit in the output data will always be “0”.



OE Bit Output

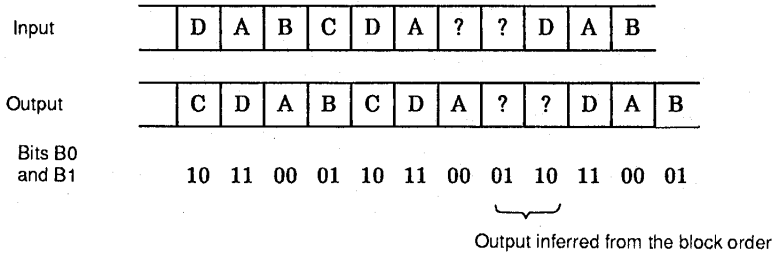
• Block Number (B0 and B1)

The block number bits indicate the data block of the output data.

B1	B0	Block
0	0	First block (the offset word A block)
0	1	Second block (the offset word B block)
1	0	Third block (the offset word C or C' block)
1	1	Fourth block (the offset word D block)

– The OE bit becomes one when the offset word E block data is output. At this point the bits B1 and B0 will be “00”, i.e., both will be zero.

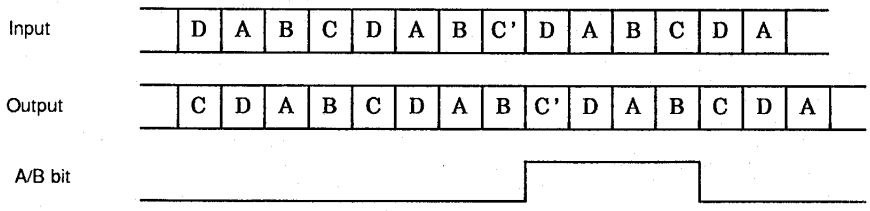
– Consider the situation where there is a block in the RDS group data output for which the input data offset word cannot be detected. Here, the IC assumes that the blocks were input in the correct offset word order, and outputs B0 to B1 accordingly.



Block Number Output

• Group Type Version (A/B)

The A/B bit is set based on the third block offset word of input data. If the offset word is “C”, the A/B bit is set to “0”, and if the offset word is “C”, the A/B bit is set to “1”.
Note that the version bit B0 in the second block (the offset word B block) data of input data is not used for group type version determination. As a result, the version bit A/B in the output data changes in the third block.



A/B Bit Output

5. Group Synchronization

• Recognized Offset Words

The LC7074/M recognizes the five offset words A, B, C, C' and D. The offset word F, which is stipulated by the EBU, is not recognized.

• Group Data Ordering and Synchronization

The LC7074/M recognizes the following three types of group data.
However, there is no limitation on the number of blocks in groups consisting of offset E blocks (type 3).

(1) A – B – C – D
(2) A – B – C' – D
(3) E – E – E – E
E – E – E
E – E
E

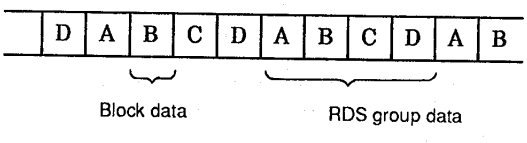
As a result, there are nine block data orders (listed as (1) to (9) below) that the LC7074/M recognizes, and any other order is determined to be an error.

Correct data orders	Data orders handled as errors
(1) A → B	A → C
(2) B → C	B → E
(3) B → C'	E → B
(4) C → D	•
(5) C' → D	•
(6) D → A	•
(7) D → E	
(8) E → E	
(9) E → A	

The data input wait state is called a synchronization sequence. When a clock signal is first input to the LC7074/M from the demodulation IC, the LC7074/M starts the operation of detecting offset words from data synchronized with the clock.
The LC7074/M synchronizes with the input data when it detects two blocks with correct offset words in correct positions.

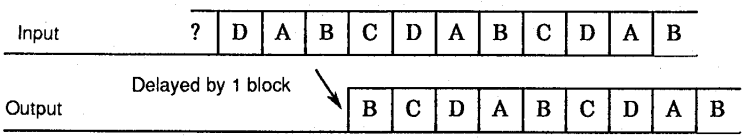
• Synchronization with RDS Group Data

– RDS block data format

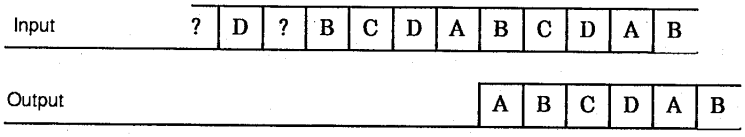


RDS Group Format

– Synchronization with RDS data



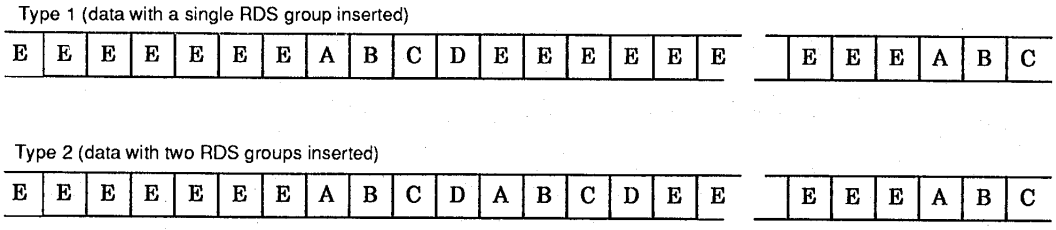
• Here the LC7074/M detects blocks D and A consecutively. Since it synchronizes at A, output starts with B from the same group.



• Here the LC7074/M detects the D and B blocks. Since it synchronizes at B, output starts with A from the next group.

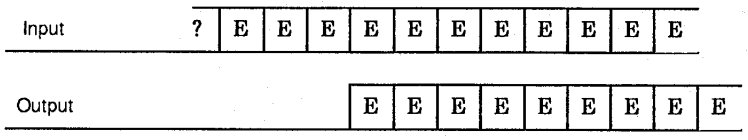
RDS Synchronization Sequence

• Synchronization with RDS/MMBS Group Data
– RDS/MMBS compound group data format

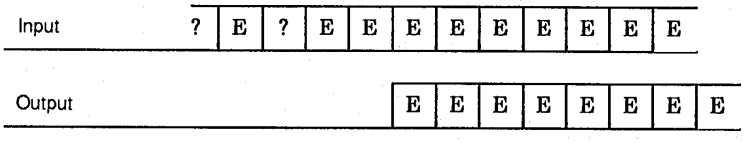


RDS/MMBS Group Data Format

– Synchronization with MMBS Group Data



• Detected for two consecutive blocks



• Detected for two of three blocks

Note: The LC7074/M does not recognize that MMBS group data consists of four MMBS blocks (offset word E blocks).

MMBS Synchronization Sequence

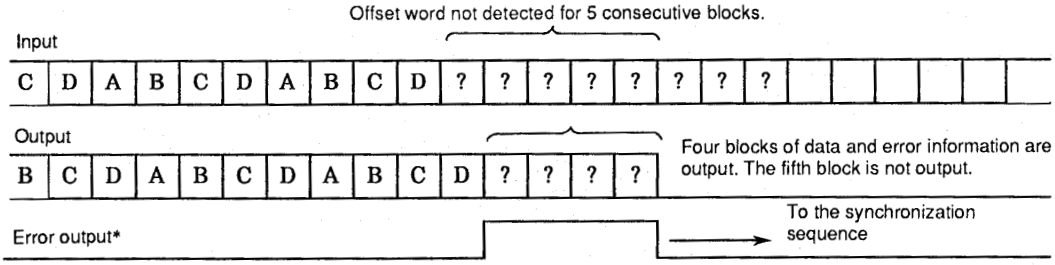
• Pull-Out

When a state occurs in which the LC7074/M is in the synchronized state and cannot detect the block data offset word, it enters a pull-out sequence.

When the LC7074/M is unable to detect the offset word in five consecutive blocks while in a pull-out sequence, it goes to the pull-out state. When the LC7074/M pulls out, it stops clock and data output and switches to the synchronization sequence.

Note that if the LC7074/M was unable to detect the offset word in fewer than five consecutive blocks, the synchronization state continues without change.

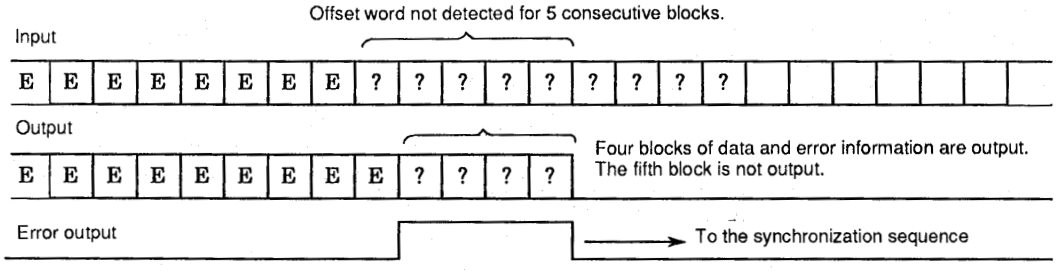
– Pull-out in RDS group data



Note: “Error output” refers to the E and F flags in the output data and to the ERROR and CORRECTION pins.

RDS Pull-Out Sequence

– Pull-out in MMBS group data

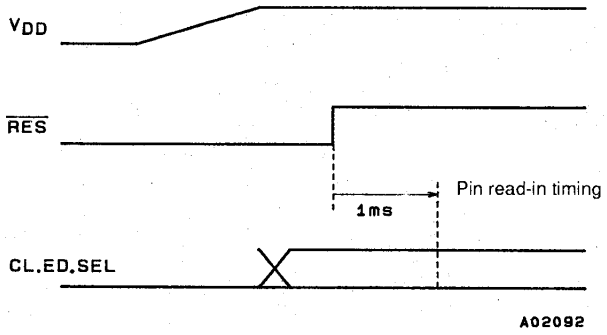


MMBS Pull-Out Sequence

6. Control Input Pin Read Timing (Pins CL.ED.SEL, CORR.SEL and D.S.CONTROL)

• CL.ED.SEL

The LC7074/M reads in the state of the CL.ED.SEL pin about 1 ms after a reset clear. It uses this signal for the internal settings that determine the clock output polarity.



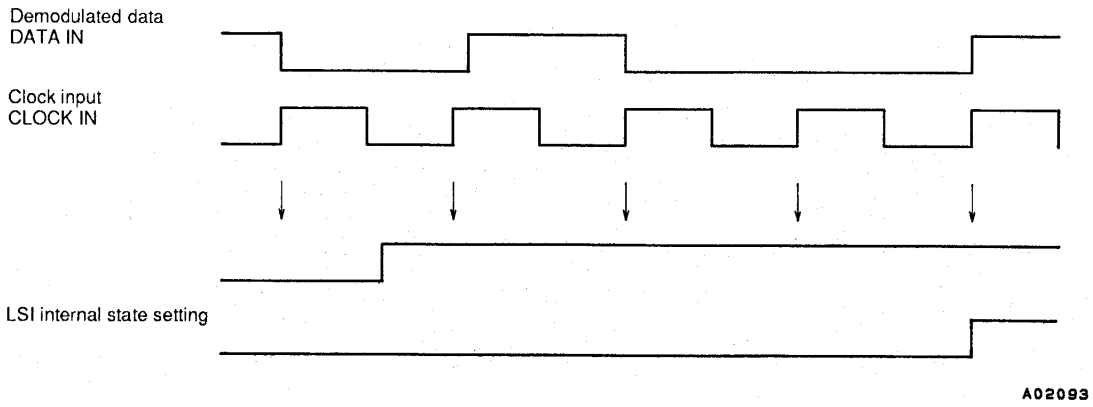
CL. ED. SEL Pin Read-In Timing

• CORR.SEL and D.S.CONTROL

The LC7074/M continuously checks the state of these pins. As a result, error correction can be turned on or off and the DATA START signal output form can be changed at any time.

– During synchronization detection (synchronization sequence)

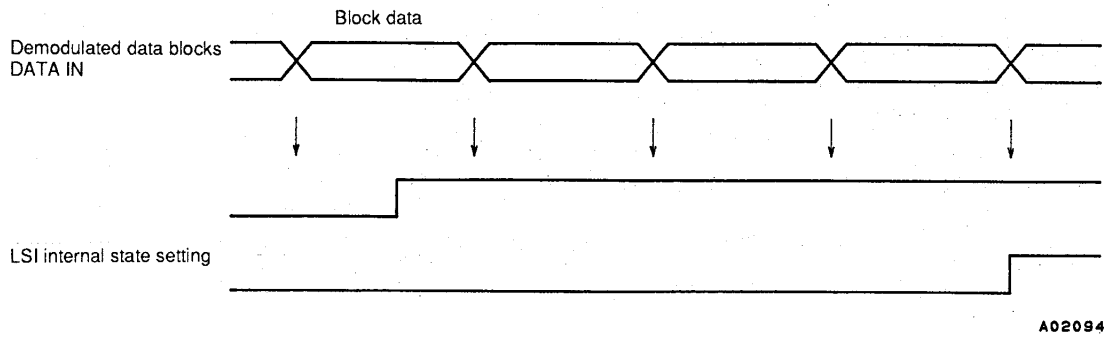
The pin states are read-in on each bit of demodulated data from the RDS demodulation IC (at the points shown by arrows in the figure). The state is read into the IC if the input values agree four times in a row.



Pin Read-In Timing during Synchronization Detection

– Following synchronization detection (while synchronized)

The LC7074/M reads in the pin state at the start of each block in the demodulated data from the RDS demodulation IC (at the points shown by arrows in the figure). The state is read into the IC if the input values agree four times in a row.



Pin Read-In Timing Following Synchronization Detection