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# LC709004A

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CMOS IC

## I/O-Expander for Microcontroller

### Overview

The LC709004A is a peripheral IC dedicated for expanding the capability of the microcontroller (MCU) I/O ports. It interfaces with the microcontroller through synchronous serial communication. Communication with the extended I/O ports is accomplished through 16-bit parallel I/O. The extended port features include the capabilities to specify the I/O direction on a bit basis, to specify the output type (CMOS or N-channel open drain), and to specify the I/O voltage level on a port basis according to the power level of the peripheral equipment. These features make allow the LC709004A to be used in a wide variety of applications.

### Features

- 4-/5-wire synchronous serial transmission and reception, and 16-bit parallel I/O
- Wide operating voltage range (2.0V to 6.0V)
- Multifunction I/O ports
  - I/O direction specification: Bit units
  - CMOS or Nch-OD output type specification: Bit units
  - Output voltage adjustment: Port (8 bits) units
- Output current: 12mA max. (capable of driving a green LED directly)
- Data transmission and reception: Can control reception of input data and transmission of output data in parallel.
- Cascaded configuration: Ports can be expanded in units of 16 bits  $\times$  n (n is the number of LSI chips).
- Packaging from: MFP24S (300mil): lead-free type (discontinued)  
MFP24SJ (300mil): lead-free type

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## Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Ratings			Unit	
				$V_{DD}[\text{V}]$	min	typ		max
Maximum supply voltage	$V_{DD \text{ max}}$	$V_{DD}, V_{DDP1}$	$V_{DD}=V_{DDP1}$		-0.3		+7.0	V
Input voltage	$V_I$	$\overline{\text{RES}}, \overline{\text{CS}}, \text{DIN}, \overline{\text{CLK}}$			-0.3		$V_{DD}+0.3$	
Output voltage	$V_O$	DOUT			-0.3		$V_{DD}+0.3$	
Input/output voltage	$V_{IO(1)}$	Port 0			-0.3		$V_{DDP1}+0.3$	
	$V_{IO(2)}$	Port 1			-0.3		$V_{DDP1}+0.3$	
High level output current								
Peak output current	IOPH(1)	Ports 0 to 1	CMOS output selected Per 1 applicable pin		-7			mA
	IOPH(2)	DOUT			-13			
Mean output current (Note 1)	IOMH(1)	Ports 0 to 1	CMOS output selected Per 1 applicable pin		-3			
	IOMH(2)	DOUT			-6			
Total output current	$\Sigma\text{IOP0H}$	Port 0	Total of all applicable pins		-32			
	$\Sigma\text{IOP1H}$	Port 1	Total of all applicable pins		-32			
	$\Sigma\text{IOAH}$	DOUT, ports 0 to 1	Total of all applicable pins		-77			
Low level output current								
Peak output current	IOPL(1)	Ports 0 to 1	Per 1 applicable pin				16	mA
	IOPL(2)	DOUT					13	
Mean output current (Note 1)	IOML(1)	ports 0 to 1	Per 1 applicable pin				7	
	IOML(2)	DOUT					6	
Total output current	$\Sigma\text{IOP0L}$	Port 0	Total of all applicable pins				32	
	$\Sigma\text{IOP1L}$	Port 1	Total of all applicable pins				32	
	$\Sigma\text{IOAL}$	DOUT, ports 0 to 1	Total of all applicable pins				77	
Power dissipation	Pd max (1)	MFP24S (300mil)	$T_a = -30$ to $+70^\circ\text{C}$				177	mW
	Pd max (2)	MFP24SJ (300mil)					T.B.D	
Operating temperature	$T_{opr}$				-30		70	$^\circ\text{C}$
Storage temperature	$T_{stg}$				-55		125	

Note 1: The mean output current is a mean value measured over 100ms.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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**Allowable Operating Conditions** at Ta = -30 to +70°C, V<sub>SS</sub> = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification (Note 3)			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Operating supply voltage	V <sub>DD</sub> (1)	V <sub>DD</sub>			2.0		6.0	V
	V <sub>DD</sub> (2)	V <sub>DD</sub> P1	Supply voltage must be within V <sub>DD</sub> (1)'s specification.	2.0 to 6.0	V <sub>DD</sub> -3.0		V <sub>DD</sub>	
High level input voltage	V <sub>IH</sub> (1)	DIN, ports 0 to 1		4.5 to 6.0	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub> Px	
	V <sub>IH</sub> (2)	DIN, ports 0 to 1		2.0 to 6.0	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub> Px	
	V <sub>IH</sub> (3)	$\overline{RES}$ , $\overline{CS}$ , $\overline{CLK}$		4.5 to 6.0	0.4V <sub>DD</sub> +0.7		V <sub>DD</sub>	
	V <sub>IH</sub> (4)	$\overline{RES}$ , $\overline{CS}$ , $\overline{CLK}$		2.0 to 6.0	0.4V <sub>DD</sub> +0.7		V <sub>DD</sub>	
Low level input voltage	V <sub>IL</sub> (1)	DIN, ports 0 to 1		4.5 to 6.0	V <sub>SS</sub>		0.2V <sub>DD</sub> +0.1	
	V <sub>IL</sub> (2)	DIN, ports 0 to 1		2.0 to 6.0	V <sub>SS</sub>		0.2V <sub>DD</sub> +0.1	
	V <sub>IL</sub> (3)	$\overline{RES}$ , $\overline{CS}$ , $\overline{CLK}$		4.5 to 6.0	V <sub>SS</sub>		0.1V <sub>DD</sub> +0.2	
	V <sub>IL</sub> (4)	$\overline{RES}$ , $\overline{CS}$ , $\overline{CLK}$		2.0 to 6.0	V <sub>SS</sub>		0.1V <sub>DD</sub> +0.2	

Note 3: V<sub>DD</sub>Px denote the power supply pin (V<sub>DD</sub>P1) for port pins.

**Electrical Characteristics** at Ta = -30 to +70°C, V<sub>SS</sub> = 0V

Parameter	Symbol	Pin/Remarks	Conditions	(Note 3)		Ratings			Unit
				V <sub>DD</sub> [V]	V <sub>DD</sub> Px[V]	min	typ	max	
High level input current	I <sub>IH</sub>	$\overline{RES}$ , $\overline{CS}$ , $\overline{CLK}$ , Ports 0 to 1	V <sub>IN</sub> =V <sub>DD</sub> (including output Tr. off leakage current)	2.0 to 6.0				10	μA
Lower level input current	I <sub>IL</sub>	$\overline{RES}$ , $\overline{CS}$ , $\overline{CLK}$ , Ports 0 to 1	V <sub>IN</sub> =V <sub>SS</sub> (including output Tr. off leakage current)	2.0 to 6.0		-10			μA
High level output voltage	V <sub>OH</sub> (1)	Ports 0	I <sub>OH</sub> =-2mA	2.0 to 6.0	4.5 to 6.0	V <sub>DD</sub> Px-0.5			V
	V <sub>OH</sub> (2)			2.0 to 6.0	4.5 to 6.0	V <sub>DD</sub> Px-1.0			
	V <sub>OH</sub> (3)			2.0 to 6.0	2.0 to 6.0	V <sub>DD</sub> Px-0.5			
	V <sub>OH</sub> (4)	Ports 1	I <sub>OH</sub> =-2mA	2.0 to 6.0	4.5 to 6.0	V <sub>DD</sub> Px-0.5			
	V <sub>OH</sub> (5)			2.0 to 6.0	4.5 to 6.0	V <sub>DD</sub> Px-1.0			
	V <sub>OH</sub> (6)			2.0 to 6.0	2.0 to 6.0	V <sub>DD</sub> Px-0.5			
	V <sub>OH</sub> (7)	DOUT	I <sub>OH</sub> =-5mA	4.5 to 6.0		V <sub>DD</sub> Px-0.5			
	V <sub>OH</sub> (8)			4.5 to 6.0		V <sub>DD</sub> Px-1.0			
	V <sub>OH</sub> (9)			2.0 to 6.0		V <sub>DD</sub> Px-0.5			
Lower level output voltage	V <sub>OL</sub> (1)	Ports 0	I <sub>OL</sub> =5mA	4.5 to 6.0	2.0 to 6.0			0.4	V
	V <sub>OL</sub> (2)			4.5 to 6.0	2.0 to 6.0			1	
	V <sub>OL</sub> (3)			2.0 to 6.0	2.0 to 6.0			0.4	
	V <sub>OL</sub> (4)	Ports 1	I <sub>OL</sub> =5mA	4.5 to 6.0	4.5 to 6.0			0.4	
	V <sub>OL</sub> (5)			4.5 to 6.0	4.5 to 6.0			1	
	V <sub>OL</sub> (6)			2.0 to 6.0	2.0 to 6.0			0.4	
	V <sub>OL</sub> (7)	DOUT	I <sub>OL</sub> =5mA	4.5 to 6.0				0.4	
	V <sub>OL</sub> (8)			4.5 to 6.0				1	
	V <sub>OL</sub> (9)			2.0 to 6.0				0.4	
Pull-up resistance	R <sub>pu</sub> (1)	$\overline{CS}$	V <sub>OH</sub> =V <sub>SS</sub>	4.5 to 6.0		100	230	650	kΩ
Voltage hysteresis	V <sub>HIS</sub>	$\overline{RES}$ , $\overline{CS}$ , $\overline{CLK}$		2.0 to 6.0			0.1V <sub>DD</sub>		V
Consumption current (operation stopped)	ID <sub>SSP</sub>	V <sub>DD</sub> =V <sub>DD</sub> P1	$\overline{RES}$ = $\overline{CS}$ =V <sub>DD</sub> CLK=DIN=V <sub>DD</sub> or V <sub>SS</sub> DOUT=open P0 to P1=open or V <sub>DD</sub> or V <sub>SS</sub> (Note 2)	2.0 to 6.0				20	μA
Pin capacity	CP	All pins	Other than test pin V <sub>IN</sub> =V <sub>SS</sub> f=1MHz Ta=25°C	2.0 to 6.0				10	pF

Note 2: The consumption current does not include the current flowing into the port's output transistor.

Note 3: V<sub>DD</sub>Px denote the power supply pin (V<sub>DD</sub>P1) for port pins.

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**Switching I/O Characteristics** at Ta=-30 to +70°C, VDD=VDDP1, VSS=0V

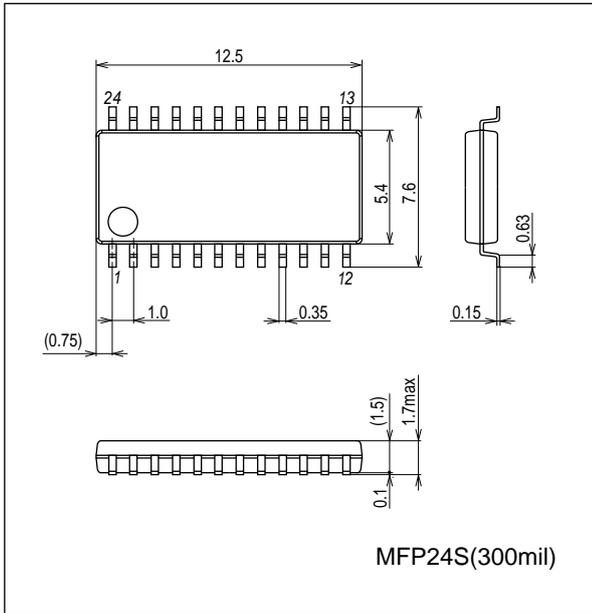
Parameter	Symbol	Pin/Remarks	Conditions	Specification (Note 3)			Unit
				VDD[V]	min	typ	
Clock setup time	TsCLK	$\overline{CS}$ , $\overline{CLK}$	•Specified with respect to falling edge of $\overline{CS}$ . •See Fig. 8.	2.0 to 6.0	100		ns
Chip select low level setup time	TsICS	$\overline{CS}$ , $\overline{CLK}$	•Specified with respect to falling edge of $\overline{CS}$ . •See Fig. 8.	2.0 to 6.0	100		
Chip select low level hold time	ThICS	$\overline{CS}$ , $\overline{CLK}$	•Specified with respect to falling edge of $\overline{CS}$ . •See Fig. 8.	2.0 to 6.0	100		
Clock hold time	ThCLK	$\overline{CS}$ , $\overline{CLK}$	•Specified with respect to falling edge of $\overline{CS}$ . •See Fig. 8.	2.0 to 6.0	200		
Clock low level pulse width	TwiCLK	$\overline{CLK}$	•See Fig. 8.	4.5 to 6.0	250		
				2.7 to 6.0	500		
				2.0 to 6.0	1000		
Clock high level pulse width	TwhCLK	$\overline{CLK}$	•See Fig. 8.	4.5 to 6.0	250		
				2.7 to 6.0	500		
				2.0 to 6.0	1000		
Chip select high level setup time	TshCS	$\overline{CS}$ , $\overline{RES}$	•See Fig. 8.	2.0 to 6.0	200		
Chip select high level hold time	ThhCS	$\overline{CS}$ , $\overline{RES}$	•See Fig. 8.	2.0 to 6.0	100		
Chip select low level pulse width	TwICS	$\overline{CS}$ , $\overline{RES}$	•See Fig. 8.	2.0 to 6.0	200		
Reset low level pulse width	TwIRES	$\overline{CS}$ , $\overline{RES}$	•See Fig. 8.	2.0 to 6.0	150		
Data setup time	TsDIN	DIN	•Specified with respect to falling edge of $\overline{CLK}$ . •See Fig. 8.	4.5 to 6.0	30		
				2.0 to 6.0	50		
Data hold time	ThDIN	DIN	•Specified with respect to falling edge of $\overline{CLK}$ . •See Fig. 8.	4.5 to 6.0	50		
				2.7 to 6.0	150		
				2.0 to 6.0	300		
Serial data output delay time (Note 4)	TdDOUT	DOUT	•Specified with respect to falling edge of $\overline{CLK}$ . •See Fig. 8.	4.5 to 6.0		200	
				2.7 to 6.0		400	
				2.0 to 6.0		800	
Port data output delay time	TdPOUT	Port 0 to 1	•Specified with respect to rising edge of $\overline{CS}$ . •See Fig. 8.	4.5 to 6.0		200	
				2.7 to 6.0		400	
				2.0 to 6.0		800	
Port data input setup time	TsPIN	Port 0 to 1	•Specified with respect to rising edge of $\overline{CLK}$ . •See Fig. 8.	4.5 to 6.0	30		
				2.0 to 6.0	50		
Port data input hold time	ThPIN	Port 0 to 1	•Specified with respect to rising edge of $\overline{CLK}$ . •See Fig. 8.	4.5 to 6.0	50		
				2.7 to 6.0	150		
				2.0 to 6.0	300		

Note 4: The input data of P00 will be out from DOUT terminal at the first negative edge of  $\overline{CLK}$  signal. Because of this, Serial data output delay time of the first clock will be the time measured from the negative edge of the  $\overline{CLK}$  or the time at the input data (P00) is settled.

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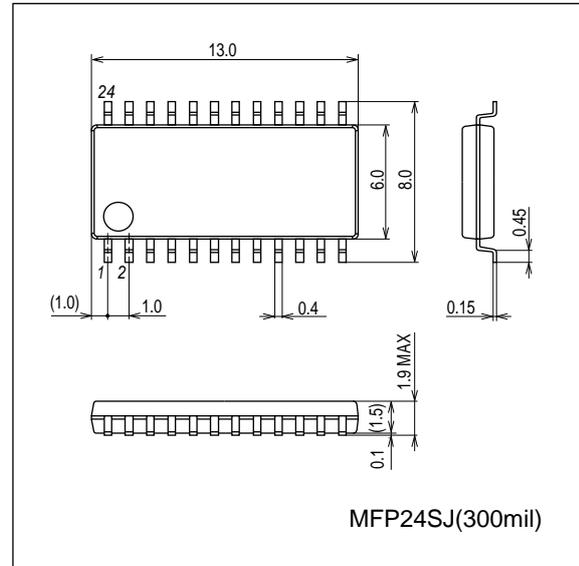
## Package Dimensions

unit : mm (typ)  
3112B

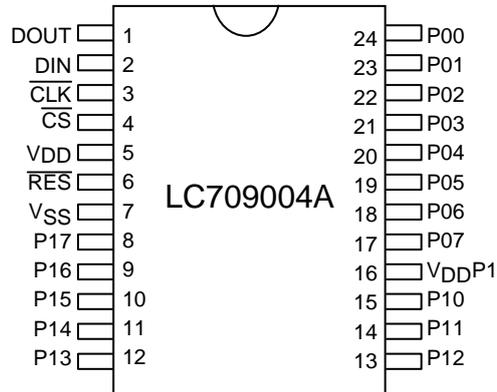


## Package Dimensions

unit : mm (typ)  
3419



## Pin Assignment

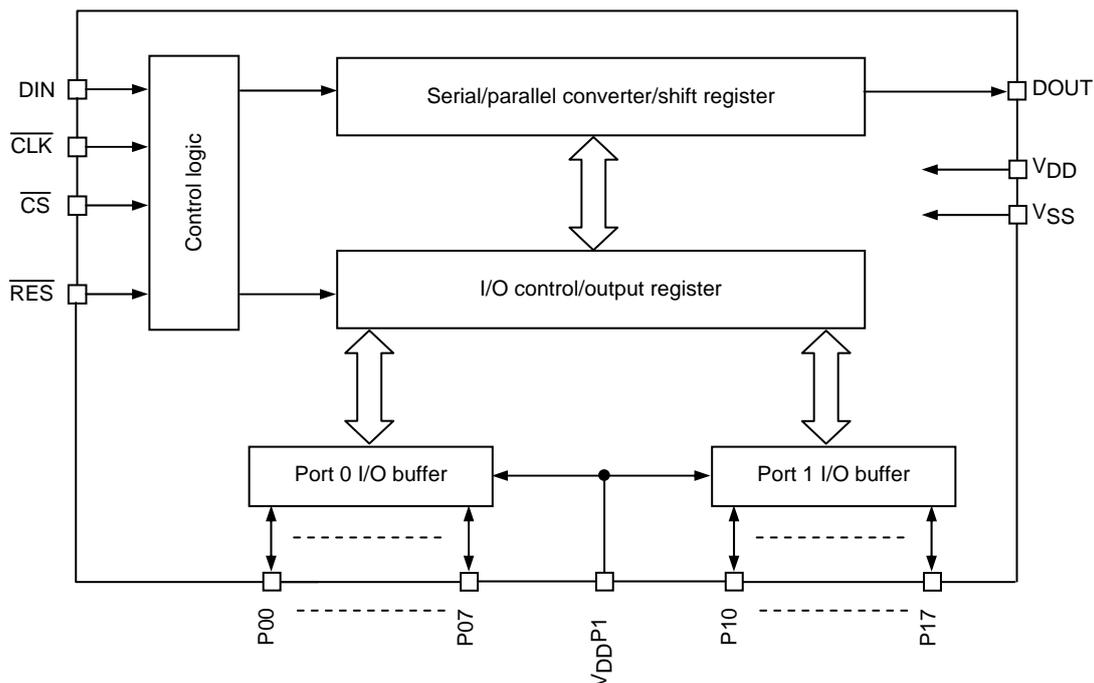


Top view

MFP24S (300mil): lead-free type/MFP24SJ (300mil): lead-free type

# LC709004A

## Block Diagram



## Pin Description

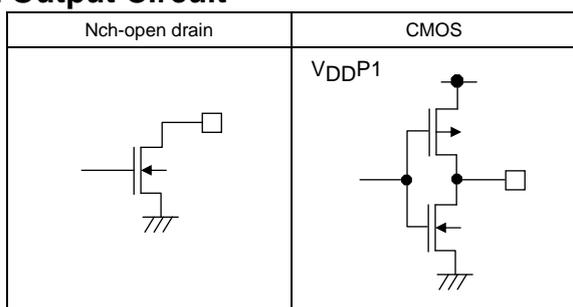
Pin Name	I/O	Description	I/O Type	Reset Time State
VSS	-	• - power supply pin		
VDD VDDP1	-	• + power supply pin • VDD is the power supply pin for blocks other than I/O ports (P00 to P17). • VDDP1 is the power supply pin for port pins P00 to P17. (Notes) • VDDP1 must not be set higher than VDD ( $V_{DDP1} \leq V_{DD}$ ).		
Port 0 P00 to P07	I/O	• 8-bit I/O port • I/O specifiable in 1 bit units. • CMOS/Nch-open drain specifiable in 1 bit units. • Output voltage variable in 1 port units according to VDDP1 voltage.	Output: CMOS/Nch-OD Input: TTL	Hi-Z
Port 1 P10 to P17	I/O	• 8-bit I/O port • I/O specifiable in 1 bit units. • CMOS/Nch-open drain specifiable in 1 bit units. • Output voltage variable in 1 port units according to VDDP1 voltage.	Output: CMOS/Nch-OD Input: TTL	Hi-Z
DIN	I	• Serial data input pin	Input: TTL	
DOUT	O	• Serial data output pin	Output: CMOS	High
CLK	I	• Serial clock input pin • Port data is placed on DOUT on the falling edge of this clock. • The data from DIN is latched on the negative-to-positive transition of this clock.	Input: TTL Schmitt	
CS	I	• Chip select input pin • Setting this pin to the low level enables serial data to be input or output.	Input: TTL Schmitt	
RES	I	• Device's system reset input pin • Setting this pin to the low level initializes the internal control circuit and registers and puts DOUT in the high level and all data port pins (P00 to P17) into the Hi-Z state.	Input: TTL Schmitt	

## Port Output Types and I/O States

The output type and I/O states of the LC709004A's ports can be selected by configuring the data direction register (DDR) and data register (DTR). Port data can be taken into the LC709004A only when DDR is set to 0 (Nch-open drain) and DTR is set to 1 (Nch-Tr OFF). The ports are held high for the other settings of DDR and DTR.

Port Name	DDR	DTR	Port		
			Output Type	Input	Output
P00 to P07 P10 to P17	0	1	Nch-open drain	Enabled	Hi-Z
	0	0	Nch-open drain	Disabled (High)	Low
	1	1	CMOS	Disabled (High)	High
	1	0	CMOS	Disabled (High)	Low

## Port Output Circuit



## Principles of Operation

The LC709004A accomplishes data transmission and reception to and from the MCU through synchronous serial communication and performs I/O operations on the extended ports in parallel mode. Its communication modes (MCU to LC709004A by serial to parallel conversion and LC709004A to MCU by parallel to serial conversion) include the initial communication modes (modes 0 and 1) in which the LC709004A initializes itself and the data communication mode in which the LC709004A sends and receives port data. The initial communication modes are used for various communication control purposes for the first time in system operation after a power-on or system reset. In these modes, the LC709004A sets up the I/O mode and output type of the ports. The data communication mode is used for communication control after the end of the initial communication modes. In this mode, the LC709004A carries out actual port I/O operations. The port I/O mode and output type settings are stored in the data direction register (DDR). The data output state settings ("High" output, "Hi-Z" output, or "Low" output) are stored in the data register (DTR). The LC709004A's operating modes are summarized below, followed by detailed mode descriptions.

Communication Mode		Description
Initial communication mode	Mode 0	Sets the output type of all ports to "N-ch-open drain."
	Mode 1	Sets the I/O direction of the ports and the their output type to CMOS or "Nch-open-drain" on a bit basis.
Data communication mode		Sends and receives port data.

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## (1) Initial communication modes

### • Mode 0

- 1) Setting the  $\overline{\text{RES}}$  pin to the low level initializes the system, sets the DOUT pin to the high level, and sets the DDR register of all ports to 0 and the DTR register to 1. The output type of the ports is set to Nch-open drain and their I/O state ( $\text{Nch-Tr=OFF}$ ) to the "Hi-Z" (input mode) state.
- 2) When the  $\overline{\text{RES}}$  pin is set high (reset) and the  $\overline{\text{CS}}$  pin is set and held low for a certain period ( $\text{TwlCS}$ ), the DDR is fixed at 0. Subsequently, the LC709004A is placed in the data communication mode.

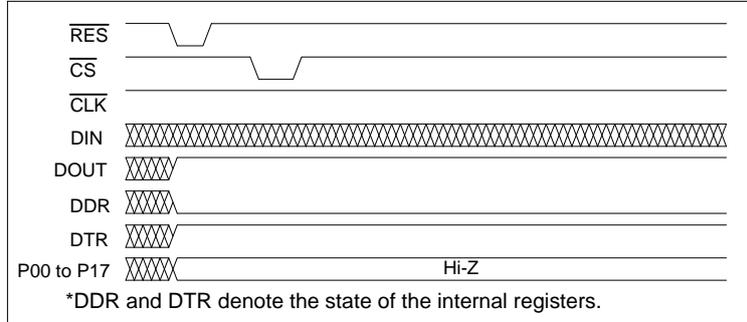


Fig. 1

### • Mode 1

- 1) When the  $\overline{\text{RES}}$  pin is set to the low level, the LC709004A initializes the system, sets the DOUT pin to the high level, and sets the DDR register of all ports to 0 and the DTR register to 1. The output type of the ports is set to Nch-open drain and their I/O state ( $\text{Nch-Tr=OFF}$ ) to the "Hi-Z" (input mode) state.
- 2) When the  $\overline{\text{RES}}$  pin is set high (reset) and the  $\overline{\text{CS}}$  pin is set low, the LC709004A gets ready for serial communication.
- 3) The input data at P00 is sent directly to the DOUT pin on the first falling edge of the transmission clock signal CLK. The data at pins P01 to P17 is loaded into the shift register on the rising edge of the next clock.
- 4) Subsequently, the ports' input data, which is loaded into the shift register on the falling edge of CLK, is placed at the DOUT pin sequentially (P00→P07, P10→P17) in synchronization with the falling edges of CLK, starting at port pin P00. In parallel with this operation, when data to be placed at the ports is supplied to the DIN pin sequentially starting at the port pin P00 (P00→P07, P10→P17), it is loaded into the internal shift register in synchronization with the rising edges of CLK.
- 5) When the  $\overline{\text{CS}}$  pin is set high after the rising edge of the 16th clock, the data loaded in the shift register is loaded into the DDR register which determines the I/O mode and output type of the data (serial data is loaded into the DDR register after a reset is effected). Subsequently, the LC709004A controls serial data transmission and reception in the data communication mode.

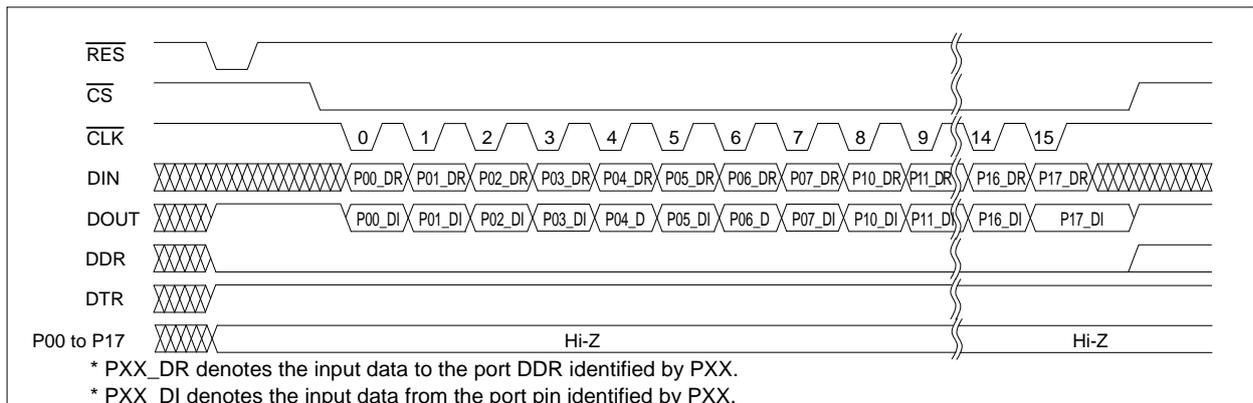


Fig. 2

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(2) Data communication mode

- 1) When the  $\overline{CS}$  pin is set low with the  $\overline{RES}$  pin held high, the LC709004A gets ready for serial communication. (Subsequently, processing in steps 2) and 3) are identical to steps 2) and 3) in paragraph (1)-2).
- 2) The input data at P00 is sent directly to the DOUT pin on the first falling edge of the  $\overline{CLK}$  signal. Data at pins P01 to P17 is loaded into the shift register on the next rising edge of the clock.
- 3) Subsequently, the ports' input data, which is loaded into the shift register on the falling edge of  $\overline{CLK}$ , is placed at the DOUT pin sequentially (P00→P07, P10→P17) in synchronization with the falling edges of  $\overline{CLK}$ , starting at port pin P00. In parallel with this operation, when data to be placed at the ports is supplied to the DIN pin sequentially starting at the port pin P00 (P00→P07, P10→P17), it is loaded into the internal shift register in synchronization with the rising edges of CLK.
- 4) When the  $\overline{CS}$  pin is set high after the rising edge of the 16th clock, the data loaded in the shift register is loaded into the DDR register which determines the output state of the ports and the states of all port pins (P00 to P17) are then changed (output) according to the conditions established in the DDR and DTR registers. Serial data that occurs following the initial communication mode processing is always loaded into the DTR register.

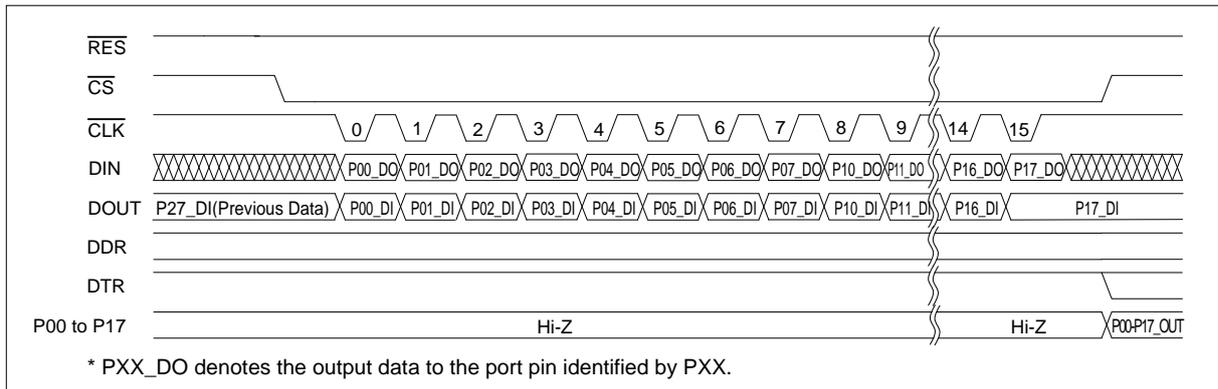


Fig. 3

- 5) Subsequently, the state of all port pins (P00 to P17) is updated each time the set of steps 1) to 4) described in paragraph (2) are performed.

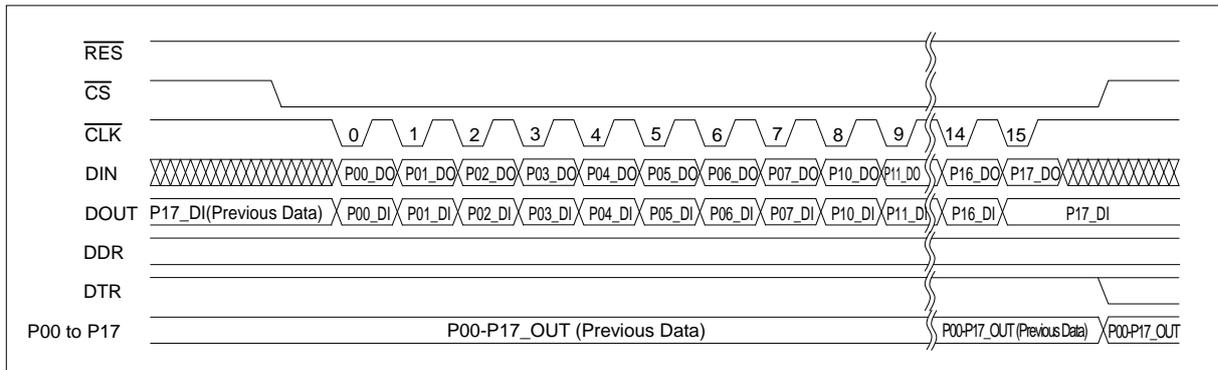


Fig. 4

## Application Examples

### (1) Example of a cascade configuration

Two or more LC709004A LSI chips can be cascaded to realize port expansion beyond 16 bits. Port expansion, however, need to be made in units of 16 bits  $\times$  n (n denotes the number of LSI chips).

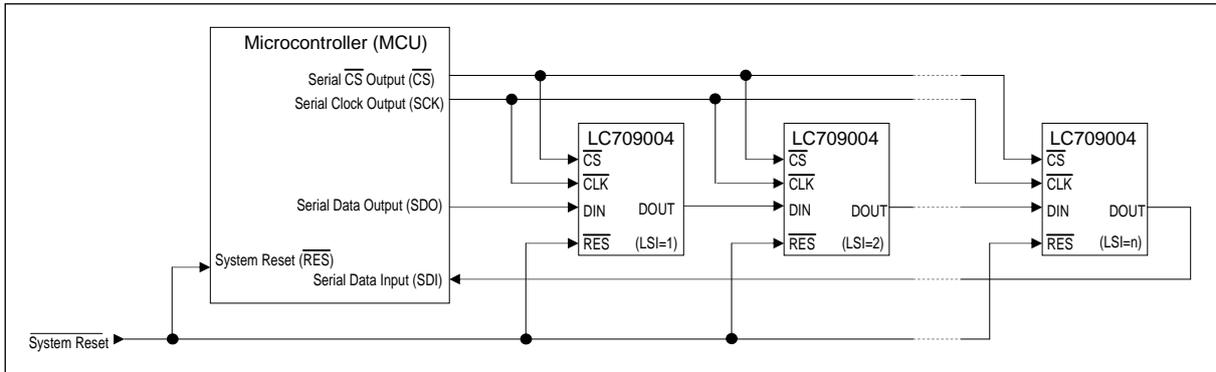


Fig. 5

### (2) Variable port power level example

When controlling the level of I/O ports according to the power voltage level of the peripheral equipment, the user can connect the output from the power supply of the peripheral equipment directly to the power supply pins for the I/O ports. The LC709004A dispenses with the need to add an external level shifter circuit.

Note the following when configuring the LC709004A in this way:

#### Note 5:

- $V_{DDP1}$ : The voltage level of  $V_{DDP1}$  must not be higher than that of  $V_{DD}$  ( $V_{DDP1} \leq V_{DD}$ ).
- The input level of all ports (P00 to P17) is dependent on the  $V_{DD}$  power source; it depends on none of the power sources  $V_{DDP1}$ .
- \* Be sure to check the electrical characteristics of the LC709004A.

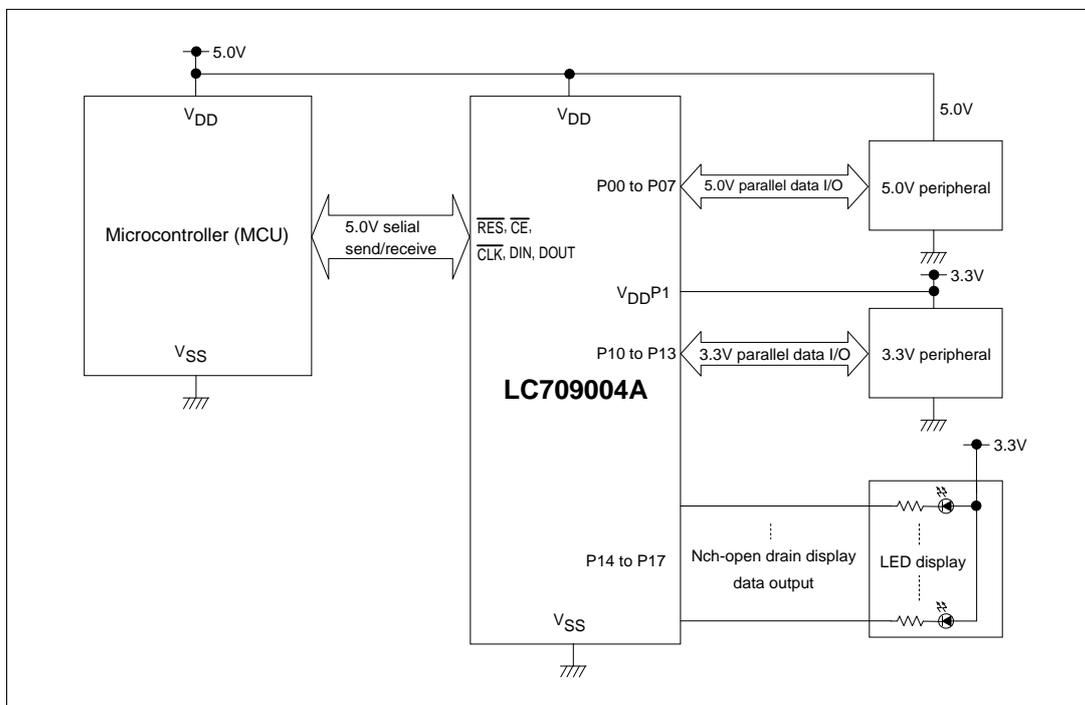


Fig. 6

Example of Placing Bypass Capacitors between V<sub>DD</sub> and V<sub>SS</sub> Terminals

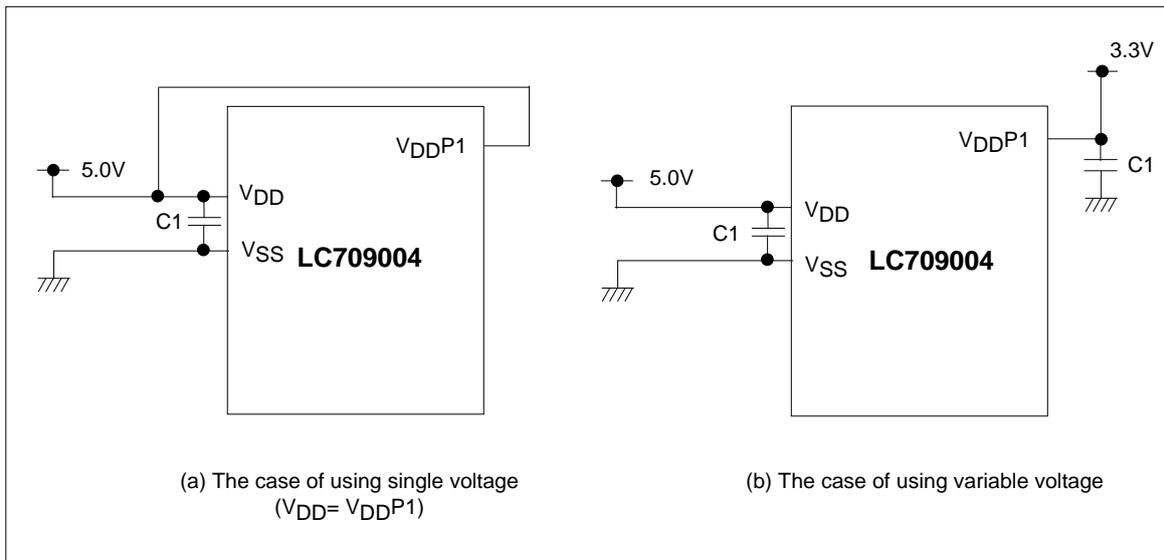


Fig. 7

In the case of using single voltage source as showing in the Fig.7 (a), you must connect a bypass capacitor (C1, about 0.1μF) between V<sub>DD</sub> and V<sub>SS</sub>. When connecting the capacitor (C1) and V<sub>DD</sub>-V<sub>SS</sub>, use a thick wire, and try to make its length as short as possible: moreover, try to make the impedance of V<sub>DD</sub>-C1 and V<sub>SS</sub>-C1 equal. In addition, when using several voltage sources as showing in the Fig.7 (b), it is suggested to connect the bypass capacitor to each set of the voltage terminals.

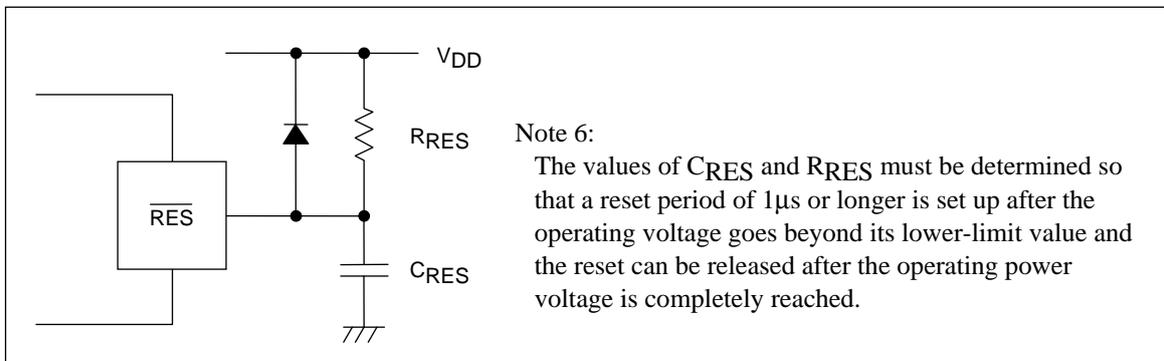


Fig. 8: Reset Circuit

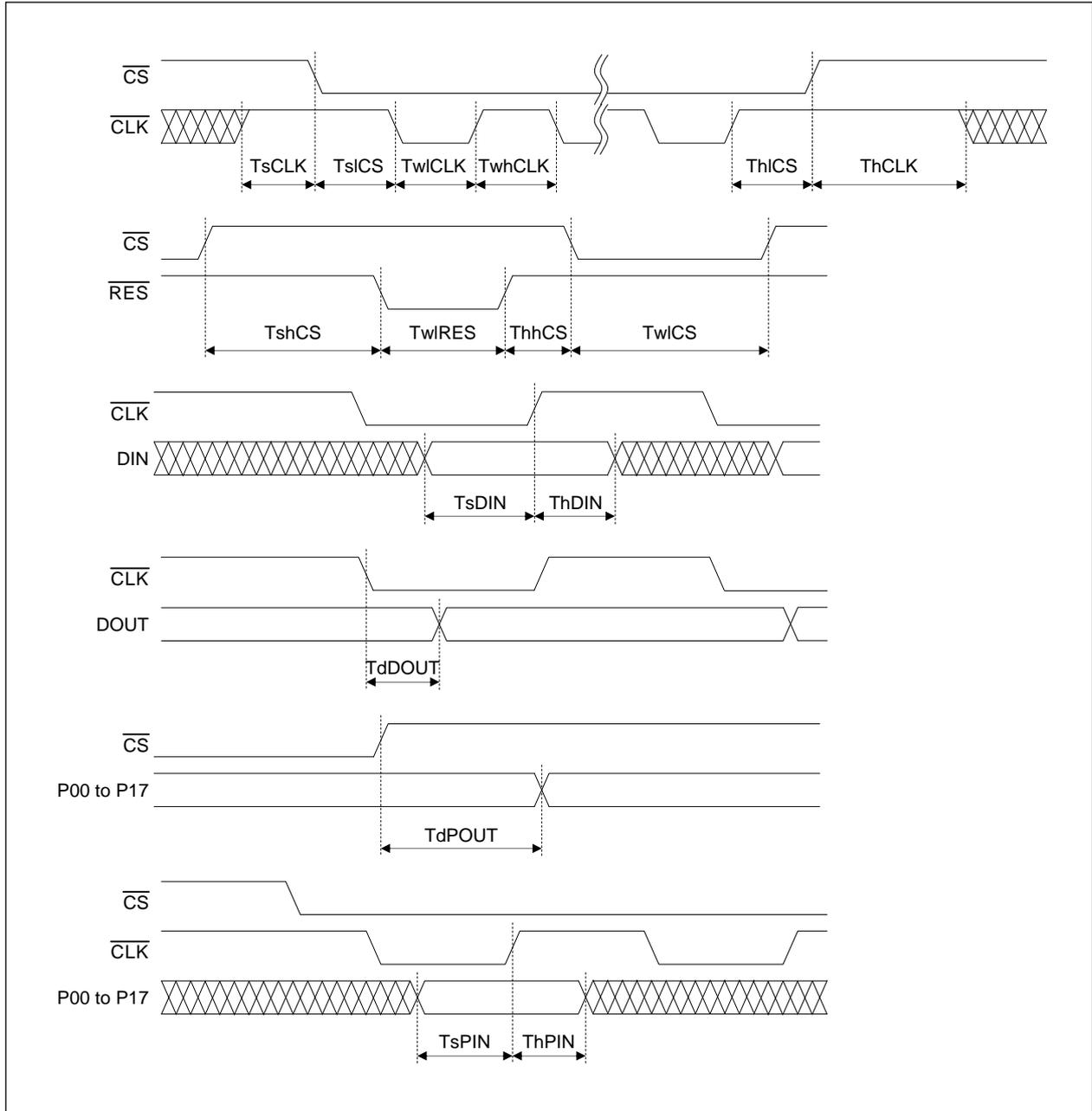


Fig. 9: Serial I/O and Parallel Data I/O Timing Diagram

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