

**SANYO**

No. 4246

**LC7472M****On-screen Video Display Controller  
for NTSC or PAL-M**

## OVERVIEW

The LC7472M is a CMOS, video display controller for superimposing text and low-level graphics onto an NTSC or PAL-M compatible television receiver. Up to 240, 8 × 8-pixel characters can be displayed under microprocessor control on a 24-character by 10-line display.

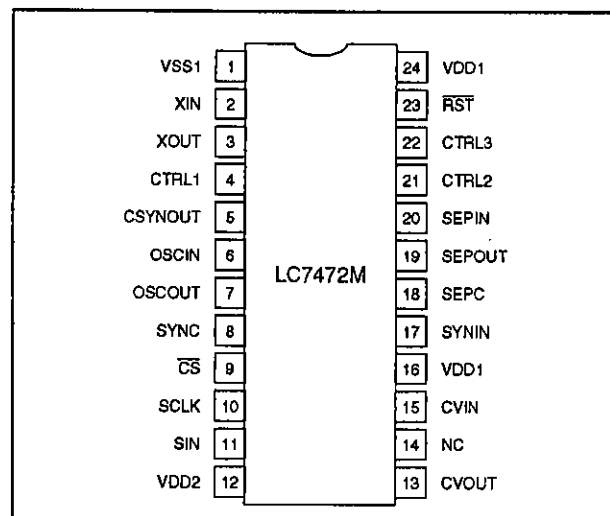
The LC7472M features selectable pixel width and height, and 64 vertical and 64 horizontal display start positions. It also features a flashing enable bit for each character position.

The LC7472M operates from a 5 V supply and is available in 24-pin SOPs.

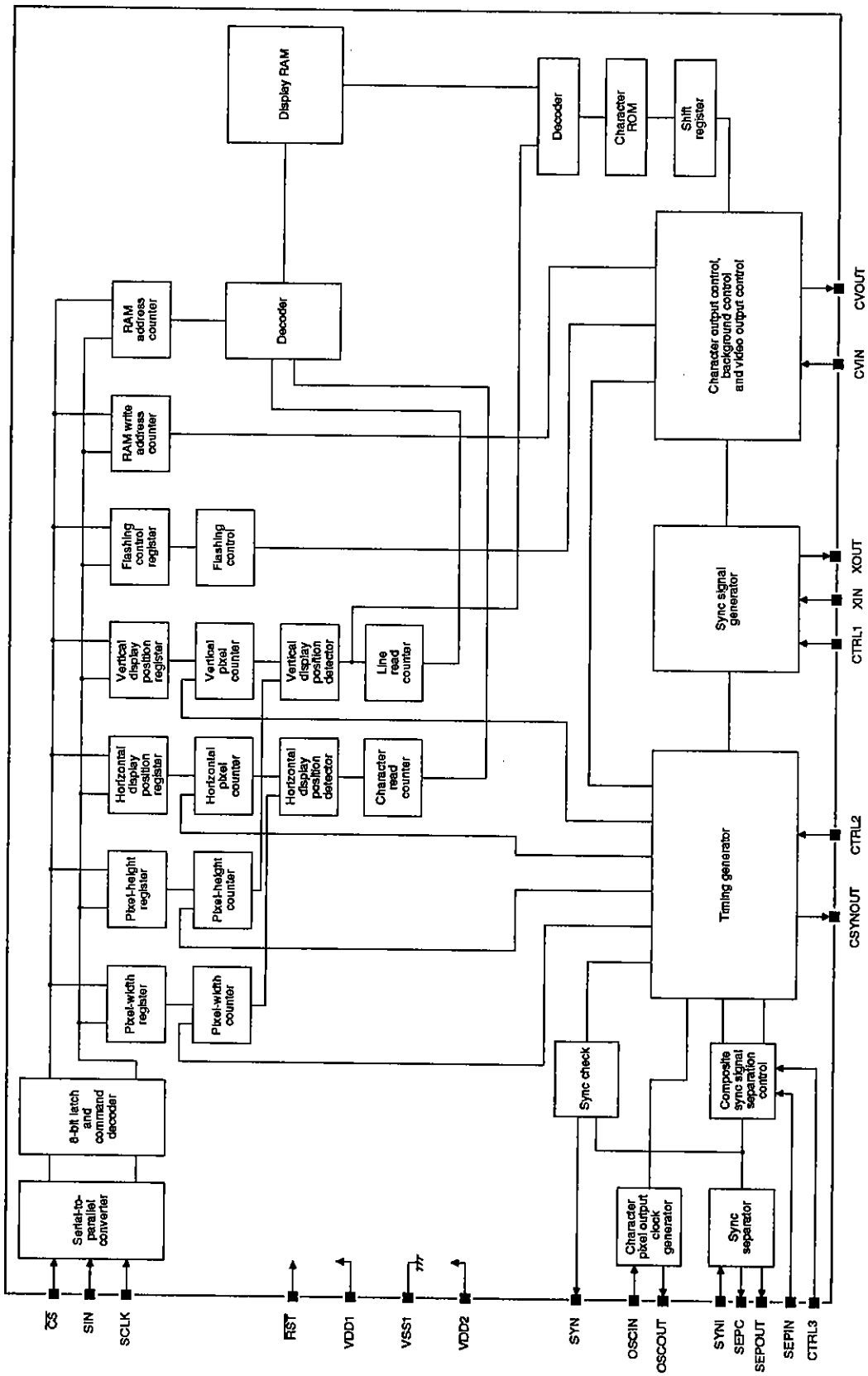
## FEATURES

- Complete text and graphics video overlay circuitry
- 64-character internal character generator ROM
- 8 × 8-pixel characters
- Three pixel widths and three pixel heights
- Selectable background color
- Built-in synchronization check and separation circuitry
- Approximately 0.5 or 1 s period character flashing option
- NTSC or PAL-M format compatibility
- 8-bit serial input format
- 5 V supply
- 24-pin SOP

## PINOUT



BLOCK DIAGRAM



## LC7472M

### PIN DESCRIPTION

Number	Name	Description
1	VSS1	Ground
2	XIN	Crystal oscillator input
3	XOUT	Crystal oscillator output
4	CTRL1	Crystal oscillator input select. HIGH for external (2fsc) clock input mode
5	CSYNOUT	Composite synchronization signal output. During reset ( $\overline{RST}$ LOW), crystal oscillator clock is output. No output for internal reset command
6	OSCIN	LC oscillator input. LC circuit for pixel clock generation character output
7	OSCOOUT	LC oscillator output. LC circuit for pixel clock generation character output
8	SYNC	External synchronization signal check output. During reset ( $\overline{RST}$ LOW), pixel clock is output. No output for internal reset command
9	$\overline{CS}$	Serial data input enable when LOW, with pull-up resistance
10	SCLK	Clock input for serial data input, with pull-up resistance
11	SIN	Serial data input, with pull-up resistance
12	VDD2	Power supply for composite video image signal level modulation (for analog system)
13	CVOUT	Composite video image signal output
14	NC	No connection
15	CVIN	Composite video image signal input
16	VDD1	5 V power supply for digital system
17	SYNCIN	Synchronization separation circuit input. If internal sync separation circuit is not used, use SYNCIN to input an external horizontal or composite synchronization signal.
18	SEPC	Synchronization separation circuit modulator capacitor connection. Leave open if not used.
19	SEPOUT	Composite synchronization separation circuit output. Outputs SYNCIN signal if internal sync separation is not used.
20	SEPIN	Vertical synchronization signal input. Tie to VDD1 if not used.
21	CTRL2	NTSC/PAL-M sync signal generation method select input. LOW for NTSC
22	CTRL3	SEPIN input control. $\overline{VSYNC}$ input signal when LOW
23	$\overline{RST}$	System reset input, with pull-up resistance
24	VDD1	5 V power supply for digital system

### SPECIFICATIONS

#### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{DD1}/V_{DD2}$	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
Input voltage range	$V_I$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Output voltage range	$V_O$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Power dissipation	$P_D$	350	mW
Operating temperature range	$T_{opr}$	-30 to 70	°C
Storage temperature range	$T_{stg}$	-40 to 125	°C

## LC7472M

### Recommended Operating Conditions

$T_a = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Logic supply voltage	$V_{DD1}$	5.0	V
Analog supply voltage	$V_{DD2}$	5.0	V
Logic supply voltage range	$V_{DD1}$	4.5 to 5.5	V
Analog supply voltage range	$V_{DD2}$	4.5 to $(1.27 \cdot V_{DD1})$	V

### Electrical Characteristics

$V_{DD1} = 5\text{ V}$ ,  $T_a = -30\text{ to }70\text{ }^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Logic supply current	$I_{DD1}$	All outputs open, 7.159 MHz crystal oscillator, 8 MHz LC oscillator	-	-	15	mA
Analog supply current	$I_{DD2}$	$V_{DD2} = 5\text{ V}$	-	-	20	mA
CVIN input leakage current	$I_{L1}$		-	-	1	$\mu\text{A}$
CVOUT output leakage current	$I_{L2}$		-	-	1	$\mu\text{A}$
CTRL1, CTRL2, CTRL3 and OSCIN LOW-level input current	$I_{L}$	$V_i = V_{SS1}$	-1.0	-	-	$\mu\text{A}$
$\overline{\text{RST}}$ , $\overline{\text{CS}}$ , SIN, SCLK, CTRL1, SEPIN, CTRL2 and CTRL3 HIGH-level input current	$I_{IH}$	$V_i = V_{DD1}$	-	-	1.0	$\mu\text{A}$
$\overline{\text{RST}}$ , $\overline{\text{CS}}$ , SIN and SCLK LOW-level input voltage	$V_{L1}$		$V_{SS} - 0.3$	-	$0.2V_{DD1}$	V
CTRL1, CTRL2, CTRL3 and SEPIN LOW-level input voltage	$V_{L2}$		$V_{SS} - 0.3$	-	$0.3V_{DD1}$	V
$\overline{\text{RST}}$ , $\overline{\text{CS}}$ , SIN and SCLK HIGH-level input voltage	$V_{IH1}$		$0.8V_{DD1}$	-	$V_{DD1} + 0.3$	V
CTRL1, CTRL2, CTRL3 and SEPIN HIGH-level input voltage	$V_{IH2}$		$0.7V_{DD1}$	-	$V_{DD1} + 0.3$	V
CVIN composite video input voltage	$V_{I1}$	Measured peak to peak	-	2.0	-	$V_{PP}$
SYNCIN composite video input voltage	$V_{I2}$	Measured peak to peak	-	2.0	2.5	$V_{PP}$
XIN input voltage	$V_{I3}$	External clock input, $f_{IN} = 7.159\text{ or }14.302\text{ MHz}$	0.20	-	5.0	$V_{PP}$
CSYNOUT, SYNC and SEPOUT LOW-level output voltage	$V_{OL1}$	$V_{DD1} = 4.5\text{ V}$ , $I_{OL} = 1.0\text{ mA}$	-	-	1.0	V
CSYNOUT, SYNC and SEPOUT HIGH-level output voltage	$V_{OH1}$	$V_{DD1} = 4.5\text{ V}$ , $I_{OH} = -1.0\text{ mA}$	3.5	-	-	V
CVOUT SYNC voltage	$V_{SN}$	$V_{DD2} = 5.0\text{ V}$	0.88	1.00	1.12	V
CVOUT pedestal voltage	$V_{PD}$		1.44	1.56	1.68	V
CVOUT LOW-level color bar strobe voltage	$V_{CBL}$		1.15	1.27	1.39	V
CVOUT HIGH-level color bar strobe voltage	$V_{CBH}$		1.75	1.87	1.99	V
CVOUT LOW-level background color voltage	$V_{RSL}$		1.59	1.71	1.83	V

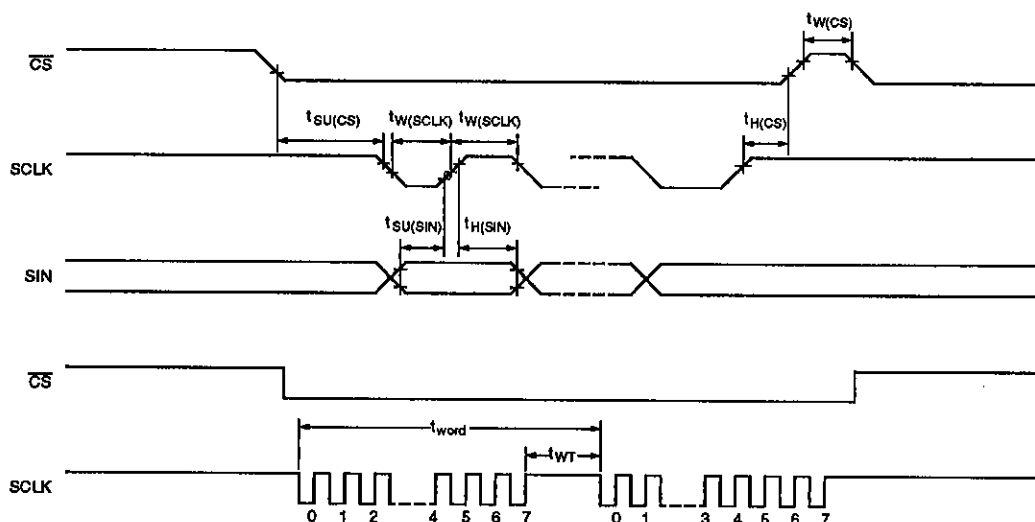
## LC7472M

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CVOUT HIGH-level background color voltage	$V_{RSH}$	$V_{DD2} = 5.0 \text{ V}$	2.12	2.24	2.36	V
CVOUT border voltage	$V_{BK}$		1.58	1.70	1.82	V
CVOUT character voltage	$V_{CHA}$		2.74	2.86	2.98	V
RST, $\overline{CS}$ , SIN and SCLK pull-up resistance	$R_{pu}$	Depends on optional settings at pins	25	50	90	k $\Omega$
XIN and XOUT oscillator frequency	$f_{osc1}$	NTSC (2isc)	–	7.159	–	MHz
		PAL-M (4isc)	–	14.302	–	MHz
OSCIN and OSCOUT oscillator frequency	$f_{osc2}$	LC oscillator	5	–	10	MHz

### Timing Characteristics

$V_{DD1} = 5 \pm 0.5 \text{ V}$ ,  $T_a = -30 \text{ to } 75 \text{ }^\circ\text{C}$

Parameter	Symbol	Rating			Unit
		min	typ	max	
SCLK input pulsewidth	$t_w(\text{SCLK})$	200	–	–	ns
$\overline{CS}$ HIGH-level input pulsewidth	$t_w(\overline{CS})$	1	–	–	$\mu\text{s}$
$\overline{CS}$ input setup time	$t_{su}(\overline{CS})$	200	–	–	ns
SIN data input setup time	$t_{su}(\text{SIN})$	200	–	–	ns
$\overline{CS}$ input hold time	$t_h(\overline{CS})$	2	–	–	$\mu\text{s}$
SIN data input hold time	$t_h(\text{SIN})$	200	–	–	ns
8-bit data word write time	$t_{word}$	4.2	–	–	$\mu\text{s}$
RAM data write time	$t_{WT}$	1	–	–	$\mu\text{s}$



## DISPLAY CONTROL FEATURES AND CHARACTERISTICS

### Display Control Command Structure

The display control commands, COMMAND0 to COMMAND5, are shifted in 8-bit serial units. The first byte of a command consists of an identification code and data. The second byte consists of data only. Once the command identification code in byte 1 has been

written, it is saved until the next time the first byte is written. If COMMAND1 is written, the display character write mode begins and the first byte does not change. When  $\overline{CS}$  is HIGH, COMMAND0 is set.

### Display Control Command Data

Command	First byte								Second byte							
	Command code				Data or register storing data				Data or register storing data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Display memory (VRAM) write address setting command	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Display character data write command	1	0	0	1	0	0	0	0	al	0	CS	C4	C3	C2	C1	C0
COMMAND2 Vertical display position and character size setting command	1	0	1	0	VS21	VS20	VS11	VS10	0	0	VP5	VP4	VP3	VP2	VP1	VP0
COMMAND3 Horizontal display position and character size setting command	1	0	1	1	HS21	HS20	HS11	HS10	0	0	HP5	HP4	HP3	HP2	HP1	HP0
COMMAND4 Display control setting command	1	1	0	0	TST MOD	CB	OSC STP	SYS RST	0	0	NON	EG	BK1	BK0	RV	DSP ON
COMMAND5 Synchronization signal control setting command	1	1	0	1	PH1	PH0	BCL	INT	0	0	0	0	SN3	SN2	SN1	SN0

**COMMAND0: Display Memory Write Address Setting Command****COMMAND0: first byte**

DA0 to DA7	Register name	Register Contents		Remarks		
		Status	Function			
0	V0	0	Display memory address 0 to 9H			
		1				
1	V1	0				
		1				
2	V2	0				
		1				
3	V3	0				
		1				
4	-	0			COMMAND0 identification code	
5	-	0				
6	-	0				
7	-	1				

**COMMAND0: second byte**

DA0 to DA7	Register name	Register Contents		Remarks		
		Status	Function			
0	H0	0	Display memory address 0 to 17H			
		1				
1	H1	0				
		1				
2	H2	0				
		1				
3	H3	0				
		1				
4	H4	0				
		1				
5	-	0				
6	-	0				
7	-	0				

**Note**

On system reset with  $\overline{RST}$ , the status of all registers is set to 0.

**COMMAND1: Display Character Data Write Command****COMMAND1: first byte**

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	-	0		
1	-	0		
2	-	0		
3	-	0		
4	-	1	COMMAND1 identification code	After command is input, display character data write mode is set until $\overline{CS}$ is set HIGH.
5	-	0		
6	-	0		
7	-	1		

**COMMAND1: second byte**

DA0 to DA7	Register name	Register Contents		Remarks		
		Status	Function			
0	C0	0	Character code 0 to 3FH			
		1				
1	C1	0				
		1				
2	C2	0				
		1				
3	C3	0				
		1				
4	C4	0				
		1				
5	C5	0				
		1				
6	-	0				
7	at	0			Character attribute OFF	
		1			Character attribute ON	

**Note**

On system reset with  $\overline{RST}$ , the status of all registers is set to 0.

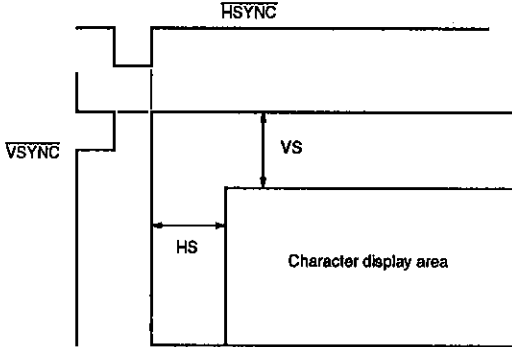


**COMMAND2: Vertical Display Position and Character Size Setting Command**

**COMMAND2: first byte**

DA0 to DA7	Register name	Register Contents			Remarks	
		Status	Function			
0	VS10	0	VS11	VS10	First row vertical character size	
		1	0	0		1H/pixel
		0	0	1		2H/pixel
1	VS11	0	1	0		3H/pixel
		1	1	1		1H/pixel
2	VS20	0	VS21	VS20		Second row vertical character size
		1	0	0	1H/pixel	
3	VS21	0	0	1	2H/pixel	
		1	1	0	3H/pixel	
4	-	0	COMMAND2 identification code			
5	-	1				
6	-	0				
7	-	1				

**COMMAND2: second byte**

DA0 to DA7	Register name	Register Contents		Remarks		
		Status	Function			
0	VP0	0	Initial vertical coordinate position determined by $VS = H \times \left( 2 \sum_{n=0}^5 2^n VP_n \right)$ where H is the horizontal synchronization pulse period.  	The initial vertical coordinate position is set in 6 bits, VP0 to VP5, where the lsb, VP0, corresponds to 2H.		
		1				
1	VP1	0				
		1				
2	VP2	0				
		1				
3	VP3	0				
		1				
4	VP4	0				
		1				
5	VP5	0				
		1				
6	-	0				
7	-	0			Second byte identification bit	

**Note**

On system reset with  $\overline{RST}$ , the status of all registers is set to 0.

**COMMAND3: Horizontal Display Position and Character Size Setting Command**

**COMMAND3: first byte**

DA0 to DA7	Register name	Register Contents			Remarks	
		Status	Function			
0	HS10	0	HS11	HS10	First row horizontal character size	
		1	0	0		1T <sub>C</sub> /pixel
1	HS11	0	0	1		2T <sub>C</sub> /pixel
		1	1	0		3T <sub>C</sub> /pixel
2	HS20	0	0	0		1T <sub>C</sub> /pixel
		1	1	1		1T <sub>C</sub> /pixel
3	HS21	0	0	1	2T <sub>C</sub> /pixel	
		1	1	0	3T <sub>C</sub> /pixel	
4	-	1	COMMAND3 identification code			
5	-	1				
6	-	0				
7	-	1				

**COMMAND3: second byte**

DA0 to DA7	Register name	Register Contents		Remarks		
		Status	Function			
0	HP0	0	The initial horizontal coordinate position is given by $HS = T_C \times \left( 2 \sum_{n=0}^5 2^n HP_n \right)$ where T <sub>c</sub> is the OSCIN and OSCOUT operation mode oscillation period.	The initial horizontal coordinate position is set in 6 bits, HP0 to HP5, where the 1sb, HP0, corresponds to 2T <sub>C</sub> .		
		1				
1	HP1	0				
		1				
2	HP2	0				
		1				
3	HP3	0				
		1				
4	HP4	0				
		1				
5	HP5	0				
		1				
6	-	0				
7	-	0			Second byte identification bit	

**Note**

On system reset with  $\overline{RST}$ , the status of all registers is set to 0.

**COMMAND 4: Display Control Setting Command****COMMAND4: first byte**

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	SYSRST	0	Resets all registers and turns the display OFF when HIGH	A system reset also occurs when $\overline{CS}$ goes LOW.
		1		
1	OSCSTP	0	Crystal and LC oscillator circuitry enable when LOW	External synchronization is effective only when the character display is OFF.
		1		
2	CB	0	Color bar strobe signal is output when LOW.	When BCL is HIGH only.
		1		
3	TSTMOD	0	Test operation mode when HIGH	Test mode should not be selected during normal operation.
		1		
4	-	0	COMMAND4 identification code	
5	-	0		
6	-	1		
7	-	1		

**COMMAND4: second byte**

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	DSPON	0	Character display ON when HIGH	
		1		
1	RV	0	Inverse characters ON when HIGH	
		1		
2	BK0	0	Blinking ON when HIGH	When blinking inverse characters, characters alternate between normal and inverse.
		1		
3	BK1	0	Blinking period 0.5 s	Selects blinking period.
		1	Blinking period 1.0 s	
4	EG	0	Border OFF	
		1	Border ON	
5	NON	0	Interlaced scanning, 262.5 H/field	
		1	Non-interlaced scanning, 263 H/field	
6	-	0		
7	-	0	Second byte identification bit	

**Note**

On system reset with  $\overline{RST}$ , the status of all registers is set to 0.

**COMMAND5: Synchronization Signal Control Setting Command**

**COMMAND5: first byte**

DA0 to DA7	Register name	Register Contents			Remarks									
		Status	Function											
0	INT	0	External synchronization											
		1	Internal synchronization											
1	BCL	0	Background color when LOW		Only available with internal synchronization									
		1												
2	PH0	0	<table border="1"> <thead> <tr> <th>PH1</th> <th>PH0</th> <th>Phase</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td><math>\pi/2</math></td> </tr> <tr> <td>0</td> <td>1</td> <td><math>\pi</math></td> </tr> </tbody> </table>		PH1	PH0	Phase	0	0	$\pi/2$	0	1	$\pi$	Phase selection. In PAL-M mode, there is only one background color (blue-black). Otherwise, there are 4 types.
		PH1	PH0	Phase										
0	0	$\pi/2$												
0	1	$\pi$												
1	<table border="1"> <tbody> <tr> <td>1</td> <td>0</td> <td><math>3\pi/2</math></td> </tr> <tr> <td>1</td> <td>1</td> <td>In phase</td> </tr> </tbody> </table>		1	0	$3\pi/2$	1	1	In phase						
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1	1	In phase												
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		1	0	$3\pi/2$										
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1	1	In phase												
4	-	1	COMMAND5 identification code											
5	-	0												
6	-	1												
7	-	1												

**COMMAND5: second byte**

DA0 to DA7	Register name	Register Contents					Remarks																														
		Status	Function																																		
0	SN0	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SN0</th> <th>Detection frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>No detection</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>16 times</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>32 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>64 times</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>128 times</td> </tr> </tbody> </table>				SN3	SN2	SN1	SN0	Detection frequency	0	0	0	0	No detection	0	0	0	1	16 times	0	0	1	0	32 times	0	1	0	0	64 times	1	0	0	0	128 times	External, horizontal synchronization signal detection
		SN3					SN2	SN1	SN0	Detection frequency																											
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0	0	0	1	16 times																																	
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1	SN1	0	<table border="1"> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>No detection</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>16 times</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>32 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>64 times</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>128 times</td> </tr> </tbody> </table>				0	0	0	0	No detection	0	0	0	1	16 times	0	0	1	0	32 times	0	1	0	0	64 times	1	0	0	0	128 times	External, horizontal synchronization signal detection					
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4	-	0																																			
5	-	0																																			
6	-	0																																			
7	-	0	Second byte identification bit																																		

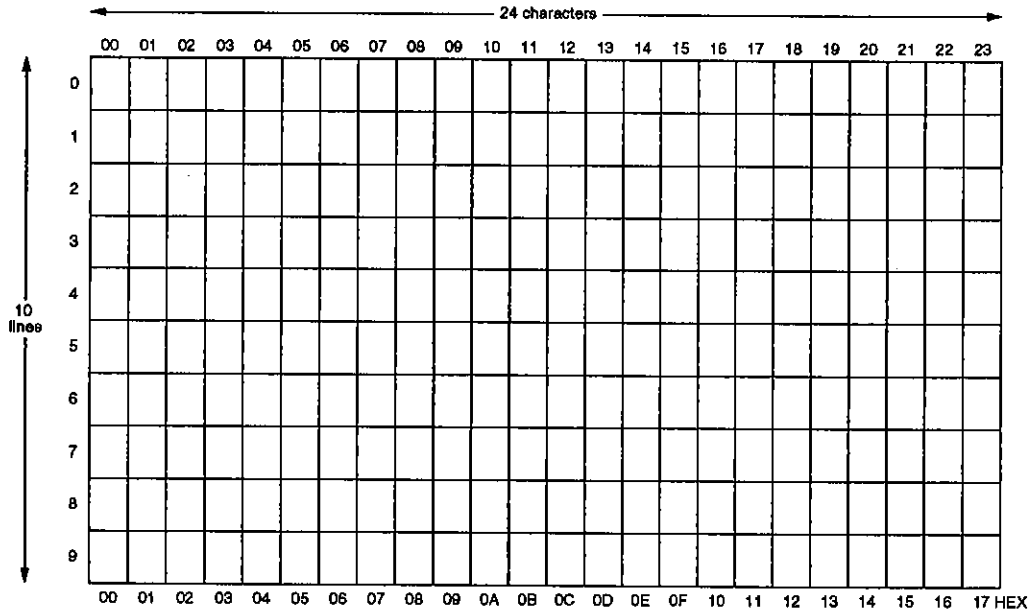
**Note**

On system reset with  $\overline{RST}$ , the status of all registers is set to 0.

### Display Configuration

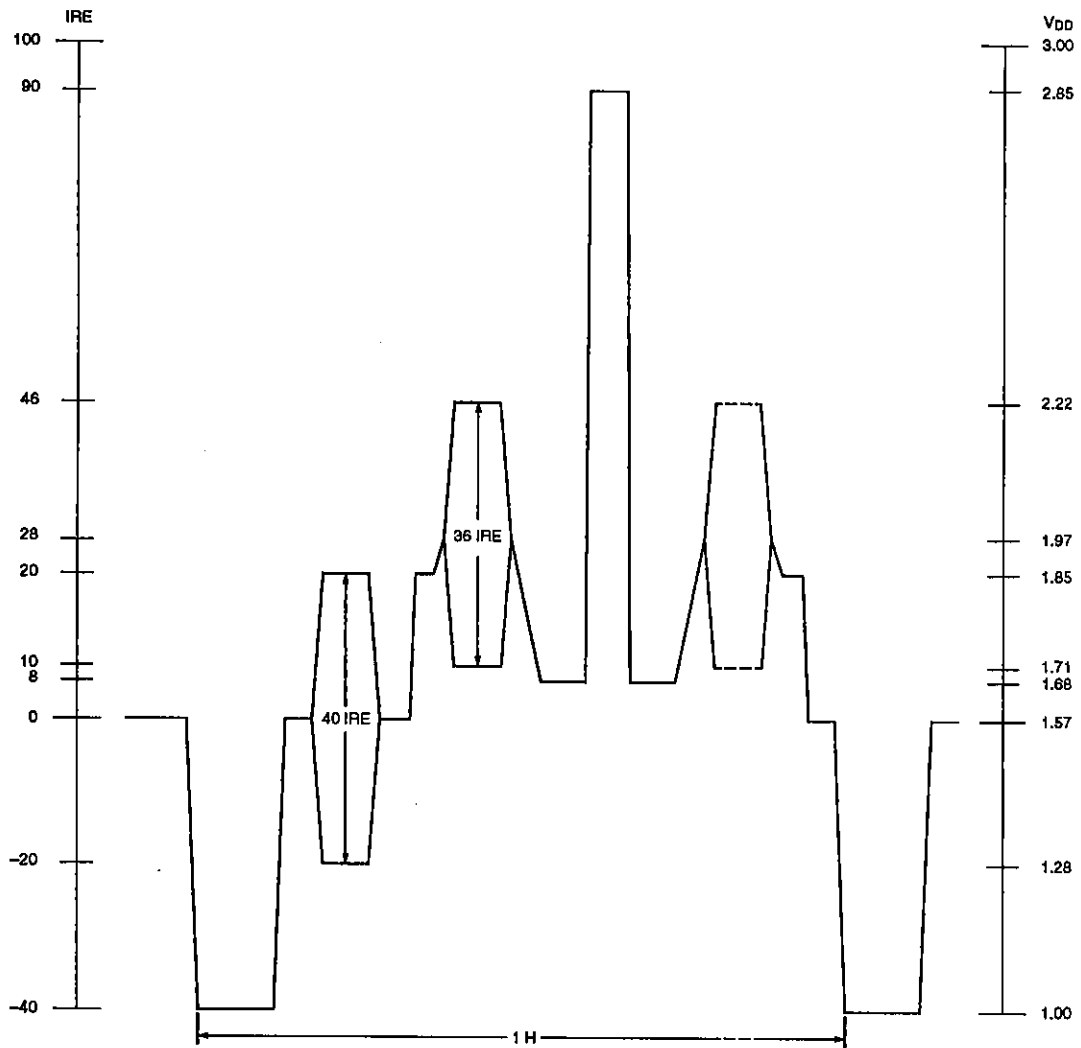
The display is 24 characters by 10 rows large. Up to 240 characters can be displayed, unless the character size is expanded. The display memory address is set as a row

address in the range 0 to 9 and a column address in the range 0 to 23.



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Composite Video Output



Relative carrier amplitude (IRE)	Output voltage amplitude (V)
100	3.000
90	2.857
46	2.228
20	1.857
10	1.714
8	1.685
0	1.571
-20	1.285
-40	1.000

Note

$V_{DD2} = 5.0 \text{ V}$