

No. X 4604A

LC8211

# Halftone Processing IC for Fax, Copier and Scanner

## **Preliminary**

## Overview

The LC8211 inputs the multi-level image data output from the LC8210 (multi-level image processing IC), and performs a process to create high quality binary image data. The LC8211 can be applied to OA equipments such as G3 and G4 facsimiles, image file systems, digital photocopiers and image scanners. The multi-level data is segmented into areas of character, photographs and screened halftone areas, and performs binary coding using various advanced processing methods.

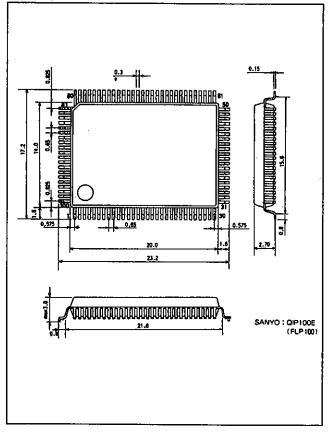
#### **Features**

- No. of processed pixels 8192pixels/line max.
   The number of pixels can be set in pixel units.
- · Processing speed: 200ns/pixel max
- Document segmentation (characters, photographs, screened halftone areas)
- Simple binary coding process (fixed threshold, density adaptive threshold)
- Simulated halftone process
   Structural dither method (64-tone) Dither threshold value can be set.
   Error diffusion method (64-tone)
- Image reduction Image data compression, black fine line retention, white fine line retention
- Single 5V power supply and low power consumption using CMOS

# **Package Dimensions**

(unit: mm)

### 3151-QIP100E



#### **Specifications**

Absolute maximum ratings at Ta = 25°C, GND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max		- 0.3 to + 7.0	V
Input/output voltage	V <sub>I</sub> , V <sub>O</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V
Operation ambient temperature	Topr		- 30 to + 70	°C
Storage ambient temperature	Tstg		- 55 to + 125	°C
Soldering heat resistance		10s	235	°C

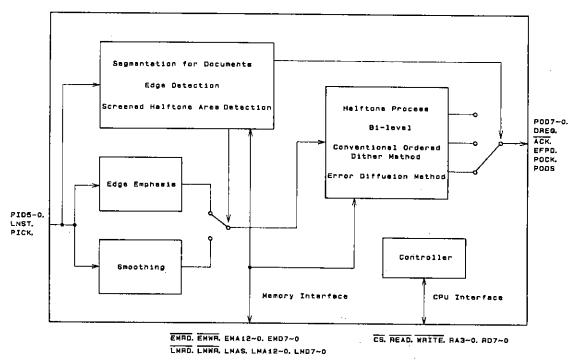
Allowable Operating Ranges at Ta = -30 to +70°C, GND = 0V

Parameter	Sumbal		Ratings		
ratameter	Symbol	min	typ	max	Unit
Power voltage	V <sub>DD</sub>	4.5		5.5	V
Input voltage	V <sub>IN</sub>	0		V <sub>DD</sub>	٧

DC Characteristics at  $Ta = -30 \text{ to } +70^{\circ}\text{C}$ , GND = 0V,  $V_{DD} = 4.5 \text{ to } 5.5V$ 

Parameter	Sumbal	Complished a		Ī., .		
raiailletei	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V <sub>IH</sub>		2.2			٧
Input low level voltage	V <sub>IL</sub>				0.8	V
Output high level voltage	VoH	I <sub>OH</sub> = -3mA	2.4		· ·	V
Output low level voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3mA			0.4	V
Current consumption	I <sub>DD</sub>	$V_{DD} = 5.0V$ SYSCLK = 20MHz		15	23	mA

# **Block Diagram**



A01570

## **Pin Functions**

			Туре		
	Input pin	В	Bidirectional pin	NC	Not connected
0	Output pin	Р	Power pin		

Pin No.	Pin name	Туре	Function
99	RD0	В	
100	RD1	В	
1	RD2	В	
2	RD3	В	
3	RD4	В	The CPU interface data bus terminal. RD7 is the MSB terminal, and RD0 is the LSB terminal.
4	RD5	В	the rise terminary and resorts the LSD terminar.
5	RD6	В	
6	RD7	В	
7	RA0	ı	
8	RA1	1	The CPU interface address bus terminal.
9	RA2	I	RD3 is the MSB terminal, and RA0 is the LSB terminal.
10	RA3	1	,
11	<u>cs</u>	1	CPU interface chip select signal terminal
12	READ	1	CPU interface READ signal terminal
13	WRITE	-	CPU interface WRITE signal terminal
14	RESET	_	System reset terminal
15	GND	Р	Ground terminal
16	VDD	Р	Power terminal
17	LMD0	В	
18	LMD1	В	
19	LMD2	В	
20	LMD3	В	Line memory data bus terminal.
21	LMD4	В	LMD7 is the MSB terminal, and LMD0 is the LSB terminal.
22	LMD5	В	
23	LMD6	В	
24	LMD7	В	
25	GND	Р	ground terminal

Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Туре	Function
26	LMA0	0	
27	LMA1	0	
28	LMA2	0	
29	LMA3	0	
30	LMA4	0	
31	LMA5	0	line memory address by stansacing 1
32	LMA6	0	Line memory address bus terminal  LMA12 is the MSB terminal, and LMA0 is the LSB terminal.
33	LMA7	0	LANCE 13 the MISS terminal, and LIMAG is the LSB terminal.
34	LMA8	0	
35	LMA9	0	
36	LMA10	0	
37	LMA11	0	
38	LMA12	0	
39	LMAS	0	Line memory line identification terminal
40	GND	Р	Ground terminal
41	VDD	Р	Power terminal
42	LMRD	0	Line memory READ terminal
43	LMWR	0	Line memory WRITE terminal
44	EMD0	В	
45	EMD1	В	
46	EMD2	В	
47	EMD3	В	Error diffusion memory data bus terminal
48	EMD4	В	EMD7 is the MSB terminal, and EMD0 is the LSB terminal.
49	EMD5	В	
50	EMD6	В	
51	EMD7	В	
52	GND	Р	Ground terminal
53	EMA0	0	
54	EMA1	0	
55	EMA2	0	
56	EMA3	0	Error diffusion memory address bus terminal
57	EMA4	0	EMA12 is the MSB terminal, and EMA0 is the LSB terminal.
58	EMA5	0	
59	EMA6	0	
60	EMA7	0	
61	EMA8	0	

Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Туре	Function
62	EMA9	0	
63	EMA10	0	Error diffusion memory address bus terminal
64	EMA11	0	EMA12 is the MSB terminal, and EMA0 is the LSB terminal.
65	EMA12	0	
66	VDD	Р	Power terminal
67	GND	Р	Ground terminal
68	EMRD	0	Error diffusion memory READ signal terminal
69	EMWR	0	Error diffusion memory WRITE signal terminal
70	PID0	1	
71	PID1		
72	PID2	_	Multi-level image data input terminal
73	PID3	_	PID5 is the MSB terminal, and PID0 is the LSB terminal.
74	PID4	_ :	
75	PID5	_	·
76	PICK		Multi-level image data transfer clock
77	LNST	_	Multi-level image line synchronous signal
78	POD0	0	
79	POD1	0	
80	POD2	0	
81	POD3	0	
82	POD4	0	Binary image data parallel data bus
83	POD5	0	POD7 is the new data, and POD0 is the old data.
84	POD6	0	
85	POD7	0	
86	PODS	0	Binary image data serial data bus
87	POCK	0	Binary image data serial transfer clock
88	EFPD	0	Binary image data output valid period signal
89	VDD	Р	Power terminal
90	GND	Р	Ground terminal
91	DREQ	0	DMA data request signal
92	ACK	I	DMA acknowledge input
93	CLKIN	ı	System clock
94	MTP	0	Motor drive timing signal
95	NC	NC	
96	NC	NC	
97	TEST	ı	Test terminal (normal grounding)
98	GND	Р	Ground terminal

## **AC Characteristics**

When GND=0V,  $V_{DD}$ =4.5 to 5.5V, Ta=-30 to +70°C,  $C_L$ =50pF and high level voltage is 2.2V and low level voltage is 0.8V.

## **Input Clock**

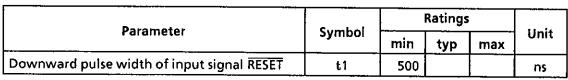
Parameter  Cycle time of input signal SYSCLK	Cl. al		Ratings			
	Symbol	min typ max			Unit	
Cycle time of input signal SYSCLK	t1	50			ns	

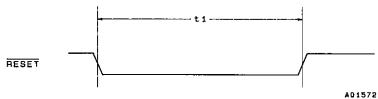
Note: The clock duty must be set to 50%.

A01571



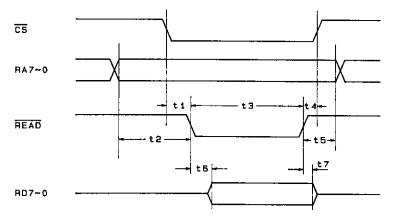
#### Reset





## **CPU Interface (READ)**

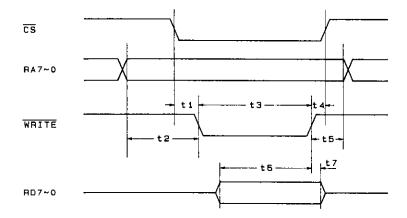
Davamatav	S1 -1		Ratings	;		
Parameter	Symbol	min	typ	max	Unit	
For READ ↓, CS setup time	t1	20	-		ns	
For READ ↓, RA7 to 0 setup time	t2	20		7.	ns	
READ pulse width	t3	50			ns	
For READ ↑, CS hold time	t4	20			ns	
For READ ↑, RA7 to 0 hold time	t5	20			ns	
For READ ↓, RD7 to 0 delay time	t6			40	ns	
For READ ↑, RD7 to 0 delay time	t7	0	****	20	ns	



A01573

#### **CPU Interface (WRITE)**

Darameter	Completel.		Ratings	latings		
Parameter	Symbol	min	typ	max	Unit	
For WRITE \$\psi\$, CS setup time	t1	20			ns	
For WRITE ↓, RA7 to 0 setup time	t2	20			ns	
WRITE pulse width	t3	50			ns	
For WRITE ↑, CS hold time	t4	20		"	ns	
For WRITE ↑, RA7 to 0 hold time	t5	20			ns	
For WRITE ↑, RD7 to 0 setup time	t6	20			ns	
For WRITE ↑, RD7 to 0 hold time	t7	10			ns	



A01574

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
  - 2 Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.