CMOS LSI

LC82220

# SANYO

# Motion JPEG Decoder LSI

## Preliminaly

### **Overview**

The LC82220 is a single-chip JPEG decoder designed for wide range of digital video playback applications including amusement systems, video games and PC JPEG playback cards. The LC82220 is capable of decoding JPEG bitstreams of SIF resolution with a picture rate of 30 frames/sec. The digital video output can be formatted for NTSC, PAL, SECAM, or any other optional video standard. The complete decoding function is realised with the LC82220, a standard 8-bit or 16-bit microcontroller and a bank of DRAM. A typical memory configuration is a single 128 k × 16 or 256 k × 16 DRAM. The LC82220 also supports efficient video display functions such as scroll and overlay.

## **Functions**

- Support for JPEG format
- Real-time decoding of motion-JPEG with rate of 30 frames/sec
- Lowest solution cost for amusement, game, PC systems
- Support for YUV 4:1:1 color format
- YUV or RGB digital video outputs compatible with optional video format
- Programmable picture and display window format
- Support for trick display: scrolling, overlaying
- Standard 8/16-bit microcontroller interface with DMA support for compressed data input
- Support SOI and EOI markers
- Direct connect to video DAC
- Direct connect to 2 M or 4 M DRAM as bit and frame buffers
- Two Q-tables included
- High-speed processing by fixed Huffman tables

# **Package Dimensions**

unit: mm

#### 3182-QFP128E



#### **Block Diagram**



#### **Pin Assignment**



A05631

#### **Pin Functions**

Pin No.	Symbol	I/O	Function
1	V <sub>DD</sub>		+5 V power supply
2	ZCTLINT	0	Control bus interrupt request (open drain output)
3	ZCTLCS	Ι	Control bus select
4	ZCTLRD	I	Control bus read or R/W select
5	ZCTLWR	I	Control bus write or Data strobe
6	ZCTLRDY	0	Control bus ready (tristate output)
7	TEST3	1	Test pin
8	TEST4	1	Test pin
9	CTLA5	1	
10	CTLA4	-	
11	CTLA3		
12	CTLAS CTLA2	1	Control bus address
12	CTLA2 CTLA1	1	
13	CTLA0		
		-	
15	CTLCPU	Ι	Control bus CPU type selection
16	V <sub>DD</sub>		+5 V power supply
17	V <sub>SS</sub>		Ground
18	CTLD7	I/O	
19	CTLD6	I/O	
20	CTLD5	I/O	
21	CTLD4	I/O	Control bus data
22	CTLD3	I/O	- Control bus data
23	CTLD2	I/O	
24	CTLD1	I/O	
25	CTLD0	I/O	1
26	TEST0	I	Test pin
27	ZRESET	I	Hardware reset
28	CLKSEL0	I	Clock divisor setting
29	CLKSEL1	I	CLKSEL1:0 = 00: no divisor, 01: clock divided by 2, 10: clock divided by 3
30	CLK	I	System (decode) clock input (CMOS level input)
31	TEST1	1	Test pin
32	V <sub>DD</sub>		+5 V power supply
33	V <sub>SS</sub>		Ground
34	ZCDCS/ZCDACK	1	Code bus select or Code bus DMA acknowledge
35	ZCDINT/ZCDREQ		Code bus interrupt or Code bus DMA request
36	ZCDWR	1	Code bus data write signal
37	ZCDRDY	0	Code bus ready (tristate output)
37	CCD15	1	יייייייייייייייייייייייייייייייייייייי
38	CCD15 CCD14	1	Code bus data
40	CCD13		
41	CCD12	1	
42	CCD11	-	
43	CCD10	1	
44	CCD9	1	
45	CCD8	Ι	
46	CCD7	I	
47	CCD6	Ι	
48	V <sub>SS</sub>		Ground
49	V <sub>DD</sub>		+5 V power supply
50	CCD5	I	
	CCD4	I	Code bus data
51			
51 52	CCD3	I	Code bus data
			Code bus data
52	CCD3 CCD2 CCD1		Code bus data

Continued on next page.

Continued from preceding page.

Sec         OEF         O           67         DP6         O           68         DP6         O           88         DB4         O           00         DC8         O           61         DB2         O           62         DB1         O           63         DB0         O           64         Vigs         Ground           65         ZBLAWK         O           66         ZPKN         I           70         DG4 data mable signal           66         ZELAWK         O           67         ZPKN         I           70         DG7         O           71         DG7         O           72         DG8         O           73         DG3         O           74         DG4         O           75         DG3         O           76         DG3         O           77         DG1         O           78         DG2         O           79         TEST2         I         Test pin           80         OR4         O           81 <th>Pin No.</th> <th>Symbol</th> <th>I/O</th> <th>Function</th>	Pin No.	Symbol	I/O	Function
S8         DBs         0           69         DB4         0           60         DB3         0           61         DR2         0           62         DB4         0           63         DB0         0           64         Vsp.         Ground           65         Vn.0         -sV.power supply           66         ZELNNK         0         Banking signal           67         ZPKEN         1         Pixel data snable signal           68         PCLK         1         Pixel data snable signal           69         ZVSVNC         1         Venci strain snable signal           70         ZSVNC         1         Venci strain snable signal           71         DG7         0         Pixel data bus G (/)           73         DG3         0         Pixel data bus G (/)           74         DG4         0         Pixel data bus G (/)           78         DG2         0         Pixel data bus G (/)           79         TES1z         1         Test pin           81         Vp0         -5 V power supply           81         NPS         Ground           82 <td>56</td> <td></td> <td>0</td> <td></td>	56		0	
99         DB4         0           60         DB3         0           61         DB2         0           62         DB1         0           63         DB0         0           64         Vg0         450           64         Vg0         650           64         Vg0         650           65         Vg0         650           77         DG4         0           78         ZVSNC         1           98         ZVSNC         1           97         DG5         0           73         DG5         0           74         DG4         0           75         DG3         0           76         DG2         0           77         DG1         0           78         DG3         0           78         DG3         0           79         TST2         1         Test pin           78         DG3         0           79         TST2         1         Stapin           78         DG3         0           79         TST2         1         St	57	DB6	0	Pixel data bus B (V)
00DB3061DB40620063DB0064Vys-65Vys-672PXEN168PXCLK1702PXSVNC171DO7072DO6073DO3074DO4075DO3076DO3077DO4078DO3079TEST2170CO4078DO3079TEST2170CO4078DO3079TEST2179TEST2170CO4078DO3079TEST2170CO4078DO5079TEST2170CO4079TEST2170CO4071DO4072DO5073DO5074DO5075CO3076TEST2177DO4078CO4079TEST2179TEST2179CO4079CO4079CO4079CO20<	58	DB5	0	
60         DB3         0           61         DB2         0           62         DB1         0           63         DD0         0           64         Vss         -         Ground-           65         Vsp         -         Standardian and signal           66         ZXENK         0         Banking signal           67         ZYKNK         1         Poel dock           68         PXCLK         1         Poel dock           69         ZVSYNC         1         Hotocontal synchronizing signal           70         ZMSNNC         1         Hotocontal synchronizing signal           71         DG6         0         77           73         DG6         0           74         DG4         0           75         DG3         0           76         DG2         0           77         DG1         0           78         TST2         I         Test pin           79         TSTS12         I         Test pin           80         DR1         0         Ground           81         DR2         O           84<	59	DB4	0	
62         DB1         O           63         DB0         O           64         V <sub>55</sub> Ground           65         V <sub>00</sub> +5V power supply           66         ZZNNK         I         Pixel data anable signal           67         ZZNNK         I         Pixel data anable signal           68         ZXNK         I         Vectoal synchronizing signal           70         ZVSTNC         I         Hotizotal synchronizing signal           71         DG7         O           72         DG6         O           73         DG3         O           74         DG4         O           75         DG3         O           76         DG4         O           77         DG6         O           78         DG9         O           79         TEST2         I         Test pin           80         Vp0         45 V power supply           81         Vp3         Ground           82         DR7         O           84         DR3         O           90         Vp35         Ground           88	60	DB3	0	
63         DB0         O           64         V <sub>38</sub> Ground           65         V <sub>30</sub>	61	DB2	0	-
64         V <sub>88</sub> Cound           66         V <sub>00</sub> -45 Voore supply           67         2PXEN         1         Pixel data enable signal           68         2XSVNC         1         Pixel data enable signal           68         2XSVNC         1         Pixel data enable signal           68         PXCLK         1         Pixel data enable signal           68         PXCLK         1         Hotschronizing signal           70         ZVSYNC         1         Hotschronizing signal           71         DG7         O           72         DG6         O           73         DG3         O           74         DG4         O           75         DG3         O           76         DG2         O           77         DG1         O           78         TEST2         I           80         Vop         +5 V power supply           81         Vys         Ground           82         DR7         O           84         DR4         O           96         DR3         O           97         Vzs         Ground	62	DB1	0	-
65         V <sub>DD</sub> +5V power supply           66         ZBLANK         0         Binkings ajgral           67         ZPKEN         1         Pixel data enable signal           68         PXCLK         1         Pixel data enable signal           68         PXCLK         1         Pixel data enable signal           70         ZHSYNC         1         Horizontal synchronizing signal           71         DG6         0           73         DG5         0           74         DG4         0           75         DG3         0           78         DG2         0           79         TET2         1           78         DG9         0           79         TET2         1           78         DG9         0           79         TET2         1           78         Ground         45 V power supply           81         V <sub>85</sub> Ground           82         DR4         0           83         DR4         0           84         DR4         0           85         DR4         0           86 <td< td=""><td>63</td><td>DB0</td><td>0</td><td>-</td></td<>	63	DB0	0	-
66Vo++V power supply66ZBLANK0Blanking signal67ZPXEN1Pixel data enable signal68PXCLK1Pixel data enable signal69ZXVSNC1Ventical synchronicing signal70Z1SYNC1Horizontal synchronicing signal71DG7073DG6074DG4075DG3076DG2077DG6078DG6079TEST2178DG7078DG6079TEST2178DG6079TEST2180Vo+5 V power supply81VagGround82DR4083DR6084DR3085DR4086DR3087DR4088DR1089Vo45 V power supply91ZZEL092ZZNEL093ZRAS094ZZOSL095ZWEH/ZCASH096Vo+5 V power supply*97VyS98MD151099MD141091MD131091MD141091MD141091MD1410 </td <td>64</td> <td>V<sub>SS</sub></td> <td></td> <td>Ground</td>	64	V <sub>SS</sub>		Ground
66         ZBLANK         0         Blanking signal           67         ZPXEN         1         Pixel data analo is signal           68         PXCLK         1         Pixel data analo is signal           69         ZVSYNC         1         Horizontal synchronizing signal           70         ZPKPNC         1         Horizontal synchronizing signal           71         DG5         0           72         DG6         0           73         DG5         0           74         DG4         0           75         DG3         0           76         DG0         0           77         DG6         0           78         DG0         0           79         TEST2         1         Feet pin           80         Voo         +5 V power supply           81         DR5         0           82         DR7         0           83         DR6         0           84         DR5         0           85         DR3         0           86         DR1         0           91         ZZVEL         0         Memory urite enable (L) <td>65</td> <td></td> <td></td> <td>+5V power supply</td>	65			+5V power supply
67         27×EN         1         Pixel data enable signal           68         PXCLK         1         Pixel data chable signal           69         ZVSYNC         1         Pixel data (chable)           70         ZHSYNC         1         Halacontal synchronizing signal           71         DG7         0         Constraint synchronizing signal           72         DG8         0           73         DG4         0           74         DG4         0           75         DG3         0           76         DG2         0           77         DG5         0           78         DG0         0           79         TESt2         1         Test pin           78         DG0         0           79         TESt2         1         Test pin           81         Vsp         Ground           82         DR7         0           83         DR6         0           84         DR5         O           85         DR4         0         Memory withe enable (1)           80         DR0         0           90         Vsp	66		0	
68         PXCLK         1         Pixel clock           69         ZVSYNC         1         Vertical synchronizing signal           70         ZZHSYNC         1         Horizontal synchronizing signal           71         DG3         0           72         DG4         0           73         DG3         0           74         DG4         0           75         DG3         0           76         DG2         0           77         DG1         0           78         DG0         0           79         TEST2         1         Test pin           80         Vos         afs V power supply         afs v power supply           81         Vss         Ground         afs up not power supply           82         DR4         0         pixel data bus R (Y)           84         DR5         0         Memory output enable           92         ZWEL         0         Memory write enable (L)           83         DR4         0         Memory write enable (L)           93         ZRAS         0         Row address strobe (L)           94         ZCSALH         0 <t< td=""><td></td><td></td><td></td><td></td></t<>				
69         ZVSYNC         1         Vertical synchronizing signal           70         ZHSYNC         1         Horizontal synchronizing signal           71         DG6         0           72         JOG6         0           73         DG6         0           74         DG7         0           75         DG3         0           76         JOG2         0           77         DG1         0           78         DG0         0           79         TEST2         1         Test pin           80         Vb0         1         45 V power supply           81         Vss         Ground         Ground           82         DR7         0         Ground           84         DR5         0         Memory unique nable           85         DR3         0         Ground           86         DR4         0         Memory unique nable           91         ZOE         0         Memory unique nable           92         ZWEJ         0         Memory unique nable           93         ZRA5         0         Ground           94         ZCASL			1	
70         ZHSYNC         1         Horizontal synchronizing signal           71         DG6         O           72         DG68         O           73         DG5         O           74         DG4         O           75         DG3         O           76         DG2         O           77         DG1         O           78         DG9         O           79         TES12         I           80         Vpo         Fets / Power supply           81         DR6         O           82         DR7         O           83         DR6         O           84         DR5         O           85         DR4         O           86         DR1         O           87         DR2         O           88         DR1         O           90         Vss         Ground           91         ZOE         Memory output enable           92         ZVEL         O         Memory output enable           93         ZRAS         O         Row address strobe           94         Vpoo			1	
71         DG7         0           72         DG6         0           73         DG5         0           74         DG4         0           76         DG2         0           77         DG1         0           78         DG0         0           77         DG1         0           78         DG0         0           79         TES12         1           80         V <sub>D0</sub> 45 V power supply           81         V <sub>S8</sub> Ground           82         DR7         0           83         DR6         0           84         DR5         0           85         DR4         0           86         DR3         0           87         DR2         0           88         DR0         0           91         ZOE         0           93         ZRAS         0           94         ZOEL         0           95         ZWEHZCASH         0           96         V <sub>D0</sub> +5 V power supplyr <sup>1</sup> 97         V <sub>S8</sub> Ground      <				
72         DG6         0           73         DG5         0           74         DG4         0           75         DG3         0           76         DG2         0           77         DG1         0           78         DG0         0           78         DG0         0           78         DG0         0           79         TEST2         1         Test pin           80         Vp0         +5 V power supply           81         Vg8         Ground           82         DR7         0           84         DR5         0           84         DR4         0           86         DR4         0           87         DR2         0           88         DR1         0           90         Vg5         Ground           91         ZOE         0           93         ZRAS         0           94         ZOEL         0           95         Memory vutie enable (L)           96         Vp0         +5 V power supply**           97         Vg8         Ground				
73         DGS         0           74         DG4         0           75         DG2         0           76         DG2         0           77         DG1         0           78         DG0         0           79         TEST2         1         Test pin           80         Vpp         45 V power supply           81         Vps         6 Ground           82         DR4         0           84         DR5         0           84         DR5         0           86         DR3         0           87         DR2         0           88         DR1         0           99         DR0         0           90         Vss         Ground           91         ZOE         Memory output enable           92         ZWEL         0         Memory output enable           93         ZAAS         0         Row address strobe           94         ZOE         0         Memory write enable (L)           95         ZWEH/ZASH         0         Memory write enable (L)           96         MD15         I/O<				-
74         DG4         0           75         DG3         0           76         DG2         0           77         DG1         0           78         DG0         0           78         DG0         0           78         DG0         0           79         TEST2         1         Test pin           80         Vpo         -5 V power supply           81         Vgs         Ground           82         DR7         0           84         DR5         0           84         DR5         0           86         DR1         0           87         DR2         0           88         DR1         0           91         ZOE         0         Memory uput enable           91         ZOE         0         Memory uput enable (L)           92         ZWAL         0         Memory uput enable (L)           93         DV0         0         Kernory uput enable (L)           94         ZCASL         0         Column address strobe (L)           95         ZWEL/CASH         0         Memory write enable (H)/column address strobe				4
75         DG3         0           76         DG2         0           77         DG1         0           78         DG0         0           78         DG0         0           79         TEST2         I           80         V <sub>D0</sub> -         -5 V power supply           81         V <sub>SS</sub> Ground           82         DR7         0           83         DR6         0           84         DR5         0           85         DR4         0           86         DR3         0           87         DR2         0           88         DR1         0           89         PR0         0           90         V <sub>SS</sub> Ground           91         ZOE         0         Memory write enable (1)           93         ZRAS         0         Rolwares strobe           94         ZCASL         0         Column address strobe (L)           95         ZWEH/ZCASH         0         Memory write enable (L)/column address strobe (H)           96         MD15         V/O         Frame memory interface data bus <tr< td=""><td></td><td></td><td></td><td>-</td></tr<>				-
76         DG2         0           77         DG1         0           78         DG3         0           79         TEST2         1           80         V <sub>D0</sub> +5 V power supply           81         V <sub>SS</sub> Ground           82         DR7         0           83         DR6         0           84         DR5         0           85         DR3         0           86         DR3         0           87         DR2         0           88         DR1         0           90         V <sub>SS</sub> Ground           91         ZOE         0           92         ZWEL         0           93         ZRAS         0           94         ZCASL         0           95         ZWEL/ZASH         0           96         V <sub>D0</sub> +5 V power supply**           97         V <sub>SS</sub> Ground           98         MD14         UO           96         ZWEL/ZASH         0           97         V <sub>SS</sub> Ground           98         MD15 <td< td=""><td></td><td></td><td></td><td>- Pixel data bus G (U)</td></td<>				- Pixel data bus G (U)
$77$ DG1         O           78         DG0         O           78         TEST2         I         Test pin           80 $V_{DD}$ +5 V power supply           81 $V_{SS}$ Ground           82         DR7         O           83         DR6         O           84         DR5         O           85         DR4         O           86         DR3         O           87         DR0         O           88         DR1         O           89         DR0         O           90         Vss         Ground           91         ZOE         O           92         ZWEL         O           93         ZRAS         O           94         ZCASL         O           95         ZWELZASH         O           96 $V_{DD}$ +5 V power supply**           97         Vss         Ground           98         MD14         I/O           99         MD14         I/O           99         MD14         I/O           100				-
$78$ DG0         O $79$ TEST2         I         Test pin $80$ $V_{DD}$ $45$ V power supply $81$ $V_{SS}$ Ground $82$ DR7         O $83$ DR6         O $84$ DR5         O $84$ DR3         O $86$ DR3         O $87$ DR2         O $89$ DR1         O $90$ Vss         Ground $91$ ZOE         O $92$ ZWEL         O         Memory output enable $92$ ZWEL         O         Memory output enable $92$ ZWEL         O         Memory write enable (L) $93$ ZRAS         O         Row address strobe $94$ ZOE         O         Column address strobe (L) $98$ MD15         I/O $98$ MD15         I/O $99$ MD14         I/O $100$ MD13         I				-
79         TEST2         I         Test pin           80         V <sub>DD</sub> 45 V power supply           81         V <sub>SS</sub> Ground           82         DR7         O           83         DR6         O           84         DR5         O           85         DR4         O           86         DR3         O           87         DR2         O           88         DR1         O           90         V <sub>SS</sub> Ground           91         ZOE         O           93         DR0         O           94         ZOKEL         O           93         ZRAS         O           94         ZOASL         O           95         ZWELQ         Memory write enable (L)           93         ZASL         O           94         ZOASL         O           95         ZWEL/CASH         O           96         V <sub>DO</sub> +5 V power supply*1           97         V <sub>SS</sub> Ground           98         MD15         I/O           101         MD10         I/O				4
80         V <sub>DD</sub> +5 <sup>1</sup> power supply           81         V <sub>SS</sub> Ground           82         DR7         O           83         DR6         O           84         DR5         O           85         DR4         O           86         DR3         O           87         DR2         O           88         DR1         O           89         DR0         O           90         V <sub>SS</sub> Ground           91         ZOE         O           93         ZRAS         O           94         ZCASL         O           95         ZWEL         O           96         V <sub>DD</sub> +5 <sup>1</sup> power supply <sup>*1</sup> 97         V <sub>SS</sub> Ground           98         MD15         I/O           99         MD14         I/O           99         MD14         I/O           91         ZOE         Ground           91         MD16         I/O           92         WD15         I/O           93         JRAS         Ground           94         So				Test nin
81         V <sub>SS</sub> Ground           82         DR7         0           83         DR6         0           84         DR5         0           85         DR4         0           86         DR3         0           87         DR2         0           88         DR1         0           90         V <sub>SS</sub> Ground           91         ZOE         0           92         ZWEL         0           93         ZRAS         0           94         ZCASL         0           95         ZWEL/CASH         0           96         V <sub>DD</sub> +5 V power supply**           97         V <sub>SS</sub> Ground           98         MD15         1/0           97         V <sub>SS</sub> Ground           98         MD15         1/0           99         MD14         1/0           100         MD10         1/0           101         MD10         1/0           102         MD11         1/0           103         MD10         1/0           104         MD9         1/			-	
82         DR         0           83         DR6         0           84         DR5         0           86         DR4         0           86         DR3         0           87         DR2         0           88         DR1         0           89         DR0         0           90         Vss         Ground           91         ZOE         0           92         ZWEL         0           93         ZRAS         0           94         ZCSL         0           95         ZWEL/CASH         0           96         V <sub>DD</sub> 45 V power supply <sup>e1</sup> 97         V <sub>SS</sub> Ground           98         MD15         1/0           96         V <sub>DD</sub> 45 V power supply <sup>e1</sup> 97         V <sub>SS</sub> Ground           98         MD14         1/0           99         MD14         1/0           101         MD12         1/0           102         MD11         1/0           103         MD10         1/0           104         V <sub>DD</sub>				
83DR6O84DR5O86DR4O86DR3O87DR2O88DR1O89DR0O90VssC91ZOEO92ZWELO93ZRASO94ZCASLO95ZWEL/CSHO96Monoy write enable (L)97VssO98MD15IO99MD14IO99MD14IO101MD12IO103MD10IO104Vpb+5V power supply105VssGround106MD9IO107MD8IO108MD7IO109MD5IO101MD7IO103MD7IO104MD9IO105VssGround106MD9IO107MD8IO108MD7IO109MD5IO100MD73IO101MD7IO102MD14IO103MD7IO104MD9IO105VssGround106MD9IO107MD8IO108MD7IO109MD5IO100MD5IO101MD5 <t< td=""><td></td><td></td><td></td><td></td></t<>				
84DR5085DR4086DR3087DR2088DR1089DR0090 $V_{SS}$ Ground91ZOE092ZWEL093ZRAS094ZCASL095ZWEH/ZCASH096 $V_{DD}$ +5 V power supply*'97 $V_{SS}$ Ground98MD151/099MD141/0910MD131/0911I/00912ZWEH/ZCASHGround913ZOSL0914Column address strobe (L)915SWEH/ZCASHFrame memory interface data bus916VDD+5 V power supply*'917VSSGround918MD151/01010MD131/01011MD101/01011MD101015VSSGround1016MD91/01017MD81/01018MD71/01019MD61/01010MD71/01011MD51/01011MD51/0				-
85DR4086DR3087DR2088DR1090NSGround90VSSGround91ZOE092ZWEL093ZRAS094ZOSL095ZWEH/ZCASH096VDD+5 V power supply*'97VSSGround98MD151/099MD141/099MD141/0101MD101/0102MD101/0103MD101/0104VDD+5 V power supply105VSSGround106MD91/0107MD81/0108MD71/0109MD61/01010MD71/01011MD51/0				-
86DR3O87DR2O88DR1O89DR0O90 $V_{SS}$ Ground91ZOEO92ZWELO93ZRASO94ZCASLO95ZWEL/ZASHO96 $V_{DD}$ +5 V power supply**97 $V_{SS}$ Ground98MD15I/O99MD14I/O100MD13I/O101MD12I/O103MD10I/O104 $V_{DD}$ +5 V power supply105 $V_{SS}$ Ground106MD9I/O107MD8I/O108MD7I/O109MD6I/O101MD5I/O101MD5I/O				Pixel data bus R (Y)
87         DR2         O           88         DR1         O           89         DR0         O           90         Vss         Ground           91         ZOE         O           92         ZWEL         O           93         ZRAS         Row address strobe           94         ZCASL         O           95         ZWEL/2CASH         O           96         VbD         +5 V power supply**           97         Vss         Ground           98         MD15         VO           99         MD14         VO           99         MD13         VO           101         MD12         VO           102         MD11         VO           103         MD10         VO           104         VbD         +5 V power supply           105         Vss         Ground           106         MD10         VO           107         MD8         VO           108         MD10         VO           109         MD6         VO           1010         MD8         VO           1010 <t< td=""><td></td><td></td><td></td></t<>				
88         DR1         0           89         DR0         0           90         V <sub>SS</sub> Ground           91         ZOE         0         Memory output enable           92         ZWEL         0         Memory write enable (L)           93         ZRAS         0         Row address strobe           94         ZCASL         0         Column address strobe (L)           95         ZWEH/ZCASH         0         Memory write enable (H)/column address strobe (H)           96         V <sub>DD</sub> +5 V power supply**         Farme memory interface data bus           97         V <sub>SS</sub> Ground         Farme memory interface data bus           98         MD15         I/O         Farme memory interface data bus           101         MD12         I/O         Farme memory interface data bus           101         MD10         I/O         Farme memory interface data bus           104         V <sub>DD</sub> +5 V power supply         Farme memory interface data bus           105         V <sub>SS</sub> Ground         Farme memory interface data bus           106         MD9         I/O         Farme memory interface data bus           107         MD8         I/O				-
89         DR0         O           90         V <sub>SS</sub> Ground           91         ZOE         O         Memory output enable           92         ZWEL         O         Memory write enable (L)           93         ZRAS         O         Row address strobe           94         ZCASL         O         Column address strobe (L)           95         ZWEH/ZASH         O         Memory write enable (H)/column address strobe (H)           96         V <sub>DD</sub> +5 V power supply*1         Ground           97         V <sub>SS</sub> Ground         Ground           98         MD15         I/O         Frame memory interface data bus           101         MD12         I/O         Frame memory interface data bus           101         MD11         I/O         Frame memory interface data bus           101         MD10         I/O         Frame memory interface data bus           104         V <sub>DD</sub> +5 V power supply         Frame memory interface data bus           105         V <sub>SS</sub> Ground         Ground           106         MD9         I/O         Frame memory interface data bus           106         MD9         I/O         Frame memory int				-
90         V <sub>SS</sub> Ground           91         ZOE         0         Memory output enable           92         ZWEL         0         Memory write enable (L)           93         ZRAS         0         Row address strobe           94         ZCASL         0         Column address strobe (L)           95         ZWEH/ZCASH         0         Memory write enable (H)/column address strobe (H)           96         V <sub>DD</sub> +5 V power supply*'           97         V <sub>SS</sub> Ground           98         MD15         //O           99         MD14         //O           100         MD13         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           109         MD6         I/O				
91         ZOE         O         Memory output enable           92         ZWEL         O         Memory write enable (L)           93         ZRAS         O         Row address strobe           94         ZCASL         O         Column address strobe (L)           95         ZWEH/ZCASH         O         Memory write enable (H)/column address strobe (H)           96         V <sub>DD</sub> +5 V power supply*1           97         V <sub>SS</sub> Ground           98         MD15         I/O           99         MD14         I/O           100         MD12         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           109         MD6         I/O			0	Cround
92         ZWEL         O         Memory write enable (L)           93         ZRAS         O         Row address strobe           94         ZCASL         O         Column address strobe (L)           95         ZWEH/ZCASH         O         Memory write enable (H)/column address strobe (H)           96         V <sub>DD</sub> +5 V power supply*1           97         V <sub>SS</sub> Ground           98         MD15         I/O           99         MD14         I/O           100         MD12         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           109         MD6         I/O				
93         ZRAS         O         Row address strobe           94         ZCASL         O         Column address strobe (L)           95         ZWEH/ZCASH         O         Memory write enable (H)/column address strobe (H)           96         V <sub>DD</sub> +5 V power supply*1           97         V <sub>SS</sub> Ground           98         MD15         I/O           99         MD14         I/O           100         MD13         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				
94         ZCASL         0         Column address strobe (L)           95         ZWEH/ZCASH         0         Memory write enable (H)/column address strobe (H)           96         V <sub>DD</sub> +5 V power supply*1           97         V <sub>SS</sub> Ground           98         MD15         I/O           99         MD14         I/O           100         MD13         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         V           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				
95         ZWEH/ZCASH         O         Memory write enable (H)/column address strobe (H)           96         V <sub>DD</sub> +5 V power supply*1           97         V <sub>SS</sub> Ground           98         MD15         I/O           99         MD14         I/O           100         MD13         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				
96         V <sub>DD</sub> +5 V power supply*'           97         V <sub>SS</sub> Ground           98         MD15         I/O           99         MD14         I/O           100         MD13         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				
97         V <sub>SS</sub> Ground           98         MD15         I/O           99         MD14         I/O           100         MD13         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				
98         MD15         V/O           99         MD14         I/O           100         MD13         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				
99         MD14         I/O           100         MD13         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O			1/0	
100         MD13         I/O           101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				4
101         MD12         I/O           102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				
102         MD11         I/O           103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				rame memory interface data bus
103         MD10         I/O           104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				•
104         V <sub>DD</sub> +5 V power supply           105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				4
105         V <sub>SS</sub> Ground           106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O			1/0	
106         MD9         I/O           107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				
107         MD8         I/O           108         MD7         I/O           109         MD6         I/O           110         MD5         I/O				Grouna
108MD7I/O109MD6I/O110MD5I/O				-
109         MD6         I/O           110         MD5         I/O				4
110 MD5 I/O				Frame memory interface data bus
				4
	111	MD4	I/O	

Continued from preceding page.

Pin No.	Symbol	I/O	Function
112	V <sub>SS</sub>		Ground
113	V <sub>DD</sub>		+5 V power supply
114	MD3	I/O	
115	MD2	I/O	Frame memory interface data bus
116	MD1	I/O	
117	MD0	I/O	
118	V <sub>SS</sub>		Ground
119	MA8	0	Frame memory address signals
120	MA7	0	
121	MA6	0	
122	MA5	0	
123	MA4	0	
124	MA3	0	
125	MA2	0	
126	MA1	0	
127	MA0	0	
128	V <sub>SS</sub>		Ground

## System Configuration Example

1. Separate code bus type

This is a system in which the code and system busses are separated. The coded data input does not load down the system bus.



#### 2. Shared code bus type

This is a system in which code bus and the system bus are connected. Coded data is written by the CPU, or alternatively, data can be written using the DMA controller.



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