

SANYO

No.3049B

## PAL CCD 1H Delay Line

**Overview**

The LC 8992 is a 1H delay line for PAL television systems. It incorporates a 565.5 stage CCD shift register, timing generator, clock driver, sync clamp and auto-bias circuits, and a sample-and-hold amplifier. Only an external low-pass filter is required to implement a 1H delay line. The LC8992 operates with a single 9V power supply and is available in 8-pin plastic DIPs.

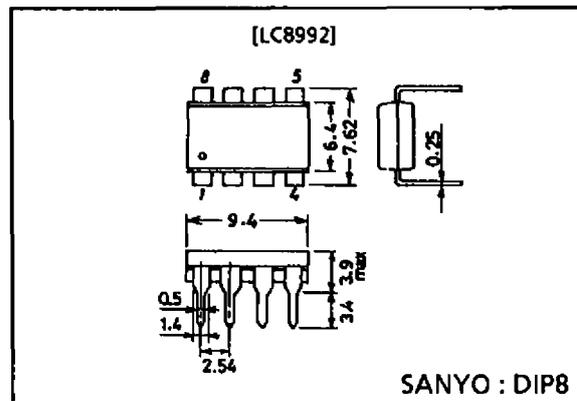
**Features**

- 1H delay with low-pass filter and 8.86MHz clock.
- Minimum of external components.
- Low clock input voltage.
- Single 9V power supply.
- 8-pin DIP

**Package Dimensions**

unit : mm

3001B-DIP8

**Specifications**Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$ 

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD}$ max		11	V
Allowable power dissipation	$P_{dmax}$		500	mW
Operating temperature	$T_{opr}$		-10 to +60	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

**Electrical Characteristics**DC Characteristics at  $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 9\text{V}$ , clock = 8.8672375MHz : 0.3Vp-p

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}$		8.5	9.0	9.5	V
Supply current	$I_{DD}$			20.0	25.0	mA
DC output voltage	$V_{GG}$			13.5		V
	OUT			3.1		V
	VOB			4.5		V
	$V_{IPIN}$			2.8		V
	CLK			2.0		V
	COMP				2.7	

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SANYO Electric Co., Ltd. Semiconductor Business Headquarters

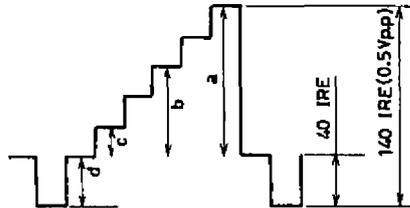
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# LC8992

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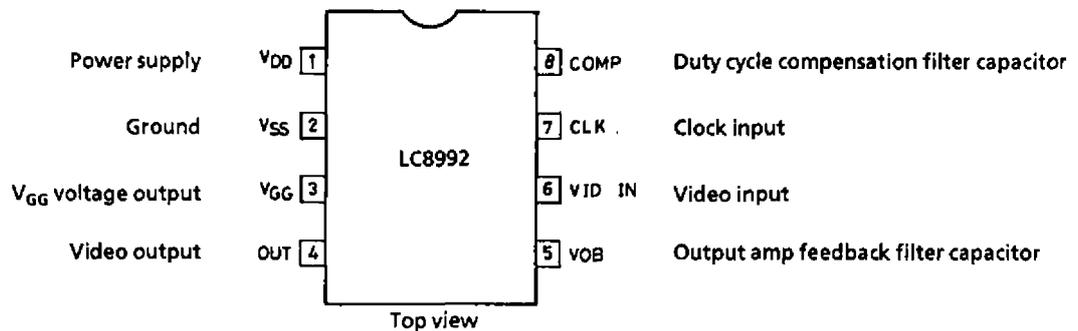
## AC Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} = 9\text{V}$ , clock = 8.8672375MHz : 0.3Vp-p

Parameter	Symbol	Conditions	min	typ	max	Unit
Video input voltage	$V_{IN\ max}$			0.5	0.7	Vp-p
Voltage gain	$G_V$	Input : 15kHz, 0.5Vp-p	6	9	11	dB
Linearity	L6	b/a, See note	56	60	64	%
	L2	c/a, See note	18	20	22	%
	L5	d/a, See note	37	40	43	%
Frequency respons	$G_f$	0.5Vp-p sine wave input, response at 2.4MHz relative to 20kHz	-3.0	-2.0		dB
Noise voltage	$V_{NO}$	3.8MHz bandwidth		1.1		mVrms
Clock input voltage	$E_{CK}$		0.1	0.3	1.0	Vp-p
Output impedance	$Z_O$			520		$\Omega$
Delay time	$t_o$			63.90		$\mu\text{s}$

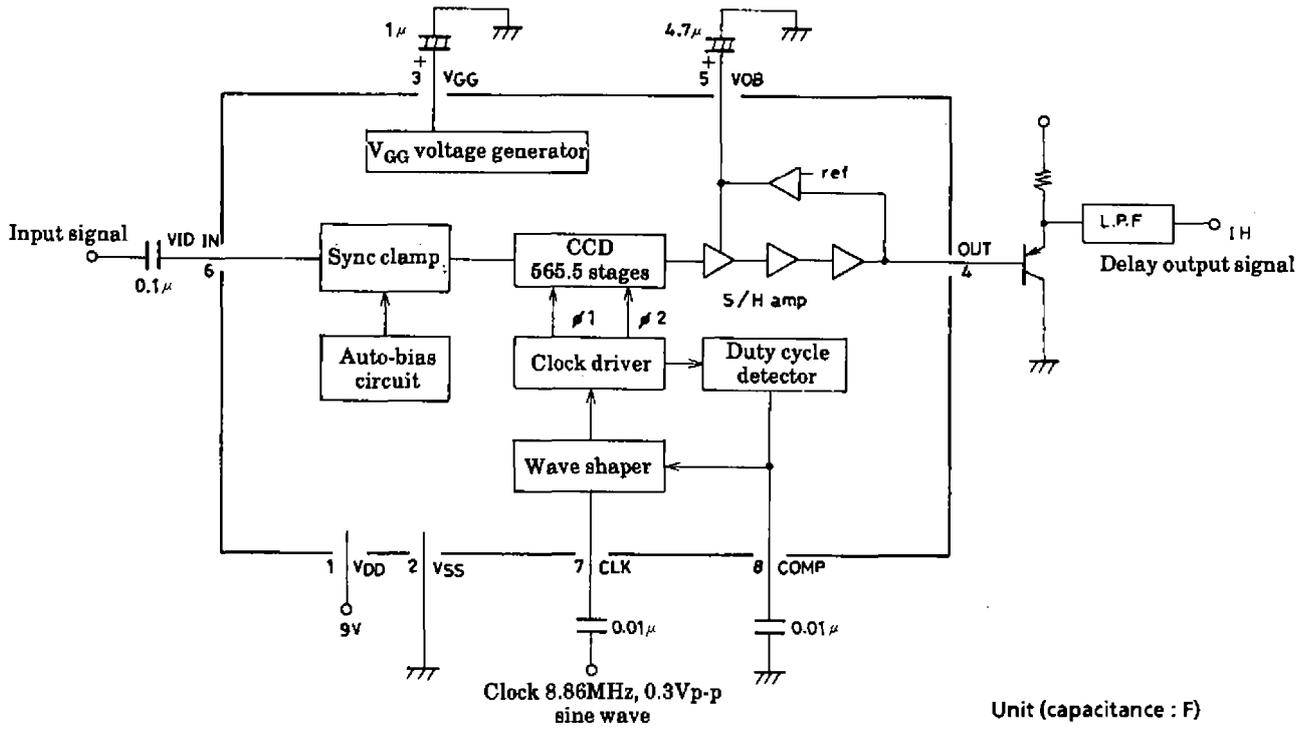


Note) : Linearity test waveform (2.4MHz) / (20kHz)

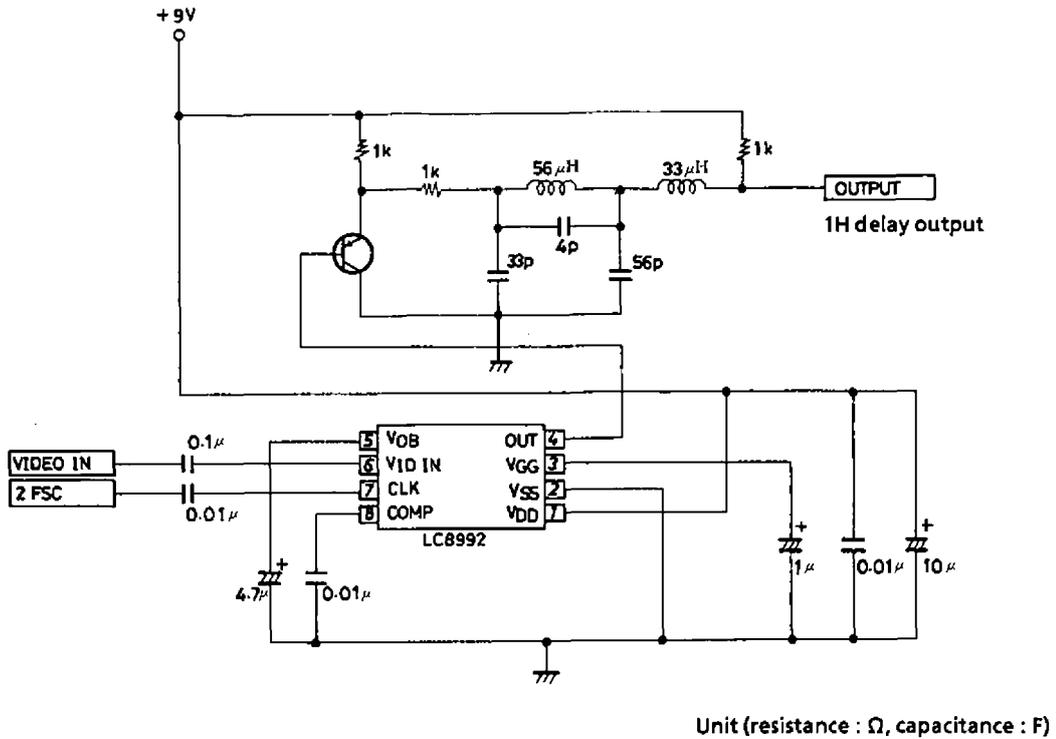
## Pin Assignment



Block Diagram



Sample Application Circuit



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