



Quad SPST JFET Analog Switches

LF11331, LF13331 4 Normally Open Switches with Disable

LF11332, LF13332 4 Normally Closed Switches with Disable

LF11333, LF13333 2 Normally Closed Switches and 2 Normally Open Switches with Disable

LF11201, LF13201 4 Normally Closed Switches

LF11202, LF13202 4 Normally Open Switches

General Description

These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of $\pm 10V$. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

These devices operate from $\pm 15V$ supplies and swing a $\pm 10V$ analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

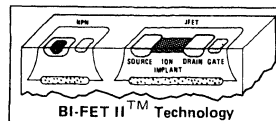
Features

- Analog signals are not loaded
- Constant "ON" resistance for signals up to $\pm 10V$ and 100 kHz
- Pin compatible with CMOS switches with the advantage of blow out free handling
- Small signal analog signals to 50 MHz
- Break-before-make action
- High open switch isolation at 1.0 MHz
- Low leakage in "OFF" state
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package on LF11331, LF11332, LF11333
- LF11201 is pin compatible with DG201

$$t_{OFF} < t_{ON}$$

$$-50 \text{ dB}$$

$$< 1.0 \text{ nA}$$



Test Circuit and Schematic Diagram

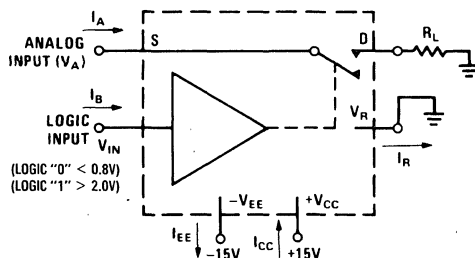


FIGURE 1. Typical Circuit for One Switch

TL/H/5667-2

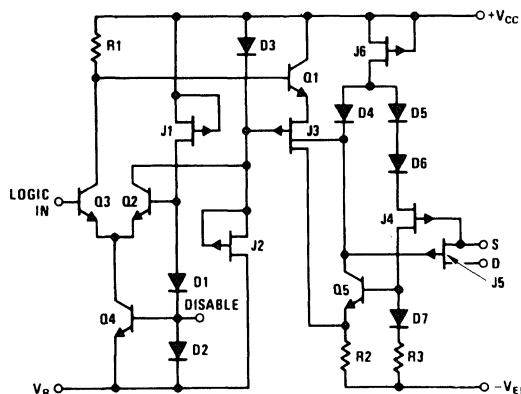
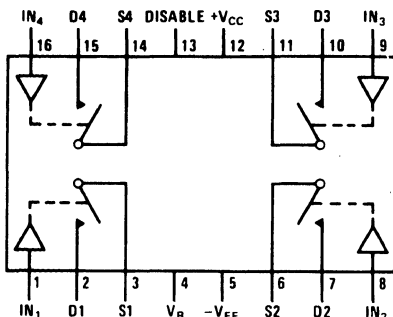


FIGURE 2. Schematic Diagram (Normally Open)

TL/H/5667-12

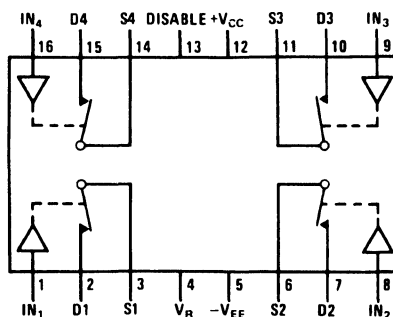
Connection Diagrams (Top View for SO and Dual-In-Line Packages) (All Switches Shown are For Logical "0")

LF11331/LF13331



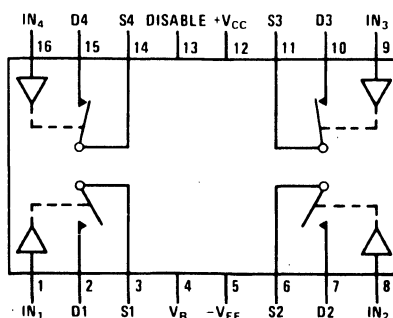
TL/H/5667-1

LF11332/LF13332



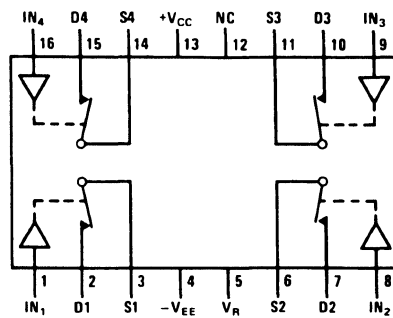
TL/H/5667-13

LF11333/LF13333



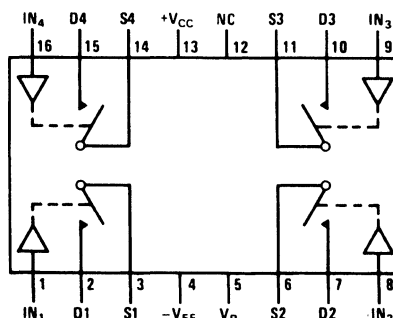
TL/H/5667-14

LF11201/LF13201



TL/H/5667-15

LF11202/LF13202



TL/H/5667-16

Order Number LF13201D, LF11201D, LF13202D, LF11202D, LF13331D, LF11331D, LF13332D, LF11332D, LF13333D or LF11333D

See NS Package Number D16C

Order Number LF13201M, LF13202M, LF13331M, LF13332M or LF13333M

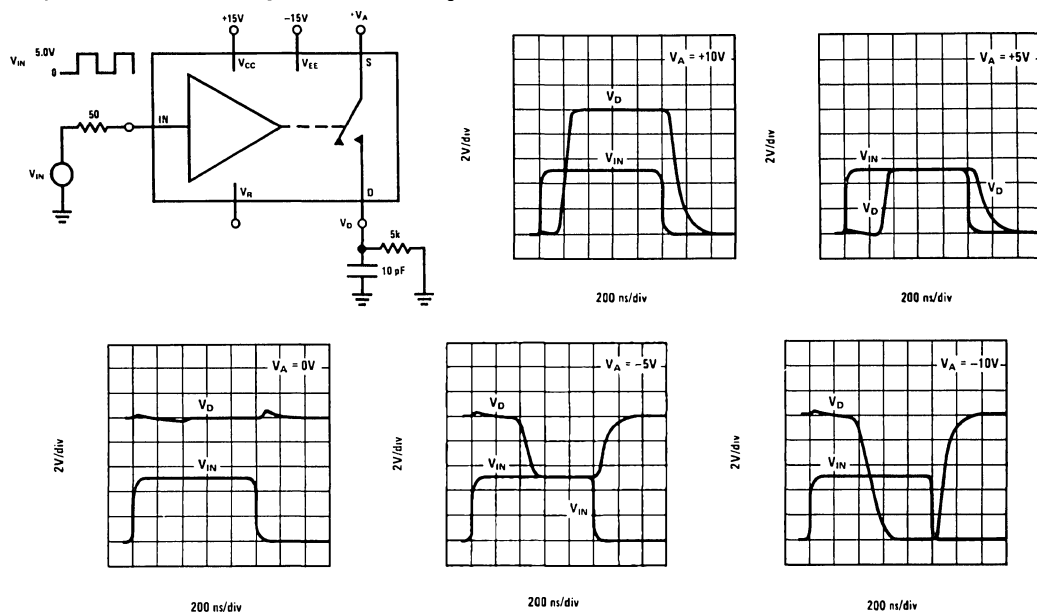
See NS Package Number M16A

Order Number LF13201N, LF13202N, LF13331N, LF13332N or LF13333N

See NS Package Number N16A

Test Circuit and Typical Performance Curves

Delay Time, Rise Time, Settling Time, and Switching Transients



TL/H/5667-3

Additional Test Circuits

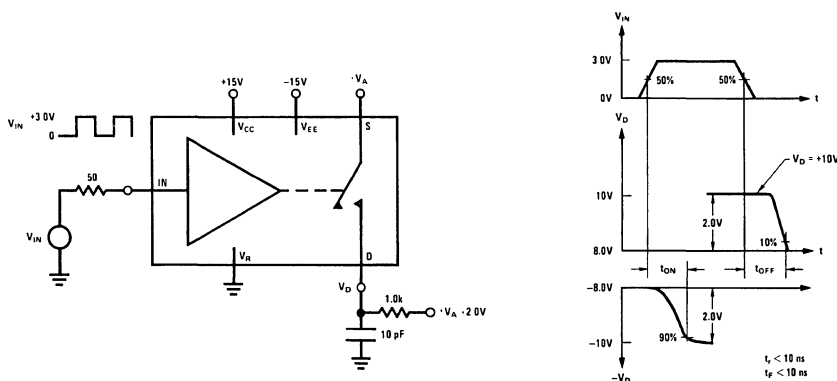


FIGURE 3. t_{ON} , t_{OFF} Test Circuit and Waveforms for a Normally Open Switch

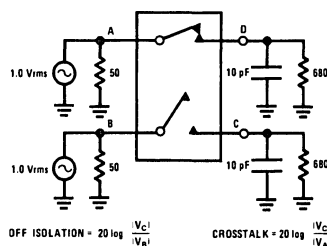


FIGURE 4. "OFF" Isolation, Crosstalk, Small Signal Response

TL/H/5667-4

"ON" Resistance

Y-axis: $R_{ON} (\Omega)$

X-axis: $V_A (\text{VOLTS})$

Conditions:
 $V_{GS} = 0V$
 $V_{DS} = 15V$
 $I_{AS} = 0.1mA$

V_A (VOLTS)	R_{ON} (Ω)
-10	150
-5	148
0	145
5	140
10	135

"ON" Resistance

Y-axis: $R_{ON} (\Omega)$ (0 to 200)
 X-axis: TEMPERATURE ($^{\circ}C$) (-50 to 150)

Test Conditions:
 $V_{CC} = 15V$
 $V_{EE} = -15V$
 $I_A = 0.1 mA$
 $V_A = 0$

"ON" Resistance

Resistance (Ω)

240
200
160
120
80
40
0

6.0 4.0 2.0 0.0 0.0 2.0 4.0 6.0

ANALOG CURRENT (mA)

$V_{CC} = 15V$
 $V_{EE} = -15V$
 $V_A = 0$

Break-Before-Make Action

TIME (ns)

$V_{CC} = 15V, -V_{EE} = -15V$
 TIME MEASURED FROM
 50% INPUT PULSE TO 90%
 OF OUTPUT PULSE

t_{ON}

t_{OFF}

V_A (VOLTS)

Switching Times

$V_{CC} = 15V$
 $V_{EE} = -15V$

$t_{ONI}, V_A = -10V$
 $t_{OFFI}, V_A = +10V$
 $t_{ONFI}, V_A = +10V$
 $t_{OFFFI}, V_A = -10V$

TIME (ns)

TEMPERATURE (°C)

Crosstalk and "OFF" Isolation vs Frequency Using Test Circuit of Figure 5

Frequency (Hz)	OFF ISOLATION (dB)	CROSSTALK (dB)
100k	-75	-85
1M	-55	-65
1	-30	-45

Supply Current

$V_A = V_{EE} = 5.0V$
ALL SWITCHES OFF

Y-axis: SUPPLY CURRENT (mA)
X-axis: SUPPLY VOLTAGE (V)

Curves shown:
POSITIVE (I_{CC})
NEGATIVE (I_{EE})
REFERENCE (I_N)

Supply Current

$V_{CC} = 15V$
 $V_{EE} = 15V$
 ALL SWITCHES OFF

Supply Current (mA)

TEMPERATURE (°C)

POSITIVE (I_{CC})

NEGATIVE (I_{EE})

REFERENCE (I_A)

Supply Current

5.0
4.0
3.0
2.0
1.0
0

POSITIVE (I_{CC})

NEGATIVE (I_{EE})

0 10 100 10k 100k 1.0

FREQUENCY (Hz)

$V_{CC} = 15V$
 $V_{EE} = -15V$
 $V_A = -10V$
 $I_A = 0$

Switch Leakage Currents

$V_{CC} = 15V, V_{EE} = -15V$
OFF LEAKAGE CONDITIONS
 $V_S = +10V, V_D = -10V$
ON LEAKAGE CONDITIONS
 $V_S = V_D = -10V$

Y-axis: CURRENT (μA)
 X-axis: TEMPERATURE ($^{\circ}C$)

Curves shown:
 I_{SIOFF}
 I_{SION}
 $I_{SION} + I_{SIOFF}$

Switch Leakage Current

$V_{GS} = 15V$
 $V_{DS} = -15V$
**POSITIVE CURRENT
 DEFINED INTO NODE**

Leakage Current (nA)

$I_{DS(ON)}$
 $I_{DS(OFF)}$

V_A (VOLTS)

Slew Rate of Analog Voltage Above Which Signal Loading Occurs

Y-axis: SLEW RATE (V/μs)
X-axis: TEMPERATURE (°C)

Supply Voltages: $V_{CC} = 15V$, $V_{EE} = 15V$

Temperature (°C)	Slew Rate (V/μs)
-100	58
0	58
125	38

Small Signal Response

$C_L = 3 \text{ pF}$
ATTENUATION = 20 LOG
 (SEE FIGURE 4)

$\frac{N_D}{N_A}$

ATTENUATION (dB)

FREQUENCY (Hz)

Maximum Accurate Analog Current vs Temperature

(NOTE 6)

Temperature (°C)	Analog Current (mA)
-50	-18
0	-12
50	-8
100	-6
150	-5

Logical "1" Input Bias Current

Y-axis: INPUT CURRENT (I_A)

X-axis: TEMPERATURE (°C)

Bias Conditions:
 $V_{CC} = 15V$
 $V_{EE} = 15V$
 $V_{IN} = +5.0V$
 $V_R = 0V$

Temperature (°C)	Input Current (I_A)
-50	9.0
-25	7.5
0	5.0
25	4.0
50	3.5
75	3.2
100	3.0

Application Hints

GENERAL INFORMATION

These devices are monolithic quad JFET analog switches with "ON" resistances which are essentially independent of analog voltage or analog current. The leakage currents are typically less than 1 nA at 25°C in both the "OFF" and "ON" switch states and introduce negligible errors in most applications. Each switch is controlled by minimum TTL logic levels at its input and is designed to turn "OFF" faster than it will turn "ON." This prevents two analog sources from being transiently connected together during switching. The switches were designed for applications which require break-before-make action, no analog current loss, medium speed switching times and moderate analog currents.

Because these analog switches are JFET rather than CMOS, they do not require special handling.

LOGIC INPUTS

The logic input (V_{IN}), of each switch, is referenced to two forward diode drops (1.4V at 25°C) from the reference supply (V_R) which makes it compatible with DTL, RTL, and TTL logic families. For normal operation, the logic "0" voltage can range from 0.8V to -4.0V with respect to V_R and the logic "1" voltage can range from 2.0V to 6.0V with respect to V_R , provided V_{IN} is not greater than $(V_{CC} - 2.5V)$. If the input voltage is greater than $(V_{CC} - 2.5V)$, the input current will increase. If the input voltage exceeds 6.0V or -4.0V with respect to V_R , a resistor in series with the input should be used to limit the input current to less than 100 μ A.

ANALOG VOLTAGE AND CURRENT

Analog Voltage

Each switch has a constant "ON" resistance (R_{ON}) for analog voltages from $(V_{EE} + 5V)$ to $(V_{CC} - 5V)$. For analog voltages greater than $(V_{CC} - 5V)$, the switch will remain ON independent of the logic input voltage. For analog voltages less than $(V_{EE} + 5V)$, the ON resistance of the switch will increase. Although the switch will not operate normally when the analog voltage is out of the previously mentioned range, the source voltage can go to either $(V_{EE} + 36V)$ or $(V_{CC} + 6V)$, whichever is more positive, and can go as negative as V_{EE} without destruction. The drain (D) voltage can also go to either $(V_{EE} + 36V)$ or $(V_{CC} + 6V)$, whichever is more positive, and can go as negative as $(V_{CC} - 36V)$ without destruction.

Analog Current

With the source (S) positive with respect to the drain (D), the R_{ON} is constant for low analog currents, but will increase at higher currents (>5 mA) when the FET enters the saturation region. However, if the drain is positive with respect to the source and a small analog current loss at high analog currents (Note 6) is tolerable, a low R_{ON} can be maintained for analog currents greater than 5 mA at 25°C.

LEAKAGE CURRENTS

The drain and source leakage currents, in both the ON and the OFF states of each switch, are typically less than 1 nA at 25°C and less than 100 nA at 125°C. As shown in the typical curves, these leakage currents are Dependent on power supply voltages, analog voltage, analog current and the source to drain voltage.

DELAY TIMES

The delay time OFF (t_{OFF}) is essentially independent of both the analog voltage and temperature. The delay time ON (t_{ON}) will decrease as either $(V_{CC}-V_A)$ decreases or the temperature decreases.

POWER SUPPLIES

The voltage between the positive supply (V_{CC}) and either the negative supply (V_{EE}) or the reference supply (V_R) can be as much as 36V. To accommodate variations in input logic reference voltages, V_R can range from V_{EE} to $(V_{CC} - 4.5V)$. Care should be taken to ensure that the power supply leads for the device never become reversed in polarity or that the device is never inadvertently installed backwards in a test socket. If one of these conditions occurs, the supplies would zener an internal diode to an unlimited current; and result in a destroyed device.

SWITCHING TRANSIENTS

When a switch is turned OFF or ON, transients will appear at the load due to the internal transient voltage at the gate of the switch JFET being coupled to the drain and source by the junction capacitances of the JFET. The magnitude of these transients is dependent on the load. A lower value R_L produces a lower transient voltage. A negative transient occurs during the delay time ON, while a positive transient occurs during the delay time OFF. These transients are relatively small when compared to faster switch families.

DISABLE NODE

This node can be used, as shown in *Figure 5*, to turn all the switches in the unit off independent of logic inputs. Normally, the node floats freely at an internal diode drop ($\approx 0.7V$) above V_R . When the external transistor in *Figure 5* is saturated, the node is pulled very close to V_R and the unit is disabled. Typically, the current from the node will be less than 1 mA. This feature is not available on the LF11201 or LF11202 series.

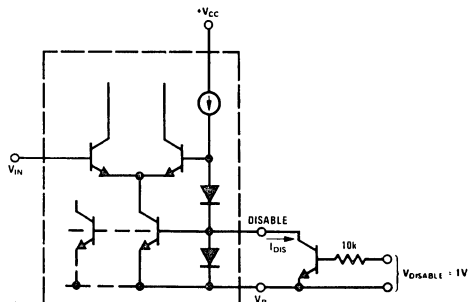
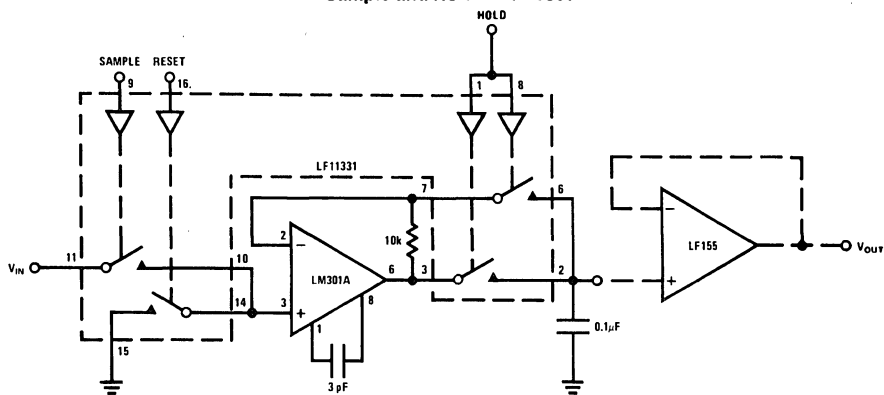


FIGURE 5. Disable Function

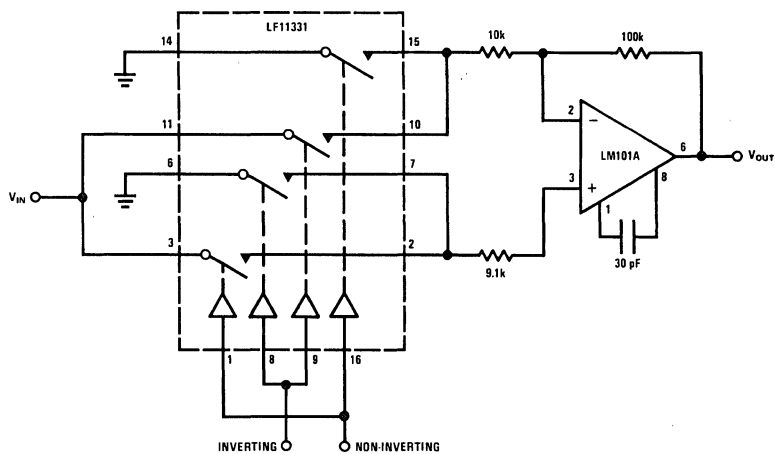
TI/H/5667-6

Typical Applications

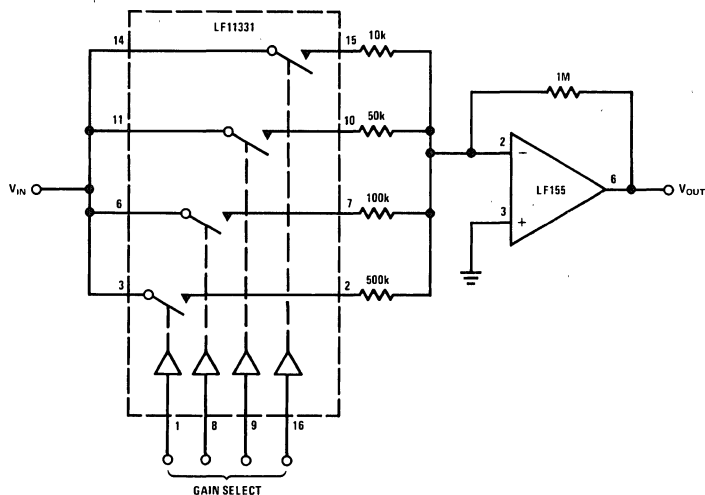
Sample and Hold with Reset

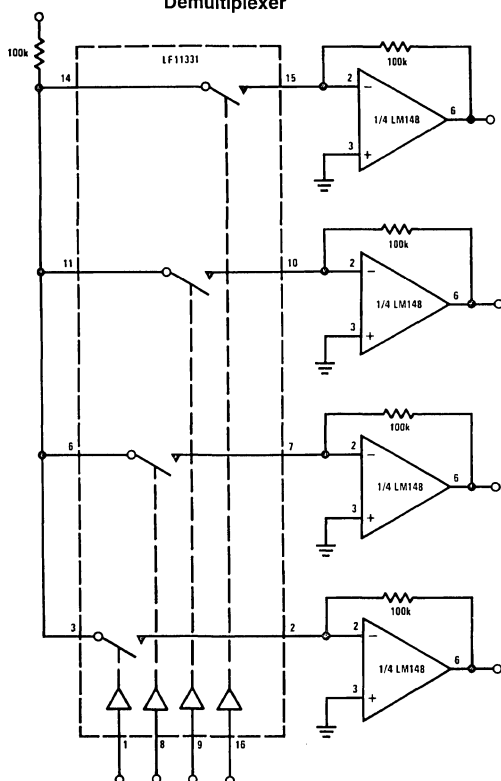


Programmable Inverting Non-Inverting Operational Amplifier

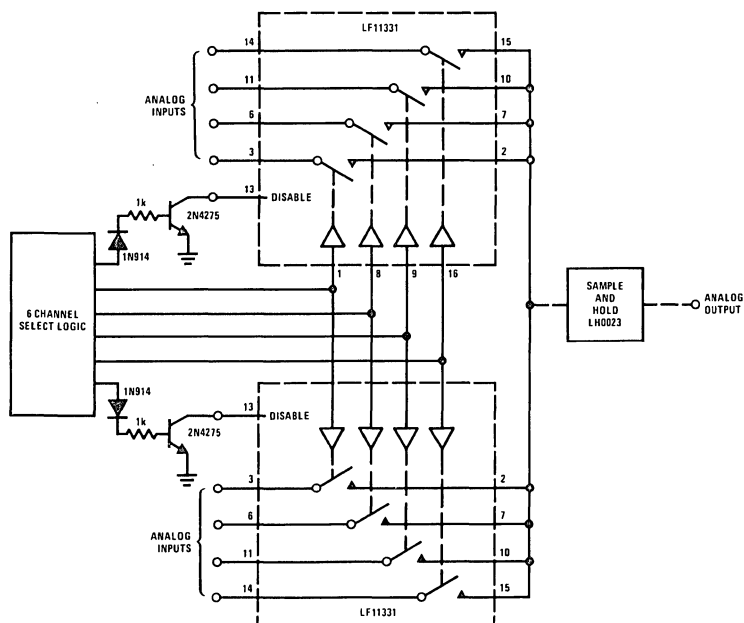
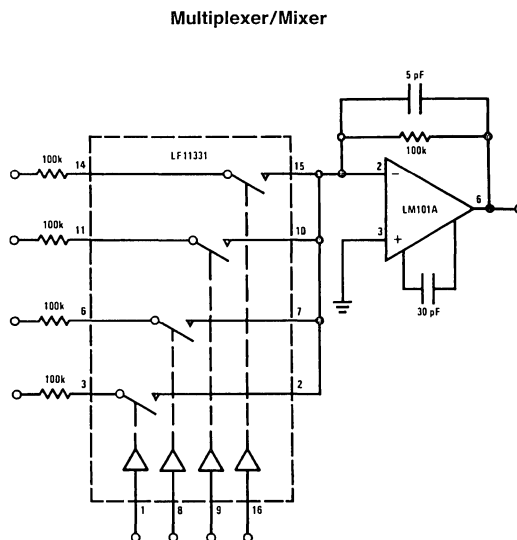


Programmable Gain Operational Amplifier



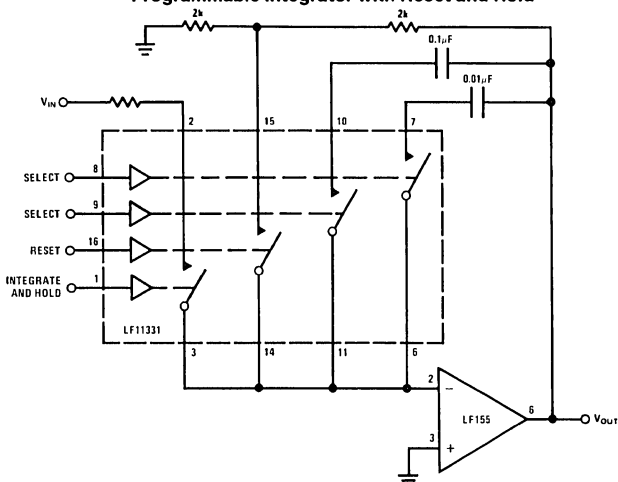


8-Channel Analog Commutator with 6-Channel Select Logic

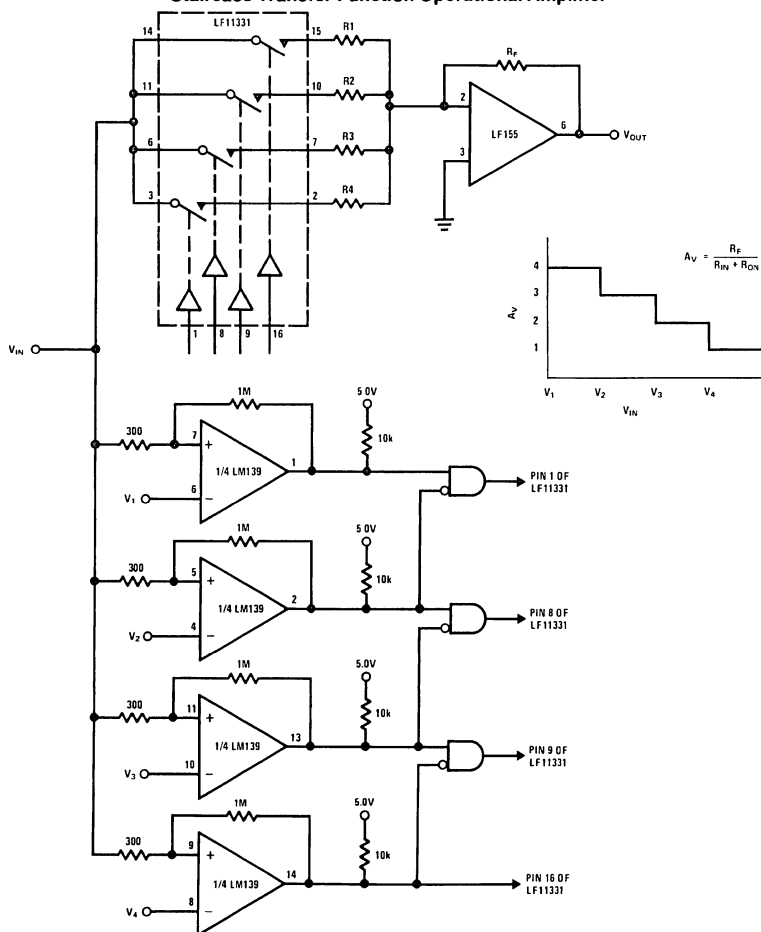


Typical Applications (Continued)

Programmable Integrator with Reset and Hold



Staircase Transfer Function Operational Amplifier



The diagram illustrates a PLL-based frequency synthesizer, divided into two main sections: the **MODULATOR** and the **DEMODULATOR**.

MODULATOR Section:

- Input:** An input frequency V_{in} is applied to the non-inverting input (+) of the first LM101A comparator.
- Reference:** A 1k resistor connects the inverting input (-) of the first LM101A to the inverting input (-) of the second LM101A. The second LM101A's non-inverting input (+) is connected to ground through a 500 resistor.
- Feedback:** The output (pin 6) of the first LM101A is connected to its inverting input (+) through a 30 pF capacitor. The output (pin 6) of the second LM101A is connected to its inverting input (+) through a 30 pF capacitor.
- Timing:** Both comparators have a 100 resistor and a 0.02 μ F capacitor connected to their output pins (pin 3 for the first, pin 6 for the second) to ground.
- Output:** The outputs of the comparators are connected to the inputs of the first LF11331 PLL (pins 3 and 2).

DEMODULATOR Section:

- Inputs:** The modulated signal from the Modulator section is connected to the inputs of the first LF11331 PLL (pins 3 and 2).
- Reference:** A 1k resistor connects the inverting input (-) of the first LF11331 to the inverting input (-) of the second LF11331. The second LF11331's non-inverting input (+) is connected to ground through a 500 resistor.
- Feedback:** The output (pin 6) of the first LF11331 is connected to its inverting input (+) through a 30 pF capacitor. The output (pin 6) of the second LF11331 is connected to its inverting input (+) through a 30 pF capacitor.
- Timing:** Both PLLs have a 100 resistor and a 0.02 μ F capacitor connected to their output pins (pin 3 for the first, pin 6 for the second) to ground.
- Output:** The outputs of the PLLs are connected to the inputs of the second LF11331 PLL (pins 3 and 2).

Waveforms:

- The top left waveform shows the input frequency V_{in} .
- The top middle waveform shows the modulated signal output from the Modulator section.
- The top right waveform shows the locked PLL outputs from the Demodulator section.

2-42