Signetics

LF198/LF298/LF398
Sample-and-Hold Amplifiers

Product Specification

Linear Products

DESCRIPTION

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize high-voltage ion-implant JFET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS; differential threshold is 1.4V. The LF198/LF298/LF398 will operate from ±5V to ±18V supplies. They are available in an 8-lead TO-5 package, or an 8-pin plastic DIP.

FEATURES

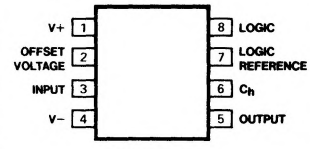
- **Operates from ±5V to ±18V supplies**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at C_H = 0.01μF**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

APPLICATION

- **The LF198/LF298/LF398 are ideally suited for a wide variety of sample-and-hold applications, including data acquisition, analog-to-digital conversion, synchronous demodulation, and automatic test setup**

PIN CONFIGURATIONS

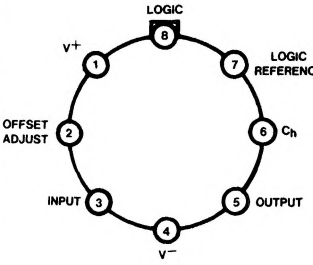
FE, N Packages



TOP VIEW

CD10920S

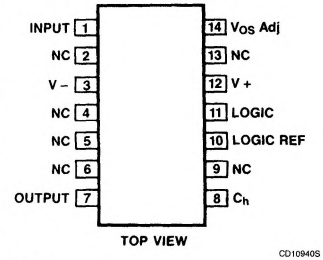
H Package



TOP VIEW

CD10931S

D Package[1]



TOP VIEW

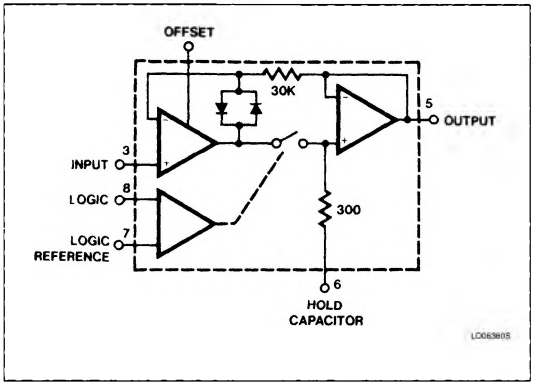
CD10940S

NOTE:
1. SO and non-standard pinouts.

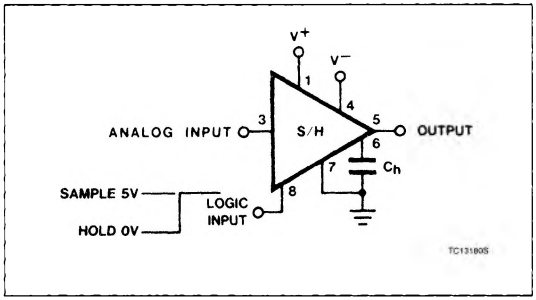
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
8-Pin Cerdip	−55°C to +125°C	LF198FE
8-Pin Metal Can	−55°C to +125°C	LF198H
14-Pin Plastic SO Package	0 to +70°C	LF398D
8-Pin Cerdip	0 to +70°C	LF398FE
8-Pin Metal Can	0 to +70°C	LF398H
8-Pin Plastic DIP	0 to +70°C	LF398N
8-Pin Cerdip	−25°C to +85°C	LF298FE
8-Pin Metal Can	−25°C to +85°C	LF298H

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±18	V
	Maximum power dissipation T_A = 25°C (still-air)[3] F package N package D package	 780 1160 1040	 mW mW mW
T_A	Operating ambient temperature range LF198 LF298 LF398	 −55 to +125 −25 to +85 0 to +70	 °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic-to-logic reference differential voltage[2]	+7, −30	V
	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	10	sec
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the packages must be derated based on the thermal resistance specified.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS Unless otherwise specified, the following conditions apply: unit is in "sample" mode; $V_S = \pm 15V$; $T_J = 25°C$; $-11.5V \leq V_{IN} \leq +11.5V$; $C_H = 0.01\mu F$; and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

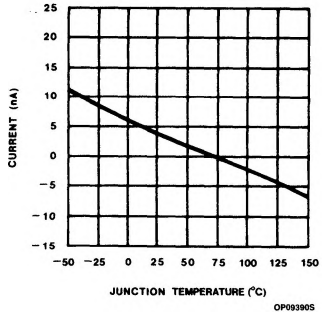
SYMBOL	PARAMETER	TEST CONDITIONS	LF198/LF298			LF398			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	$T_J = 25°C$		1	3 5		2	7 10	mV mV
I_{BIAS}	Input bias current[4]	$T_J = 25°C$ Full temperature range		5	25 75		10	50 100	nA nA
	Input impedance	$T_J = 25°C$		10^{10}			10^{10}		Ω
	Gain error	$T_J = 25°C$, $R_L = 10k$ Full temperature range		0.002	0.005 0.02		0.004	0.01 0.02	% %
	Feedthrough attenuation ratio at 1kHz	$T_J = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
	Output impedance	$T_J = 25°C$, "HOLD" mode Full temperature range		0.5	2 4		0.5	4 6	Ω Ω
	"HOLD" step[2]	$T_J = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	$T_J \leq 25°C$		4.5	5.5		4.5	6.5	mA
	Logic and logic reference input current	$T_J = 25°C$		2	10		2	10	μA
	Leakage current into hold capacitor[4]	$T_J = 25°C$[3], "HOLD" mode		30	100		30	200	pA
t_{AC}	Acquisition time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$		4 20			4 20		μs μs
	Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
	Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		80	110		dB
	Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES:

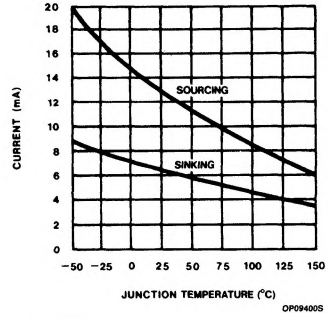
1. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_J = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a $0.01\mu F$ hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. The parameters are guaranteed over a supply voltage of ±5 to ±18V.

TYPICAL DC PERFORMANCE CHARACTERISTICS

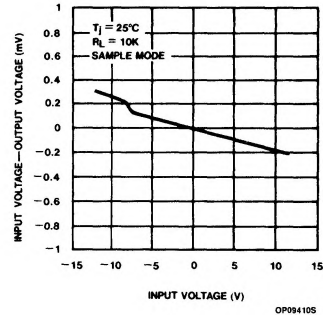
Input Bias Current



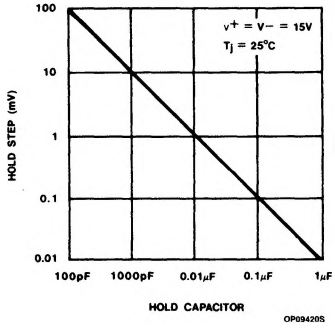
Output Short Circuit Current



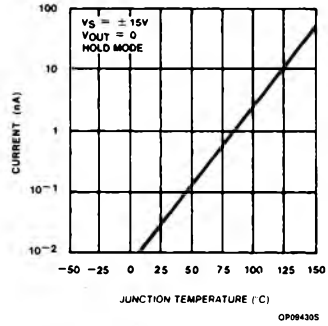
Gain Error



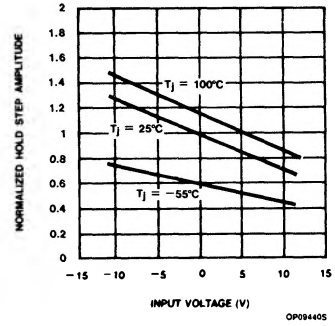
Hold Step



Leakage Current Into Hold Capacitor

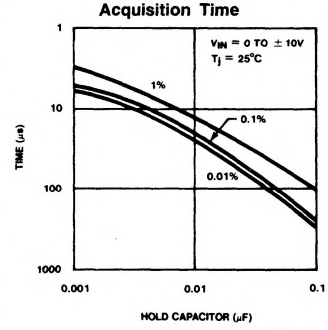


Hold Step Input Voltage

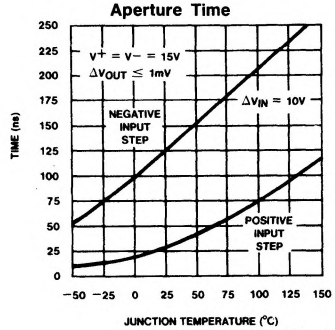


TYPICAL AC PERFORMANCE CHARACTERISTICS

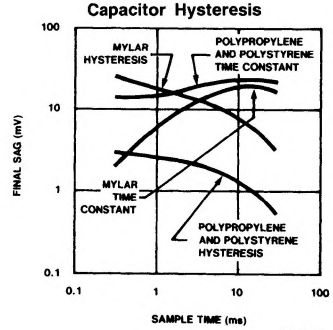
Acquisition Time



Aperture Time

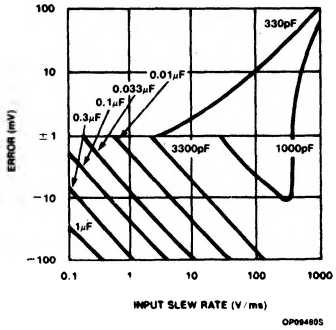


Capacitor Hysteresis



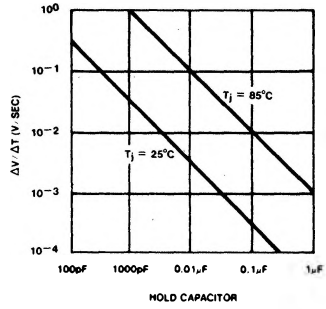
TYPICAL AC PERFORMANCE CHARACTERISTICS (Continued)

Dynamic Sampling Error



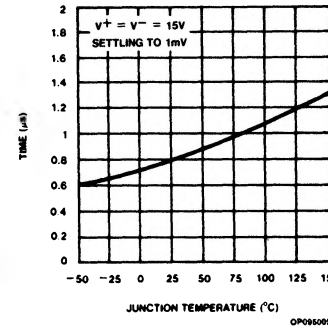
OP09480S

Output Droop Rate



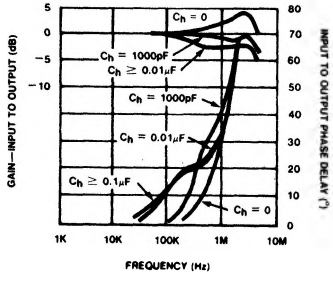
OP09490S

'Hold' Settling Time



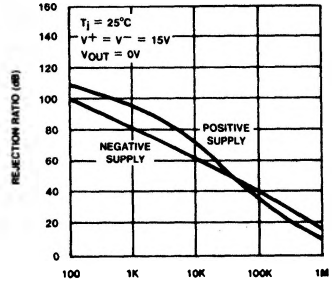
OP09500S

Phase And Gain (Input to Output, Small-Signal)



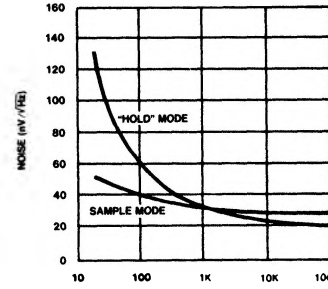
OP09510S

Power Supply Rejection



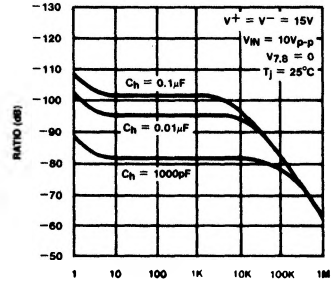
OP09520S

Output Noise



OP09530S

Feedthrough Rejection Ratio (Hold Mode)



OP09541S