LF198JAN Monolithic Sample-and-Hold Circuits

Check for Samples: LF198JAN

FEATURES

- **Operates from ±5V to ±18V supplies**
- **Less than 10 µs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5 mV typical hold step at C_h = 0.01 µF**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**
- **Space Qualified**
  Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

DESCRIPTION

The LF198 is a monolithic sample-and-hold circuit which utilizes BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 µF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

Connection Diagrams

Metal Can Package

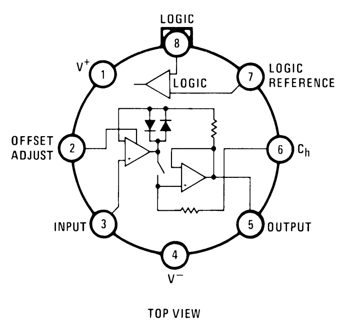


Figure 1.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Typical Connection and Performance Curve

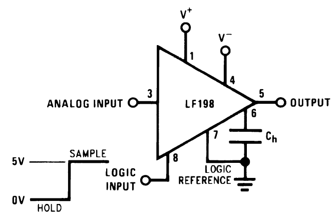
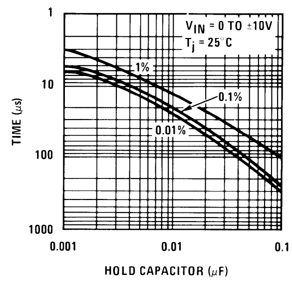
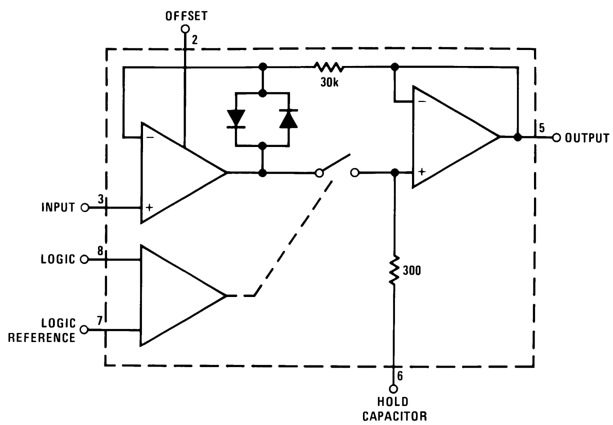


Figure 2. Acquisition Time



Functional Diagram



Absolute Maximum Ratings [1]

Supply Voltage	±18V
Power Dissipation (Package Limitation) [2]	500 mW
Operating Ambient Temperature Range	−55°C ≤ T_A ≤ +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_{Jmax})	+150°C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage [3]	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering, 10 sec.)	300°C
Thermal Resistance	
θ_{JA}	
Metal Can (Still Air @ 0.5W)	160°C/W
Metal Can (500 LF/Min Air Flow @ 0.5W)	84°C/W
θ_{JC}	
Metal Can	48°C/W
ESD Tolerance [4]	500V

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$, or the number given in the Absolute Maximum Ratings, whichever is lower. .
(3) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
(4) Human body model, 100pF discharged through 1.5KΩ

Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

Subgroup	Description	Temperature (°C)
1	Static tests at	+25°C
2	Static tests at	+125°C
3	Static tests at	−55°C
4	Dynamic tests at	+25°C
5	Dynamic tests at	+125°C
6	Dynamic tests at	−55°C
7	Functional tests at	+25°C
8A	Functional tests at	+125°C
8B	Functional tests at	−55°C
9	Switching tests at	+25°C
10	Switching tests at	+125°C
11	Switching tests at	−55°C

Electrical Characteristics DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 3.5V, $-V_{CC}$ = -26.5V, V_{CM} = 11.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		$+V_{CC}$ = 26.5V, $-V_{CC}$ = -3.5V, V_{CM} = -11.5V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		$+V_{CC}$ = 7V, $-V_{CC}$ = -3V, V_{CM} = 2V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
		$+V_{CC}$ = 3V, $-V_{CC}$ = -7V, V_{CM} = -2V		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
I_{IB}	Input Bias Current	$+V_{CC}$ = 3.5V, $-V_{CC}$ = -26.5V, V_{CM} = 11.5V		-1.0	25	nA	1
				-25	75	nA	2, 3
		$+V_{CC}$ = 26.5V, $-V_{CC}$ = -3.5V,V_{CM} = -11.5V		-1.0	25	nA	1
				-25	75	nA	2, 3
		$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V		-1	25	nA	1
				-25	75	nA	2, 3
		$+V_{CC}$ = 7V, $-V_{CC}$ = -3V, V_{CM} = 2V		-1	25	nA	1
				-25	75	nA	2, 3
		$+V_{CC}$ = 3V, $-V_{CC}$ = -7V, V_{CM} = -2V		-1.0	25	nA	1
				-25	75	nA	2, 3
Z_I	Input Impedance	$+V_{CC}$ = 3.5V to 26.6V, $-V_{CC}$ = -26.5V to -3.5V, V_{CM} = 11.5V to -11.5V		2.0		GΩ	1
				1.0		GΩ	2, 3
$V_{IO\ Adj}+$	Input Offset Voltage Adjustment	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V		6.0		mV	1, 2, 3
$V_{IO\ Adj}-$	Input Offset Voltage Adjustment	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V			-6.0	mV	1, 2, 3
PSRR+	Power Supply Rejection Ratio	$-V_{CC}$ = -18V, $+V_{CC}$ = 18V to 12V		80		dB	1, 2, 3
PSRR-	Power Supply Rejection Ratio	$+V_{CC}$ = 18V, $-V_{CC}$ = -12V to -18V		80		dB	1, 2, 3
I_{CC}	Supply Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V		1.0	5.5	mA	1,2
				1.0	6.5	mA	3
A_E	Gain Error	$+V_{CC}$ = 3.5V to 26.5V, $-V_{CC}$ = -26.5V to -3.5V, V_{CM} = -11.5V to 11.5V		-0.005	0.005	%	1
				-0.02	0.02	%	2, 3
		$+V_{CC}$ = 3V to 7V, $-V_{CC}$ = -7V to -3V, V_{CM} = -2V to 2V		-0.02	0.02	%	1
				-0.04	0.04	%	2, 3
R_{SC}	Series Charge Resistance	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V		75	400	Ω	1, 2, 3
I_{IH} (a)	Logical 1 Input Current	$+V_{CC}$ = 8.5V, $-V_{CC}$ = -21.5V		0	10	µA	1, 2, 3
I_{IH} (b)	Logical 1 Input Current	$+V_{CC}$ = 8.5V, $-V_{CC}$ = -21.5V		0	10	µA	1, 2, 3
I_{IL} (a)	Logical 0 Input Current	$+V_{CC}$ = 21.5V, $-V_{CC}$ = -8.5V		-1.0	1.0	µA	1, 2, 3
I_{IL} (b)	Logical 0 Input Current	$+V_{CC}$ = 21.5V, $-V_{CC}$ = -8.5V		-1.0	1.0	µA	1, 2, 3
$I_{OS}+$	Output Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V		-25		mA	1, 2, 3
$I_{OS}-$	Output Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V			25	mA	1, 2, 3

Electrical Characteristics DC Parameters (continued)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$I_{CH}+$	Hold Capacitor Charge Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V			-3.0	mA	1
					-2.0	mA	2, 3
$I_{CH}-$	Hold Capacitor Charge Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V		3.0		mA	1
				2.0		mA	2, 3
V_{Th}(H)	Differential Logic Threshold	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V Logic = 2.0V, Logic Ref = 2.0V		1.0		mA	1, 2, 3
V_{Th}(L)	Differential Logic Threshold	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V Logic = 0.8V, Logic Ref = 2.0V		-10	10	µA	1, 2, 3
$I_{HL}+$	Hold Mode Leakage Current	$+V_{CC}$ = 3.5V, $-V_{CC}$ = -26.5V, V_{CM} = -11.5V	(1)	-0.100	0.100	nA	1
				-50	50	nA	2
$I_{HL}-$	Hold Mode Leakage Current	$+V_{CC}$ = 26.5V, $-V_{CC}$ = -3.5V, V_{CM} = 11.5V	(2)	-0.100	0.100	nA	1
				-50	50	nA	2
Z_O	Output Impedance	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V			2.0	Ω	1, 2, 3
V_{HS}	(HOLD) Step Voltage	$+V_{CC}$ = 3.5V, $-V_{CC}$ = -26.5V, V_{CM} = 11.5V	(3)	-2.0	2.0	mV	1
				-5.0	5.0	mV	2, 3
		$+V_{CC}$ = 26.5V, $-V_{CC}$ = -3.5V, V_{CM} = -11.5V	(3)	-2.0	2.0	mV	1
				-5.0	5.0	mV	2, 3
F_{RR}	Feedthrough Rejection Ratio	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V, V_I = 0V to 11.5V		86		dB	1
				80		dB	2, 3
		$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V, V_I = 11.5V to 0V		86		dB	1
				80		dB	2, 3
		$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V, V_I = 0V to -11.5V		86		dB	1
				80		dB	2, 3
		$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V, V_I = -11.5V to 0V		86		dB	1
				80		dB	2, 3

(1) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
(2) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
(3) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

AC/DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
Delta V_{IO} / Delta T	Input Offset Voltage Temp Sensitivity			-20	20	µV/°C	8A, 8B
T_{AQ}	Aquisition Time	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V			25	µS	7
T_{AP}	Aperture Time	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V			300	nS	7
T_S	Settling Time	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V			1.5	µS	7
F_{RR} AC	Feedthrough Rejection Ratio	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_I = 20Vpp		86		dB	7
TR_{TS}	Transient Response (settling time)	$+V_{CC}$ = 3.5V, $-V_{CC}$ = -26.5V, V_I = 100mV pulse			2.5	µS	7
		$+V_{CC}$ = 26.5V, $-V_{CC}$ = -3.5V, V_I = 100mV pulse			2.5	µS	7
TR_{OS}	Transient Response (overshoot)	$+V_{CC}$ = 3.5V, $-V_{CC}$ = -26.5V, V_I = 100mV pulse			40	%	7
		$+V_{CC}$ = 26.5V, $-V_{CC}$ = -3.5V, V_I = 100mV pulse			40	%	7
en_H	Noise	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V			10	mV_{RMS}	7
en_S	Noise	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V			10	mV_{RMS}	7

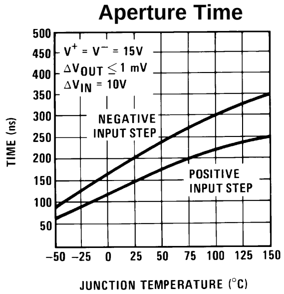
DC Parameters: Drift Values

Delta calculations performed on S-Level devices at group B, subgroup 5 ONLY.

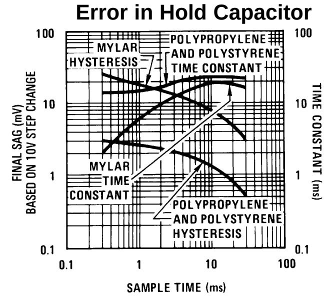
Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V		-0.5	0.5	mV	1
I_{IB}	Input Bias Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, V_{CM} = 0V		-2.5	2.5	nA	1

Typical Performance Characteristics

Aperture Time

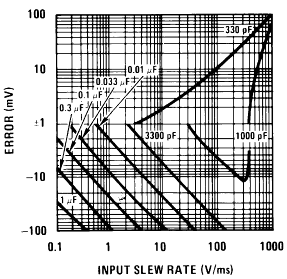


(1)Dielectric Absorption Error in Hold Capacitor

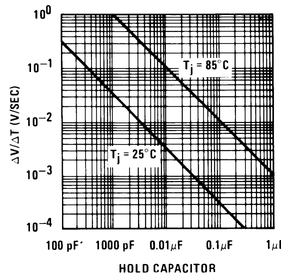


Dynamic Sampling Error

(1)

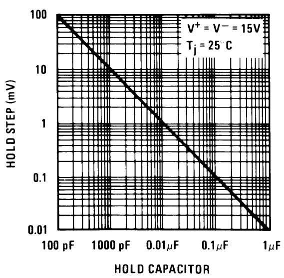


Output Droop Rate



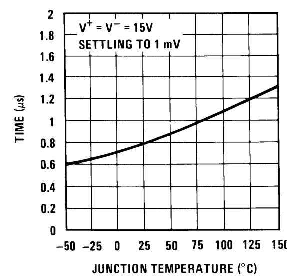
Hold Step

(1)

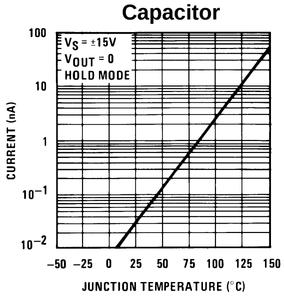


"Hold" Settling Time

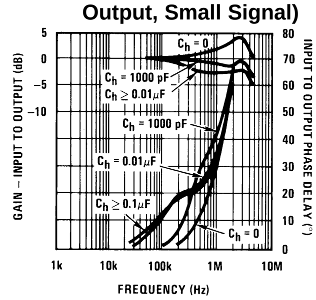
(1)



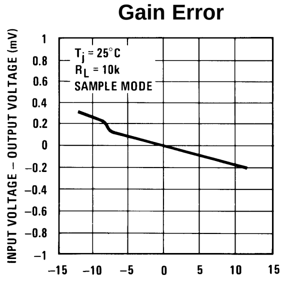
Leakage Current into Hold Capacitor



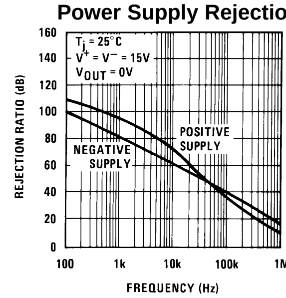
Phase and Gain (Input to Output, Small Signal)



Gain Error



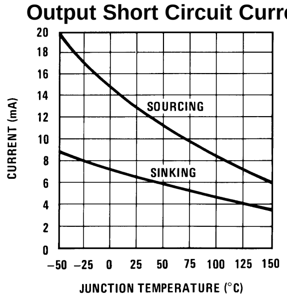
Power Supply Rejection



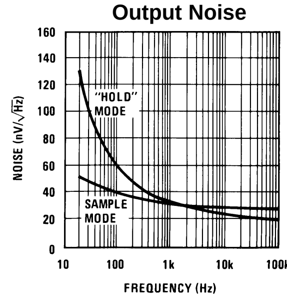
(1) See Definition of Terms

Typical Performance Characteristics (continued)

Output Short Circuit Current

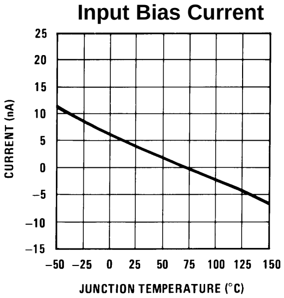


Output Noise

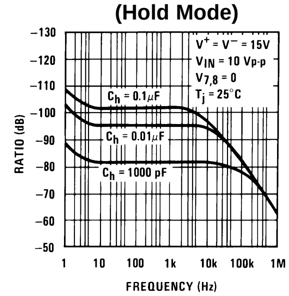


See Definition

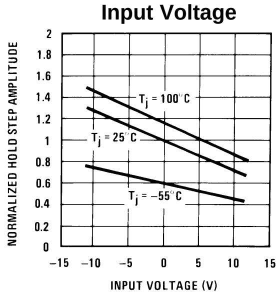
Input Bias Current



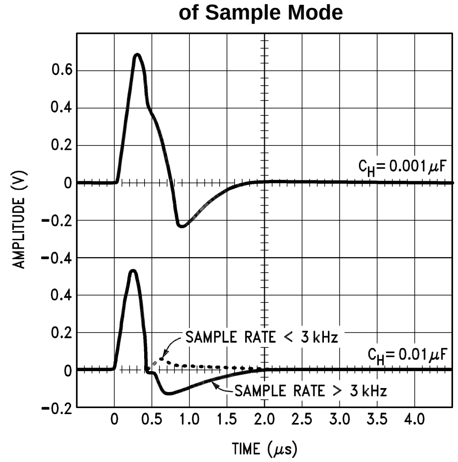
Feedthrough Rejection Ratio (Hold Mode)



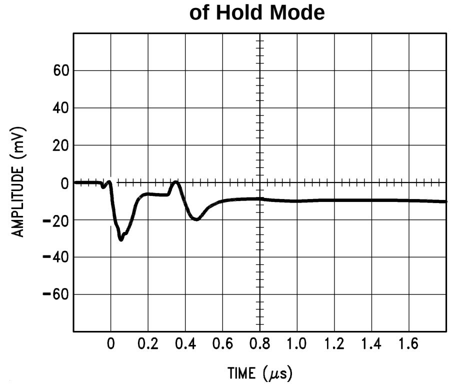
Hold Step vs Input Voltage



Output Transient at Start of Sample Mode

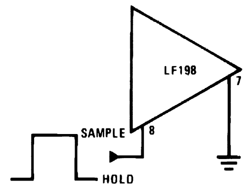


Output Transient at Start of Hold Mode

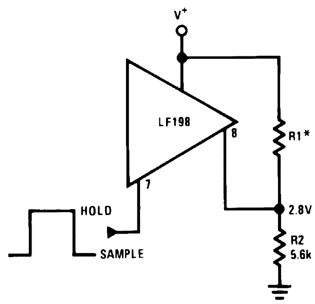


Logic Input Configurations

TTL & CMOS
3V ≤ V_{LOGIC} (Hi State) ≤ 7V

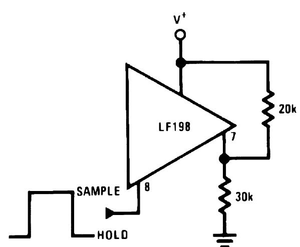


Threshold = 1.4V

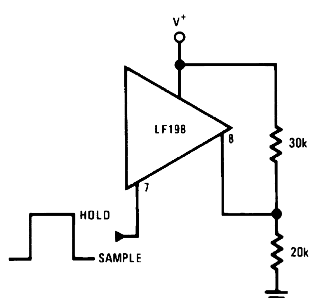


Threshold = 1.4V*Select for 2.8V at pin 8

CMOS
7V ≤ V_{LOGIC} (Hi State) ≤ 15V

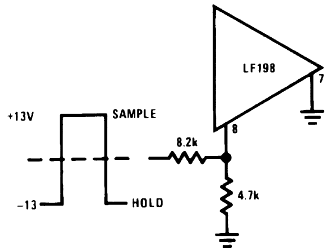


Threshold = 0.6 (V^+) + 1.4V

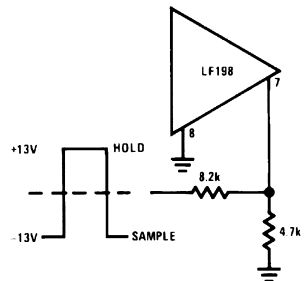


Threshold = 0.6 (V^+) − 1.4V

Op Amp Drive



Threshold ≈ +4V



Threshold = −4V

Application Hints

HOLD CAPACITOR

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may “sag back” up to 0.2% after a quick change in voltage. A long sample time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. Most ceramic capacitors are unusable with > 1% hysteresis. Ceramic “NPO” or “COG” capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see the curve *Dielectric Absorption Error.* The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10—50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC AND AC ZEROING

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01 μF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

LOGIC RISE TIME

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/μs.

SAMPLING DYNAMIC SIGNALS

Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the “hold” command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1 μs)(0.6V/μs)= 60 mVerror if the “hold” signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 μs) (0.6 V/μs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the “hold” command. This curve is based on a 1 mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1 mV after the “hold” command.

DIGITAL FEEDTHROUGH

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input and the C_h pin. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Guarding Technique

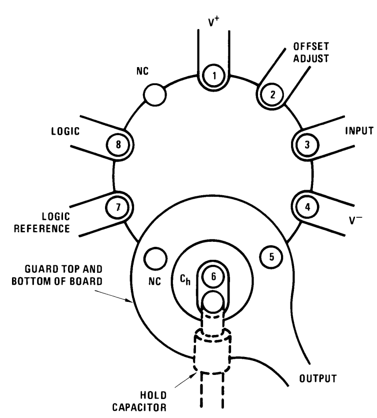
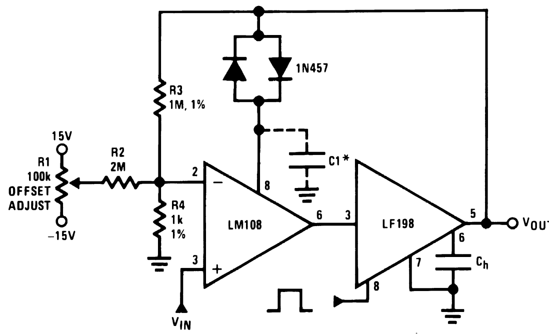


Figure 3. Use 10-pin layout. Guard around $C_h$is tied to output.

Typical Applications

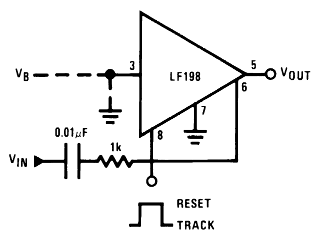
Figure 4. X1000 Sample & Hold



*For lower gains, the LM108 must be frequency compensated

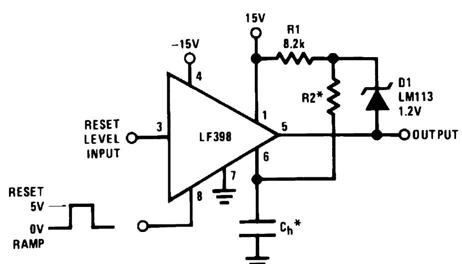
Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Figure 5. Sample and Difference Circuit (Output Follows Input in *Hold* Mode)



$V_{OUT} = V_B + \Delta V_{IN}$(HOLD MODE)

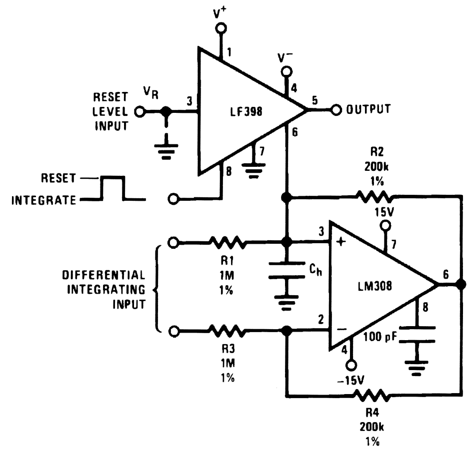
Figure 6. Ramp Generator with Variable Reset Level



*Select for ramp rate $\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)(C_h)}$

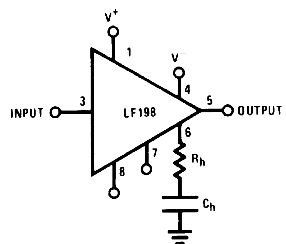
R2 ≥ 10k

Figure 7. Integrator with Programmable Reset Level



$$V_{OUT}\ (\text{Hold Mode}) = \left[\frac{1}{(R1)\ (C_h)} \int_0^t V_{IN}\,dt\right] + \left[V_R\right]$$

Figure 8. Output Holds at Average of Sampled Input



$$\text{Select } (R_h)\ (C_h) \gg \frac{1}{2\pi f_{IN}\ (\text{Min})}$$

Figure 9. Increased Slew Current

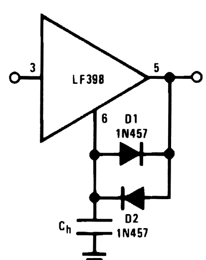
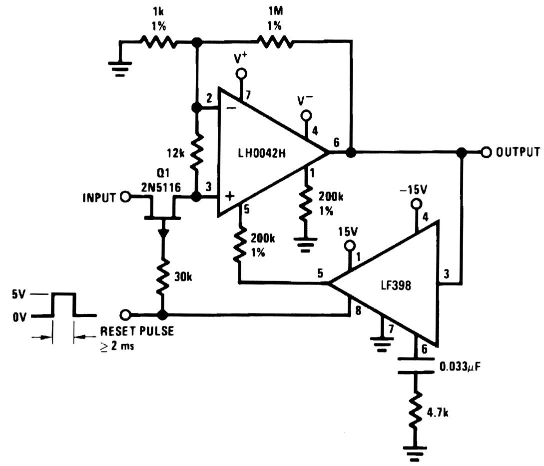


Figure 10. Reset Stabilized Amplifier (Gain of 1000)



$V_{OS} \leq 20\mu V$ (No trim)

$Z_{IN} \approx 1\ M\Omega$

$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/sec$

$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/°C$

Figure 11. Fast Acquisition, Low Droop Sample & Hold

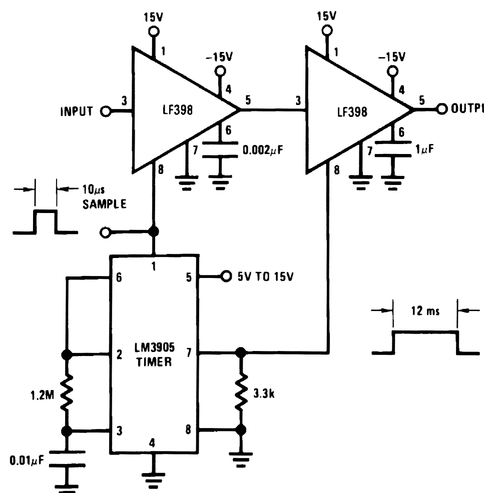


Figure 12. Synchronous Correlator for Recovering Signals Below Noise Level

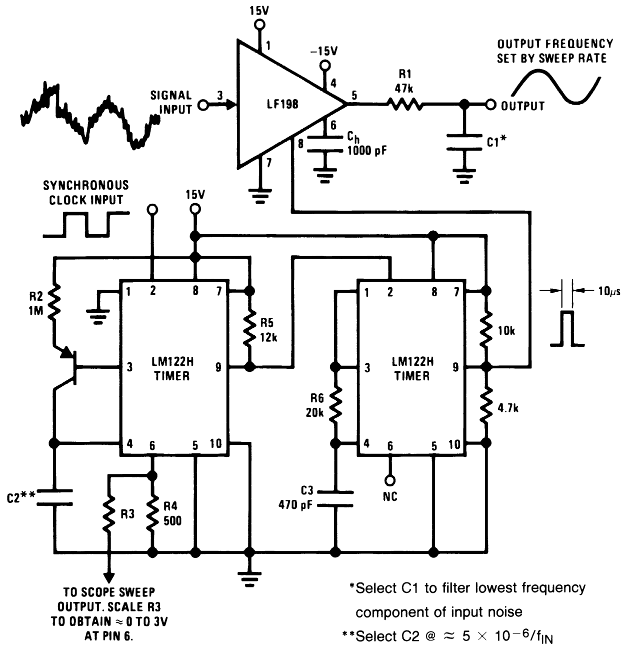
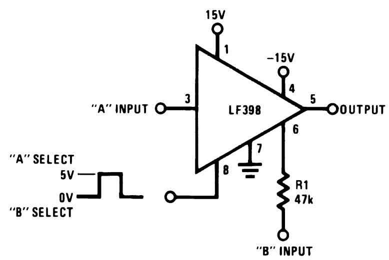


Figure 13. 2–Channel Switch



	A	B
Gain	1 ± 0.02%	1 ± 0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≈ 1 MHz	≈ 400 kHz
Crosstalk	−90 dB	−90 dB
@ 1 kHz		
Offset	≤ 6 mV	≤ 75 mV

Figure 14. DC & AC Zeroing

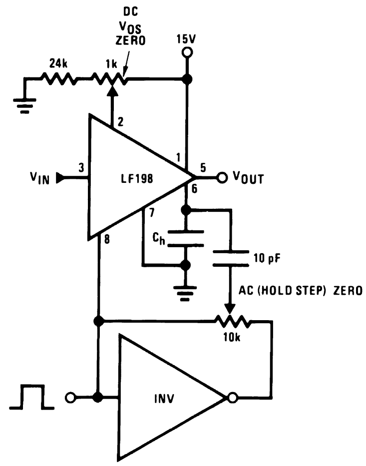
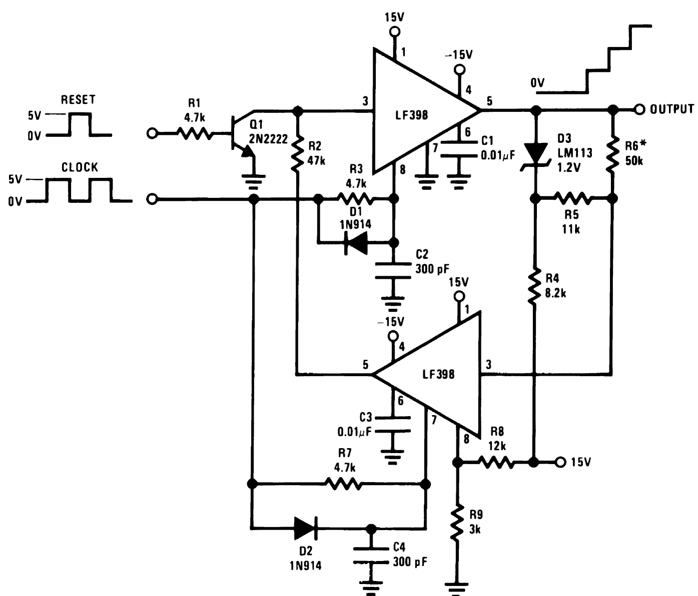


Figure 15. Staircase Generator



*Select for step height
50k → ≅ 1V Step

Figure 16. Differential Hold

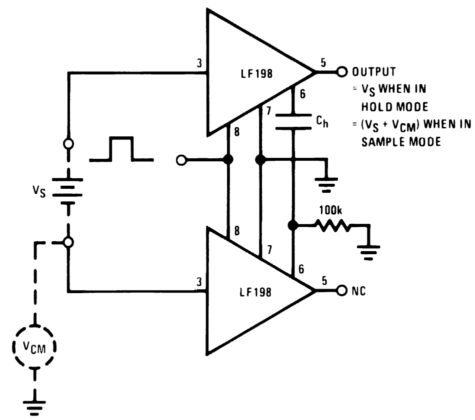
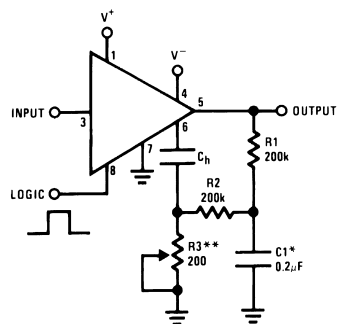


Figure 17. Capacitor Hysteresis Compensation



*Select for time constant $C1 = \frac{\tau}{100k}$

**Adjust for amplitude

Definition of Terms

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the “hold” logic command.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between “Hold” command and an input analog transition, so that the transition does not affect the held output.

REVISION HISTORY SECTION

Date Released	Revision	Section	Originator	Changes
02/25/05	A	New release, Corporate format	L. Lytle	1 MDS converted to corp. datasheet format. MJLF198–X Rev 2B0 MDS to be archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
JL198BGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL198BGA JM38510/12501BGA Q ACO JM38510/12501BGA Q >T	Samples
JL198SGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL198SGA JM38510/12501SGA Q ACO JM38510/12501SGA Q >T	Samples
JM38510/12501BGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL198BGA JM38510/12501BGA Q ACO JM38510/12501BGA Q >T	Samples
JM38510/12501SGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL198SGA JM38510/12501SGA Q ACO JM38510/12501SGA Q >T	Samples
M38510/12501BGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL198BGA JM38510/12501BGA Q ACO JM38510/12501BGA Q >T	Samples
M38510/12501SGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL198SGA JM38510/12501SGA Q ACO JM38510/12501SGA Q >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] Only one of markings shown within the brackets will appear on the physical device.

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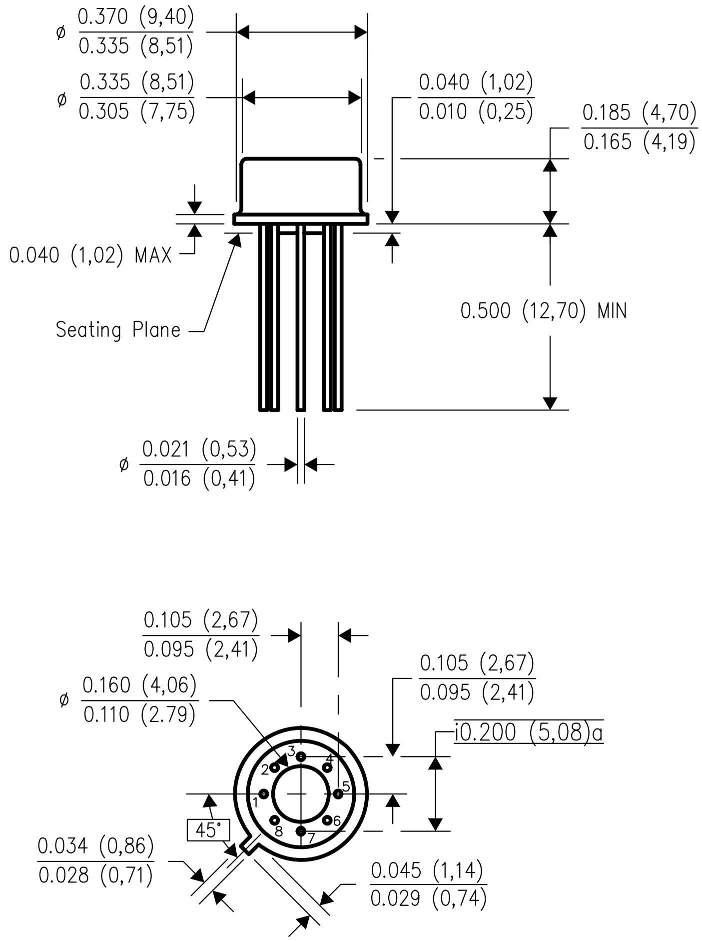
OTHER QUALIFIED VERSIONS OF LF198JAN, LF198JAN-SP :

- Military: LF198JAN
- Space: LF198JAN-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

LMC (O-MBCY-W8) METAL CYLINDRICAL PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
- D. Pin numbers shown for reference only. Numbers may not be marked on package.
- E. Falls within JEDEC MO-002/TO-99.

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