

LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

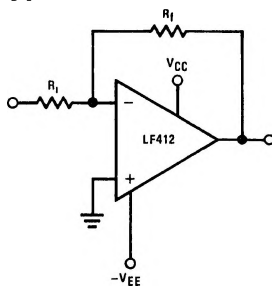
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage 1 mV (max)
- Input offset voltage drift 10 $\mu\text{V}/^\circ\text{C}$ (max)
- Low input bias current 50 pA
- Low input noise current 0.01 pA/ $\sqrt{\text{Hz}}$
- Wide gain bandwidth 3 MHz (min)
- High slew rate 10V/ μs (min)
- Low supply current 1.8 mA/Amplifier
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10\text{k}$, $V_O = 20\text{ Vp-p}$, BW = 20 Hz-20 kHz $\leq 0.02\%$
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Typical Connection



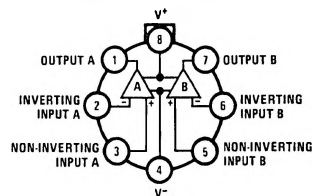
Ordering Information

LF412XYZ

- X indicates electrical grade
- Y indicates temperature range
- "M" for military
- "C" for commercial
- Z indicates package type
- "H" or "N"

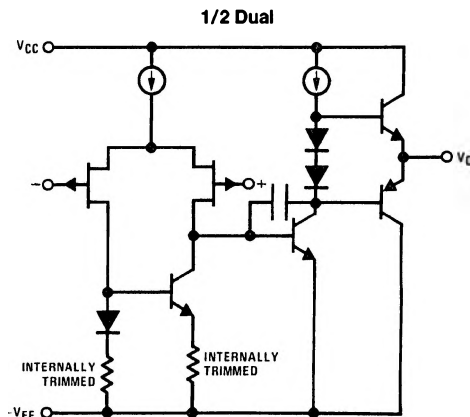
Connection Diagrams

Metal Can Package



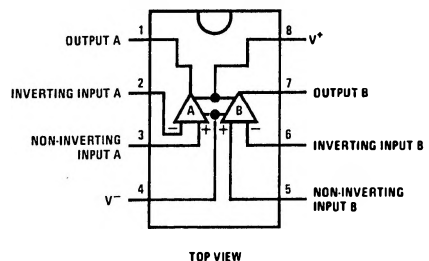
Note. Pin 4 connected to case.
TOP VIEW

Simplified Schematic



**Order Number LF412AMH,
LF412MH, LF412ACH or LF412CH**
See NS Package Number H08B

Dual-In-Line Package



TOP VIEW

**Order Number LF412ACJ, LF412CJ,
LF412ACN or LF412CN**
See NS Package Number J08A or N08E

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 9)

	LF412A	LF412		H Package (Note 3)	N Package
Supply Voltage	±22V	±18V	Power Dissipation (Note 10)	150°C	670 mW
Differential Input Voltage	±38V	±30V	T_j max	150°C	115°C
Input voltage Range (Note 1)	±19V	±15V	θ_{JA} (Typical)	152°C/W	115°C/W
Output Short Circuit Duration (Note 2)	Continuous	Continuous	Operating Temp. Range	(Note 4)	(Note 4)
			Storage Temp. Range	-65°C ≤ T _A ≤ 150°C - 65°C ≤ T _A ≤ 150°C	
			Lead Temp. (Soldering, 10 sec.)	260°C	260°C
			ESD rating to be determined.		

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF412A			LF412			Units
			Min	Typ	Max	Min	Typ	Max	
V _{OS}	Input Offset Voltage	R _S = 10 kΩ, T _A = 25°C		0.5	1.0		1.0	3.0	mV
ΔV _{OS} /ΔT	Average TC of Input Offset Voltage	R _S = 10 kΩ (Note 6)		7	10		7	20 (Note 6)	μV/°C
I _{OS}	Input Offset Current	V _S = ±15V (Notes 5 and 7)	T _J = 25°C	25	100		25	100	pA
					2			2	nA
					25			25	nA
I _B	Input Bias Current	V _S = ±15V (Notes 5 and 7)	T _J = 25°C	50	200		50	200	pA
					4			4	nA
					50			50	nA
R _{IN}	Input Resistance	T _J = 25°C		10 ¹²			10 ¹²		Ω
A _{VOL}	Large Signal Voltage Gain	V _S = ±15V, V _O = ±10V, R _L = 2k, T _A = 25°C	50	200		25	200		V/mV
		Over Temperature	25	200		15	200		V/mV
V _O	Output Voltage Swing	V _S = ±15V, R _L = 10k	±12	±13.5		±12	±13.5		V
V _{CM}	Input Common-Mode Voltage Range		±16	+19.5		±11	+14.5		V
				-16.5			-11.5		V
CMRR	Common-Mode Rejection Ratio	R _S ≤ 10k	80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)	80	100		70	100		dB
I _S	Supply Current	V _O = 0V, R _L = ∞		3.6	5.6		3.6	6.5	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF412A			LF412			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	T _A = 25°C, f = 1 Hz-20 kHz (Input Referred)		-120			-120		dB
SR	Slew Rate	V _S = ±15V, T _A = 25°C	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	V _S = ±15V, T _A = 25°C	3	4		2.7	4		MHz
e _n	Equivalent Input Noise Voltage	T _A = 25°C, R _S = 100Ω, f = 1 kHz		25			25		nV/√Hz
i _n	Equivalent Input Noise Current	T _A = 25°C, f = 1 kHz		0.01			0.01		pA/√Hz

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} .

Note 4: These devices are available in both the commercial temperature range $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ and the military temperature range $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only. In all cases the maximum operating temperature is limited by internal junction temperature T_J max.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20\text{V}$ for the LF412A and for $V_S = \pm 15\text{V}$ for the LF412. V_{OS} , I_B , and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 85% of the amplifiers meet this specification.

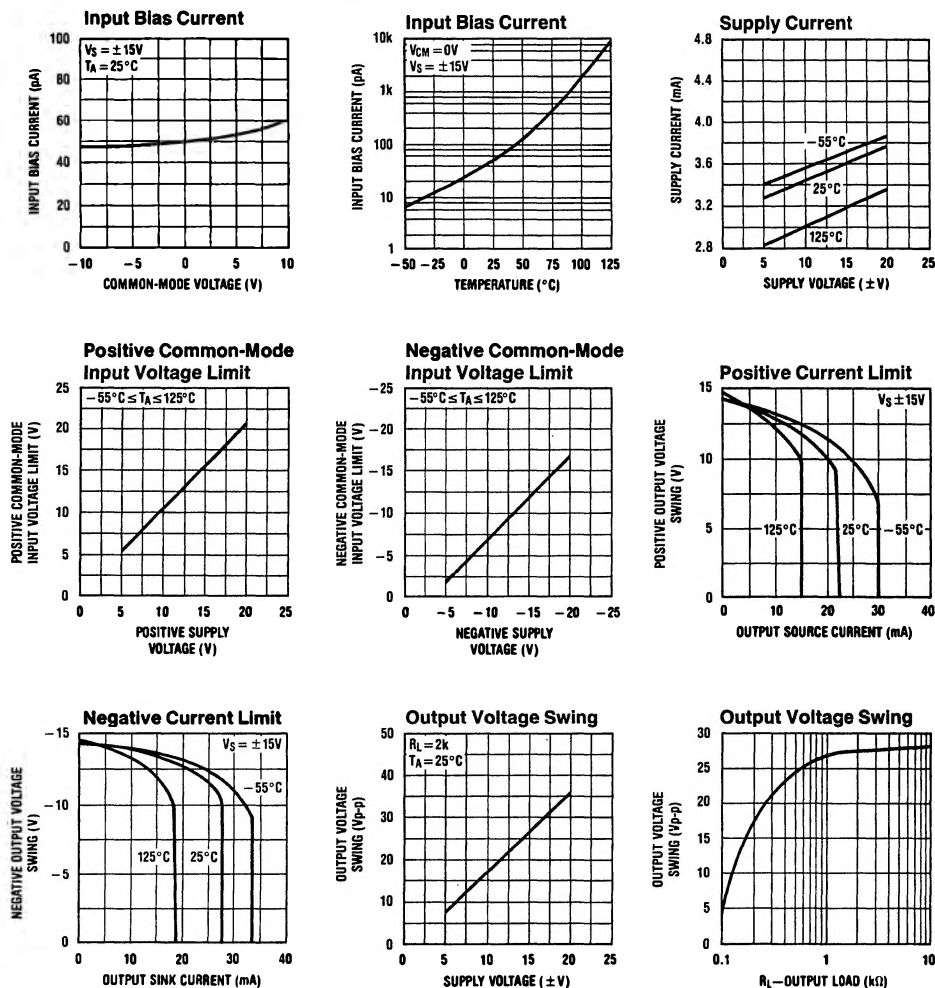
Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm 6\text{V}$ to $\pm 15\text{V}$.

Note 9: Refer to RETS412AX for LF412AMH military specifications and to RETS412X for LF412MH military specifications.

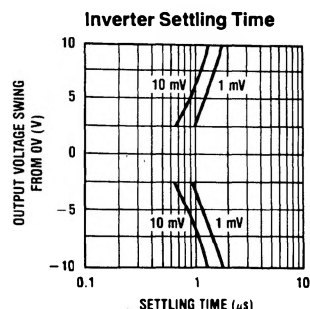
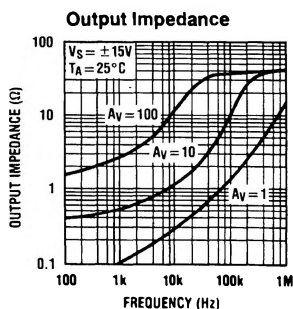
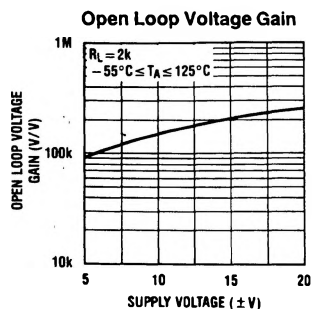
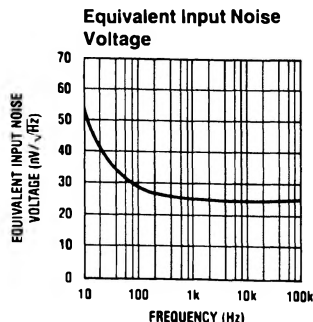
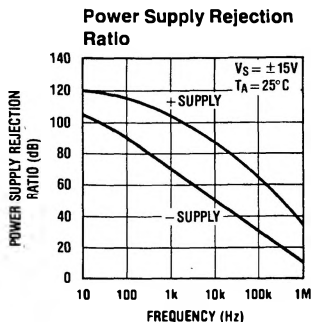
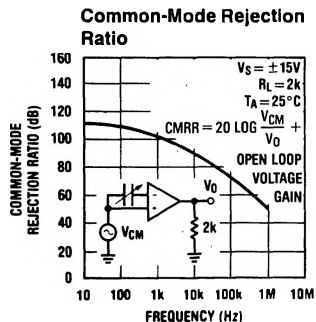
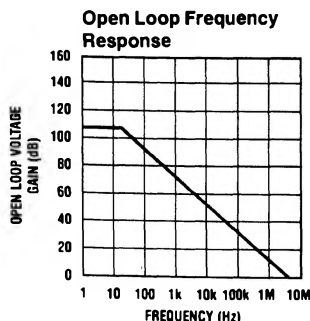
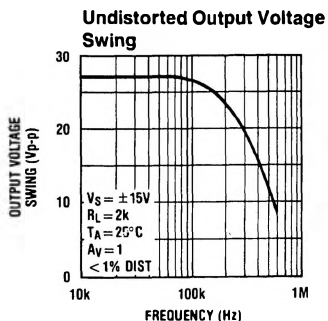
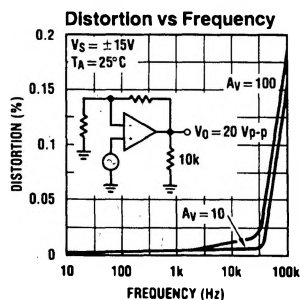
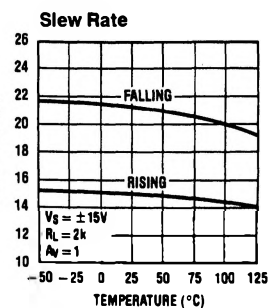
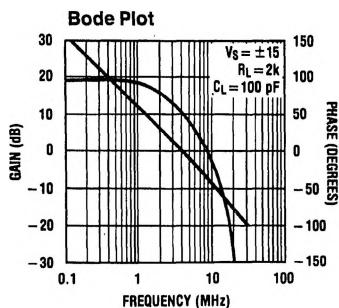
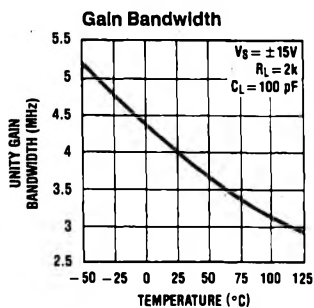
Note 10: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics



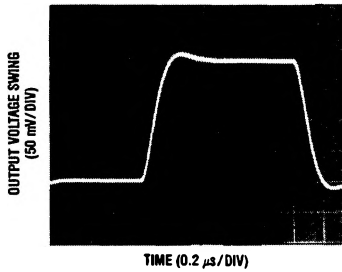
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Typical Performance Characteristics (Continued)

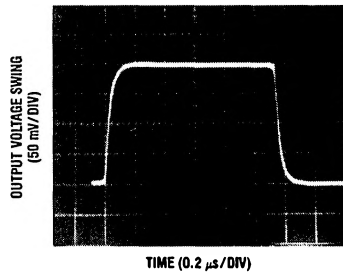


Pulse Response $R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$

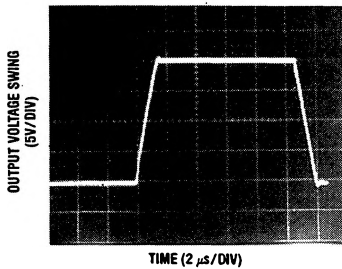
Small Signal Inverting



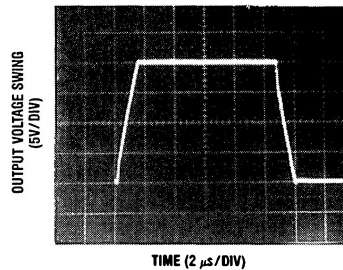
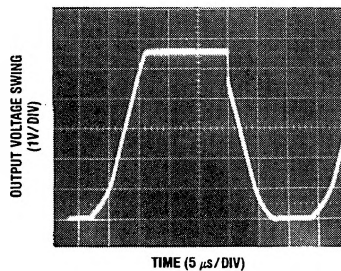
Small Signal Non-Inverting



Large Signal Inverting



Large Signal Non-Inverting

Current Limit ($R_L = 100\Omega$)

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Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Application Hints (Continued)

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 6.0V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a $2\text{ k}\Omega$ load resistance to $\pm 10V$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

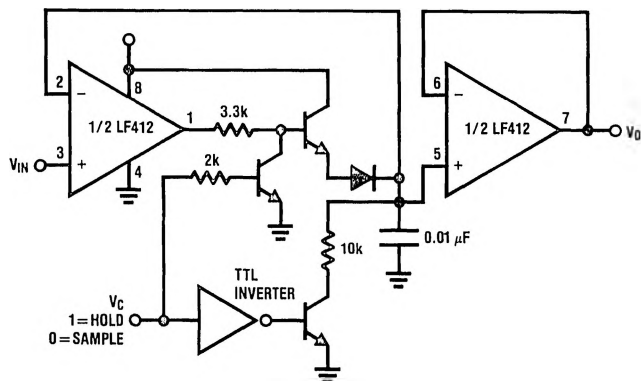
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

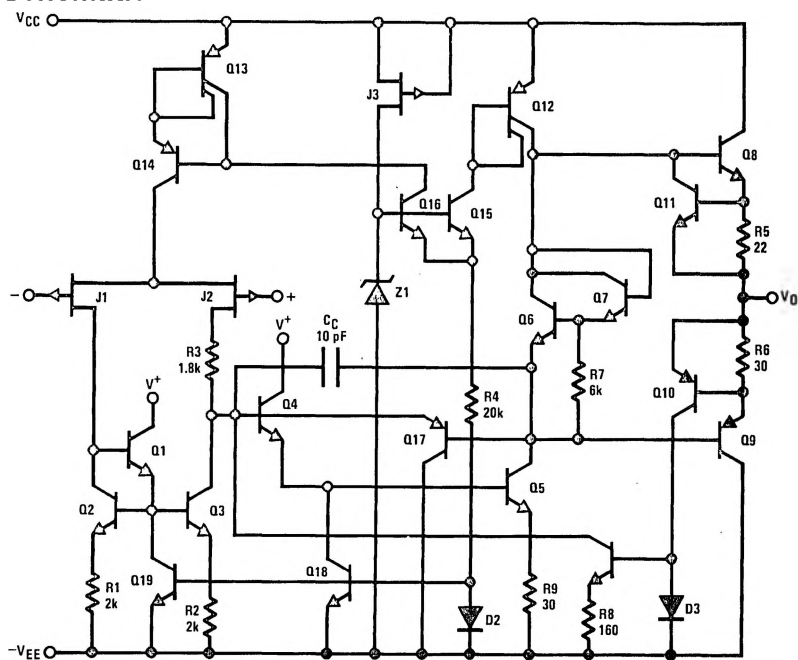
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

Single Supply Sample and Hold



Detailed Schematic



TL/H/5658-9