National Semiconductor

LH0023/LH0023C/LH0043/LH0043C Sample and Hold Circuits

General Description

The LH0023/LH0023C and LH0043/LH0043C are complete sample and hold circuits including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. They are designed to operate from standard ±15V DC supplies, but provision is made on the LH0023/LH0023C for connection of a separate +5V logic supply in minimum noise applications. The principal difference between the LH0023/LH0023C and the LH0043/LH0043C is a 10:1 trade-off in performance between sample accuracy and sample acquisition time. Devices are pin compatible except for TTL logic polarity.

The LH0023/LH0023C and LH0043/LH0043C are ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. They offer significant cost and size reduction over equivalent module or discrete designs. Each device is available in a hermetic TO-8 package and is completely specified over both full military and industrial temperature ranges.

The LH0023 and LH0043 are specified for operation over the −55°C to +125°C military temperature range. The LH0023C and LH0043C are specified for operation over the −25°C to +85°C temperature range.

Features

LH0023/LH0023C

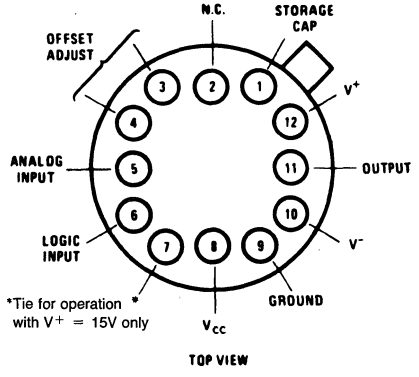
- Sample accuracy–0.01% max
- Hold drift rate–0.5 mV/sec typ
- Sample acquisition time–100 μs max for 20V
- Aperture time–150 ns typ
- Wide analog input range– ±10V min
- Logic input–TTL/DTL compatible
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

LH0043/LH0043C

- Sample acquisition time–15 μs max for 20V
  4 μs typ for 5V
- Aperture time–20 ns typ
- Hold drift rate–1 mV/sec typ
- Sample accuracy–0.1% max
- Wide analog input range– ±10V min
- Logic input–TTL/DTL compatible
- Offset adjustable to zero with single 10k pot
- Output short circuit protection

Connection Diagrams

LH0023/LH0023C



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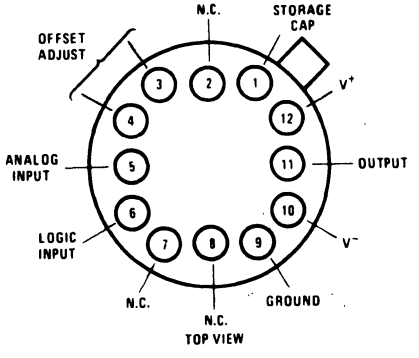
LH0043/LH0043C



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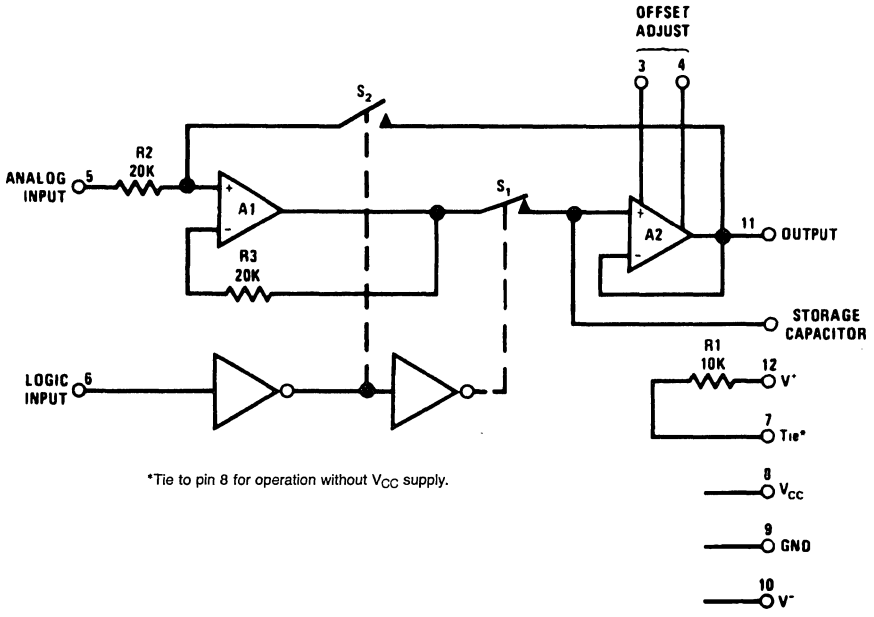
Order Number LH0023G or LH0023CG or LH0043G or LH0043CG
See Package Number G12B

Block Diagrams

LH0023/LH0023C



*Tie to pin 8 for operation without V_{CC} supply.

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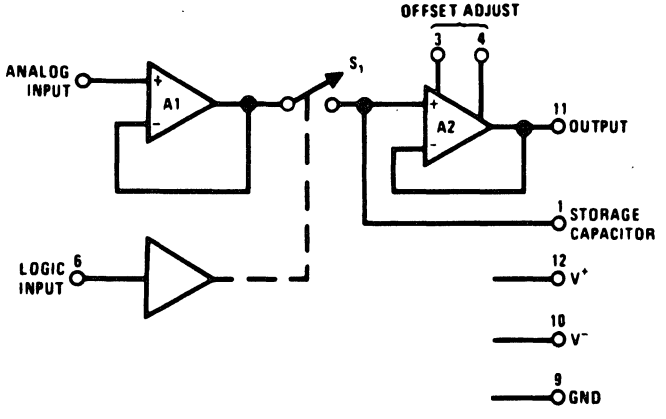
LH0043/LH0043C



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_S)	±20V
Logic Supply Voltage (V_{CC}) LH0023, LH0023C	+7.0V
Logic Input Voltage (V_6)	+5.5V
Analog Input Voltage (V_5)	±15V
Power Dissipation	See graph
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0023, LH0043	−55°C to +125°C
LH0023C, LH0043C	−25°C to +85°C
Storage Temperature Range	−65°C to −150°C
Lead Soldering (10 seconds)	300°C

Electrical Characteristics LH0023/LH0023C (Note 1)

Parameter	Conditions	Limits						Units
		LH0023			LH0023C			
		Min	Typ	Max	Min	Typ	Max	
Sample (Logic "1") Input Voltage	V_{CC} = 4.5V	2.0			2.0			V
Sample (Logic "1") Input Current	V_6 = 2.4V, V_{CC} = 5.5V			5.0			5.0	μA
Hold (Logic "0") Input Voltage	V_{CC} = 4.5V			0.8			0.8	V
Hold (Logic "0") Input Current	V_6 = 0.4V, V_{CC} = 5.5V			0.5			0.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current – I_{10}	V_5 = 0V, V_6 = 2V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_{12}	V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_8	V_8 = 5.0V, V_5 = 0		1.0	1.6		1.0	1.6	mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.002	0.01		0.002	0.02	%
DC Input Resistance	Sample Mode Hold Mode	500 20	1000 25		300 20	1000 25		kΩ kΩ
Input Current – I_5	Sample Mode		0.2	1.0		0.3	1.5	μA
Input Capacitance			3.0			3.0		pF
Leakage Current – pin 1	V_5 = ±10V; V_{11} = ±10V,		10.0	200		20.0	500	pA
	−55°C≤T_A ≤ 125°C V_5 = ±10V; V_{11} = ±10V			5.0			2.0	nA
Drift Rate	V_{OUT} = ±5V, C_S = 0.01 μF, T_A = 25°C		0.5			0.5		mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_A = 25°C		1.0	20		2.0	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF			0.50			0.2	mV/ms
Aperture Time			150			150		ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.01 μF		50	100		50	100	μs
Output Amplifier Slew Rate		1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	R_S ≤ 10k, V_5 = 0V, V_6 = 2.0V			±20			±20	mV
Analog Voltage	R_L ≥ 1k, T_A = 25°C	±10	±11		±10	±11		V
Output Range	R_L ≥ 2k	±10	±12		±10	±12		V

Note 1: Unless otherwise noted, these specifications apply for V^+ = +15V, V_{CC} = +5V, V^- = −15V, pin 9 grounded, a 0.01μF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0023, and −25°C to +85°C for the LH0023C. All typical values are for T_A = 25°C.

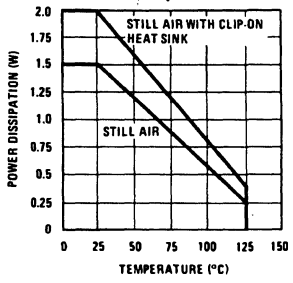
Electrical Characteristics LH0043/LH0043C: (Note 2)

Parameter	Conditions	Limits						Units
		LH0043			LH0043C			
		Min	Typ	Max	Min	Typ	Max	
Hold (Logic "1") Input Voltage		2.0			2.0			V
Hold (Logic "1") Input Current	V_6 = 2.4V			5.0			5.0	μA
Sample (Logic "0") Input Voltage				0.8			0.8	V
Sample (Logic "0") Input Current	V_6 = 0.4V			1.5			1.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	V_5 = 0V, V_6 = 2V, V_{11} = 0V V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		20 14	22 18		20 14	22 18	mA mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.02	0.1		0.02	0.3	%
DC Input Resistance	T_C = 25°C	10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Current – I_5			1.0	5.0		2.0	10.0	nA
Input Capacitance			1.5			1.5		pF
Leakage Current–pin 1	V_5 = ±10V; V_{11} = ±10, T_C = 25°C V_5 = ±10V; V_{11} = ±10V		10 10	25 25		20 2	50 5	pA nA
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF, T_C = 25°C		10	25		20	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF		10	25		2	5	mV/ms
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_C = 25°C		1	2.5		2	5	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF		1	2.5		0.2	0.5	mV/ms
Aperture Time			20	60		20	60	ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.001 μF ΔV_{OUT} = 20V, C_S = 0.01 μF ΔV_{OUT} = 5V, C_S = 0.001 μF		10 30 4	15 50		10 30 4	15 50	μs μs μs
Output Amplifier Slew Rate	V_{OUT} = 5V, C_S = 0.001 μF	1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	R_S ≤ 10k, V_5 = 0V, V_6 = 0V			±40			±40	mV
Analog Voltage Output Range	R_L ≥ 1k, T_A = 25°C R_L ≥ 2k	±10 ±10	±11 ±12		±10 ±10	±11 ±12		V V

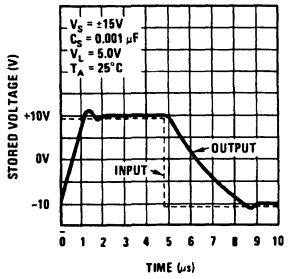
Note 2: Unless otherwise noted, these specifications apply for V^+ = ±15V, V^- = −15V, pin 9 grounded, a 5000 pF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0043, and −25°C to +85°C for the LH0043C. All typical values are for T_C = 25°C.

Typical Performance Characteristics

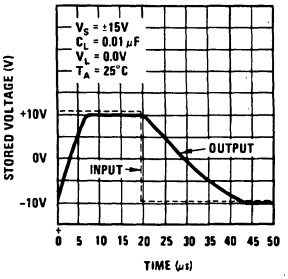
Power Dissipation



Sample Acquisition Time—LH0043



Sample Acquisition Time—LH0043



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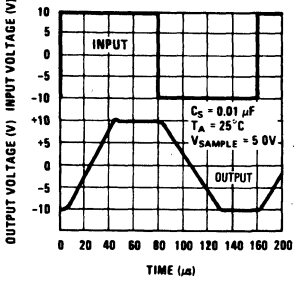
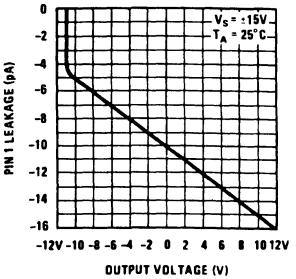
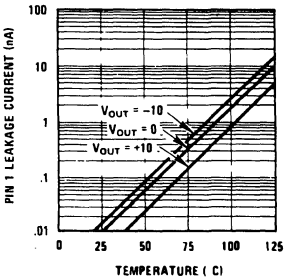
Sample Acquisition Time—LH0023



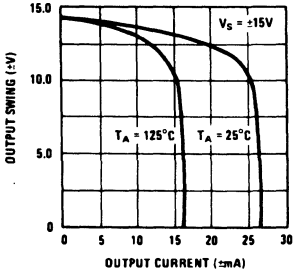
Pin 1 Leakage Current vs Output Voltage



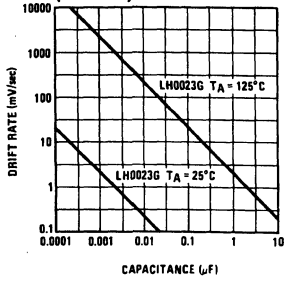
Pin 1 Leakage Current vs Temperature



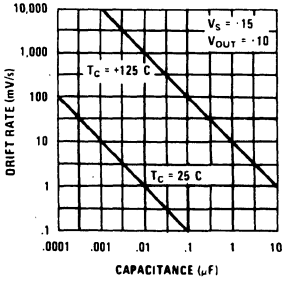
Output Current Limiting



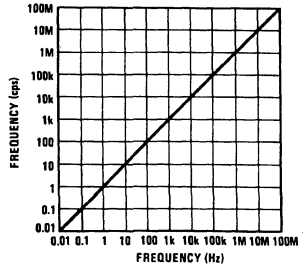
Drift vs Capacitance (LH0023)



Drift vs Capacitance (LH0043)



(LH0023)



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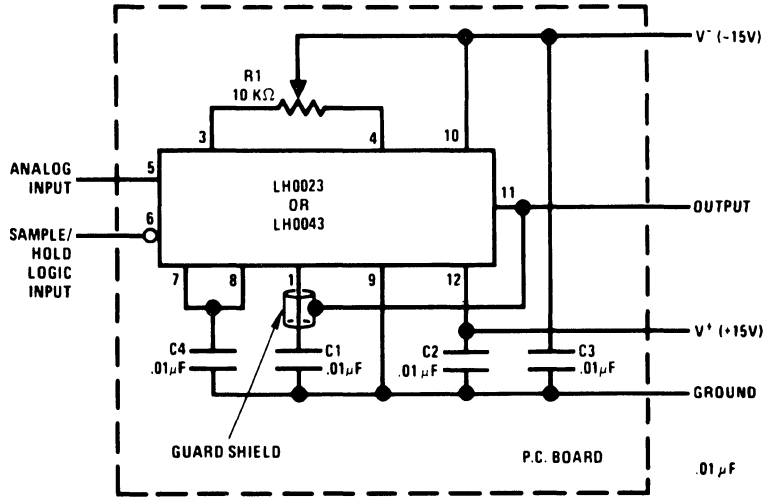
Typical Applications

How to Build a Sample and Hold Module



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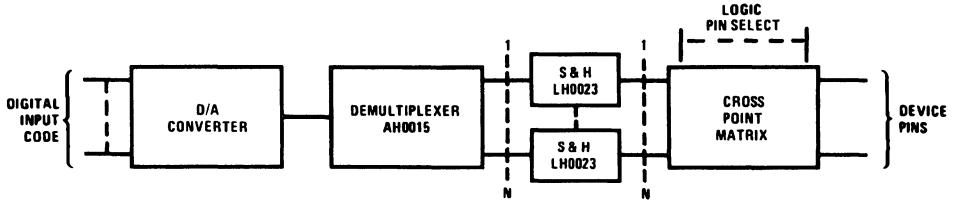
Note 1: C1 is polystyrene.

Note 2: C2, C3, C4 are ceramic disc.

Note 3: Jumper 7-8 and C4 not required for LH0043.

Note 4: R1 optional if zero trim is required.

Forcing Function Setup for Automatic: Test Gear



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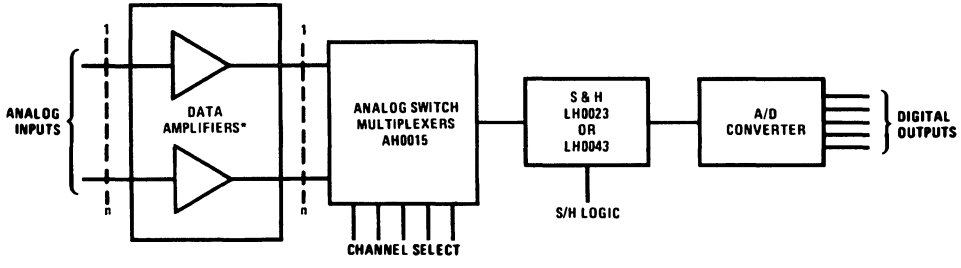
Data Acquisition System



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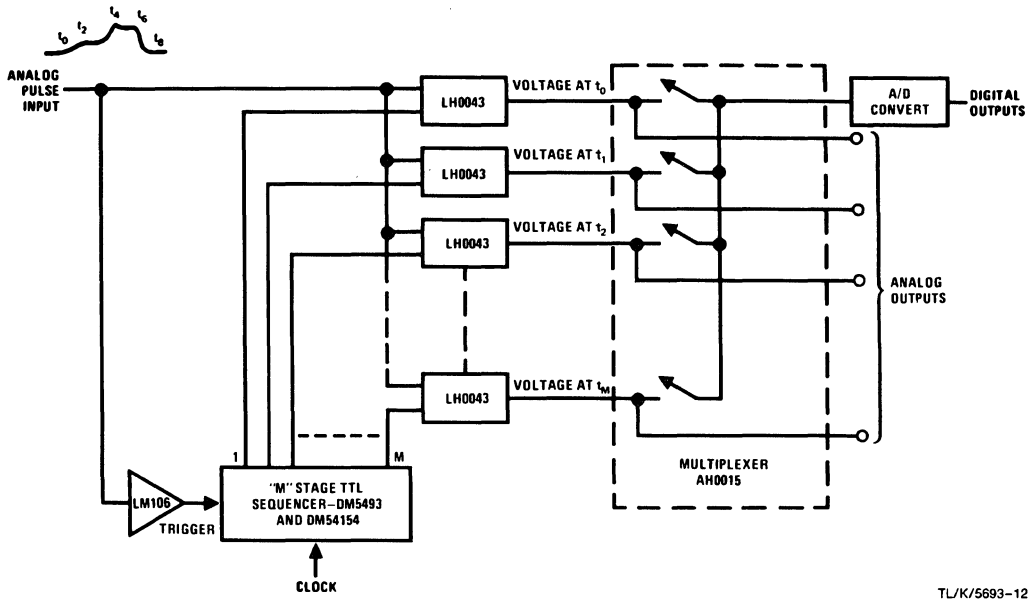
*See op amp selection guide for details. Most popular types include LH0052, LM108, LM112, LH0044, LH0036, and LH0038.

Typical Applications (Continued)

Single Pulse Sampler



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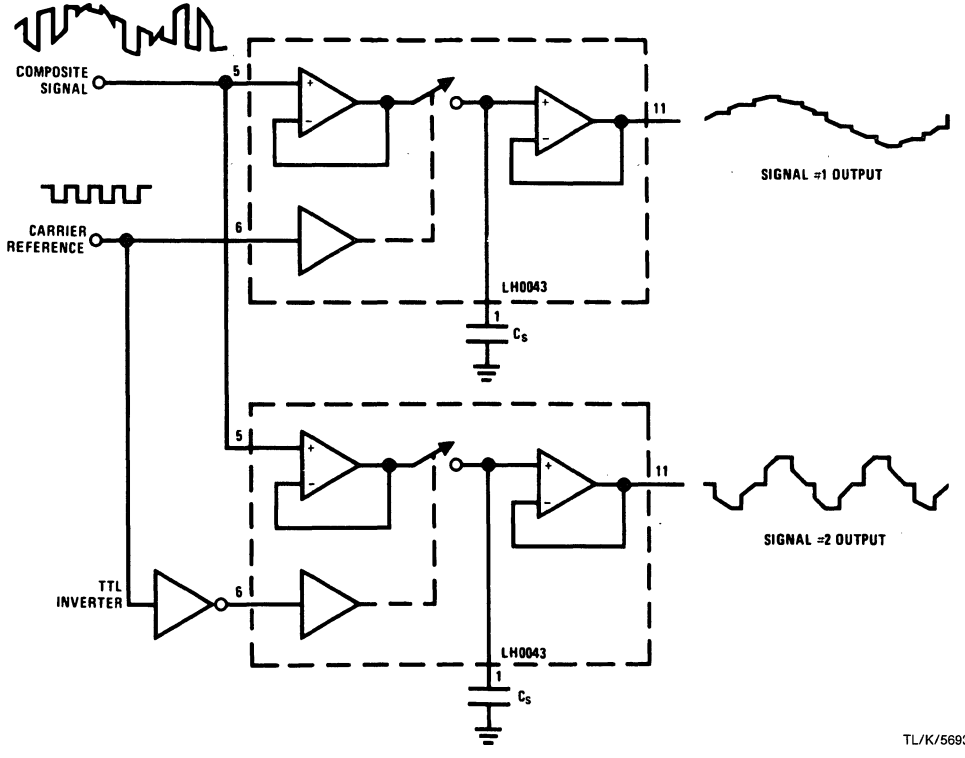
Two Channel Double Sideband Demodulator



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Applications Information

1.0 DRIFT ERROR MINIMIZATION

In order to minimize drift error, care in selection of C_S and layout of the printed circuit board is required. The capacitor should be of high quality Teflon, polycarbonate, or polystyrene construction. Board cleaniness and layout are critical particularly at elevated temperatures. See AN-63 for detailed recommendations. A guard conductor connected to the output surrounding the storage node (pin 1) will be helpful in meeting severe environmental conditions which would otherwise cause leakage across the printed circuit board.

2.0 CAPACITOR SELECTION

The size of the capacitor is dictated by the required drift rate and acquisition time. The drift is determined by the leakage current at pin 1 and may be calculated by $\frac{dV}{dt} = \frac{I_L}{C_S}$, where I_L is the total leakage current at pin 1 of the device, and C_S is the value of the storage capacitor.

2.1 Capacitor Selection – LH0023

At room temperature leakage current for the LH0023 is approximately 100 pA. A drift rate of 10 mV/sec would require a 0.01 μF capacitor.

For values of C_S up to 0.01 μF the acquisition time is limited by the slew rate of the input buffer amplifier, A1, typically 0.5 V/μs. Beyond this point, current availability to charge C_S also enters the picture. The acquisition time is given by:

$$t_A \cong \sqrt{\frac{2\Delta e_O RC_S}{0.5 \times 10^6}} = 2 \times 10^{-3}\sqrt{\Delta e_o RC_S}$$

where: R = the internal resistance in series with C_S

Δe_o = change in voltage sampled

An average value for R is approximately 600 ohms. The expression for t_A reduces to:

$$t_A \cong \frac{\sqrt{\Delta e_o C_S}}{20}$$

For a −10V to +10V change and C_S = .05 μF, acquisition time is typically 50 μs.

2.2 Capacitor Selection–LH0043

At 25°C case temperature, the leakage current for the LH0043G is approximately 10 pA, so a drift rate of 5 mV/s would require a capacitor of $C_S = 10 \bullet 10^{12}/5 \bullet 10^3 = 2000$ pF or larger.

For values of C_S below about 5000 pF, the acquisition time of the LH0043G will be limited by the slew rate of the output amplifier (the signal will be acquired, in the sense that the voltage will be stored on the capacitor, in much less time as dictated by the slew rate and current capacity of the input amplifier, but it will not be available at the output). For larger values of storage capacitance, the limitation is the current sinking capability of the input amplifier, typically 10 mA. With C_S = 0.01 μF, the slew rate can be estimated by

$$\frac{dV}{dt} = \frac{10 \bullet 10^{-3}}{0.01 \bullet 10^{-6}} = 1\text{V}/\mu\text{s}$$ or a slewing time for a 5 volt signal change of 5μs.

3.0 OFFSET NULL

Provision is made to null both the LH0023 and LH0043 by use of a 10k pot between pins 3 and 4. Offset null should be accomplished in the sample mode at one half the input voltage range for minimum average error.

4.0 SWITCHING SPIKE MINIMIZATION–LH0043

A capacitive divider is formed by the storage capacitor and the capacitance of the internal FET switch which causes a small error current to be injected into the storage capacitor at the termination of the sample interval. This can be considered a negative DC offset and nulled out as described in (3.0), or the transient may be nulled by coupling an equal but opposite signal to the storage capacitor. This may be accomplished by connecting a capacitor of about 30 pF (or a trimmer) between the logic input (pin 6) and the storage capacitor (pin 1). Note that this capacitor must be chosen as carefully as the storage capacitor itself with respect to leakage. The LH0023 has switch spike minimization circuitry built into the device.

5.0 ELIMINATION OF THE 5V LOGIC SUPPLY – LH0023

The 5V logic supply may be eliminated by shorting pin 7 to pin 8 which connects a 10k dropping resistor between the +15V and V_C. Decoupling pin 8 to ground through 0.1 μF disc capacitor is recommended in order to minimize transients in the output.

6.0 HEAT SINKING

The LH0023 and LH0043G may be operated without damage throughout the military temperature range of −55 to +125°C (−25 to +85°C for the LH0023CG and LH0043CG) with no explicit heat sink, however power dissipation will cause the internal temperature to rise above ambient. A simple clip-on heat sink such as Wakefield #215−1.9 or equivalent will reduce the internal temperature about 20°C thereby cutting the leakage current and drift rate by one fourth at max. ambient. There is no internal electrical connection to the case, so it may be mounted directly to a grounded heat sink.

7.0 THEORY OF OPERATION–LH0023

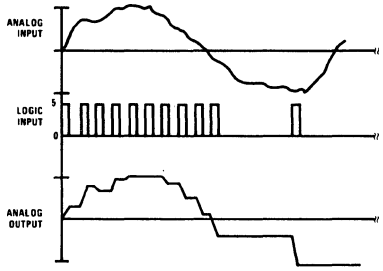
The LH0023/LH0023C is comprised of input buffer amplifier, A1, analog switches, S1 and S2, a TTL to MOS level

Applications Information (Continued)

translator, and output buffer amplifier, A2. In the "sample" mode, the logic input is raised to logic "1" ($V_6 \leq 2.0V$) which closes S1 and opens S2. Storage capacitor, C_S, is charged to the input voltage through S1 and the output slews to the input voltage. In the "hold" mode, the logic input is lowered to logic "0" ($V_6 \leq 0.8V$) opening S1 and closing S2. C_S retains the sample voltage which is applied to the output via A2. Since S1 is open, the input signal is overriden, and leakage across the MOS switch is therefore minimized. With S1 open, drift is primarily determined by input bias current of A2, typically 100 pA at 25°C.

7.1 Theory of Operation–LH0043

The LH0043/LH0043C is comprised of input buffer amplifier A1, FET switch S1 operated by a TTL compatible level translator, and output buffer amplifier A2. To enter the "sample" mode, the logic input is taken to the TTL logic "0" state ($V_6 = 0.8V$) which commands the switch S1 closed and allows A1 to make the storage capacitor voltage equal to the analog input voltage. in the "hold" mode ($V_6 = 2.0V$), S1 is opened isolating the storage capacitor from the input and leaving it charged to a voltage equal to the last analog input voltage before entering the hold mode. The storage capacitor voltage is brought to the output by low leakage amplifier A2.



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8.0 DEFINITIONS

V_5: The voltage at pin 5, e.g., the analog input voltage.

V_6: The voltage at pin 6, e.g., the logic control input signal.

V_{11}: The voltage at pin 11, e.g., the output signal.

T_A: The temperature of the ambient air.

T_C: The temperature of the device case at the center of the bottom of the header.

Acquisition Time:

The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to the input (pin 5) with the logic input (pin 6) in the low state.

Aperture Time:

The time indeterminacy when switching from sample mode to hold including the delay from the time the mode control signal (pin 6) passes through its threshold (1.4 volts) to the time the circuit actually enters the hold mode.

Output Offset Voltage:

The voltage at the output terminal (pin 11) with the analog input (pin 5) at ground and logic input (pin 6) in the "sample" mode. This will always be adjustable to zero using a 10k pot between pins 3 and 4 with the wiper arm returned to V^-.