PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LH28F160BJHE-TTLZE

Flash Memory

16M (1M × 16)

(Model No.: LHF16JZE)

Spec No.: EL135023

Issue Date: May 11, 2001

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●Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

LH28F160BJHE-TTLZE
16M-BIT (1Mbit ×16)
Boot Block Flash MEMORY

- Low Voltage Operation
  - $V_{CC}=V_{CCW}=2.7V\text{-}3.6V$ Single Voltage
- 16bit I/O Interface
- High-Performance Read Access Time
  - 90ns($V_{CC}=2.7V\text{-}3.6V$)
- Operating Temperature
  - -40°C to +85°C
- Low Power Management
  - Typ. 2µA ($V_{CC}=3.0V$) Standby Current
  - Automatic Power Savings Mode Decreases I_{CCR} in Static Mode
  - Typ. 120µA ($V_{CC}=3.0V$, $T_A=+25°C$, f=32kHz) Read Current
- Optimized Array Blocking Architecture
  - Two 4K-word Boot Blocks
  - Six 4K-word Parameter Blocks
  - Thirty-one 32K-word Main Blocks
  - Top Boot Location
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
  - Word Write Suspend to Read
  - Block Erase Suspend to Word Write
  - Block Erase Suspend to Read
- Enhanced Data Protection Features
  - Absolute Protection with $V_{CCW} \leq V_{CCWLK}$
  - Block Erase, Full Chip Erase, Word Write and Lock-Bit Configuration Lockout during Power Transitions
  - Block Locking with Command and WP#
  - Permanent Locking
- Automated Block Erase, Full Chip Erase, Word Write and Lock-Bit Configuration
  - Command User Interface (CUI)
  - Status Register (SR)
- SRAM-Compatible Write Interface
- Industry-Standard Packaging
  - 48-Lead TSOP
- ETOX^{TM*} Nonvolatile Flash Technology
- CMOS Process (P-type silicon substrate)
- Not designed or rated as radiation hardened

SHARP’s LH28F160BJHE-TTLZE Flash memory is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications.

LH28F160BJHE-TTLZE can operate at $V_{CC}=2.7V\text{-}3.6V$ and $V_{CCW}=2.7V\text{-}3.6V$ or 11.7V-12.3V. Its low voltage operation capability realizes long battery life and suits for cellular phone application.

Its Boot, Parameter and Main-blocked architecture, low voltage and extended cycling provide for highly flexible component suitable for portable terminals and personal computers. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications.

For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F160BJHE-TTLZE offers four levels of protection: absolute protection with $V_{CCW} \leq V_{CCWLK}$, selective hardware block locking or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F160BJHE-TTLZE is manufactured on SHARP’s 0.25µm ETOX^{TM*} process technology. It come in industry-standard package: the 48-lead TSOP, ideal for board constrained applications.

*ETOX is a trademark of Intel Corporation.

1 INTRODUCTION

This datasheet contains LH28F160BJHE-TTLZE specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4 and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 Features

Key enhancements of LH28F160BJHE-TTLZE boot block Flash memory are:

- Single low voltage operation
- Low power consumption
- Enhanced Suspend Capabilities
- Boot Block Architecture

Please note following:

- V_{CCWLK} has been lowered to 1.0V to support 2.7V-3.6V block erase, full chip erase, word write and lock-bit configuration operations. The V_{CCW} voltage transitions to GND is recommended for designs that switch V_{CCW} off during read operation.

1.2 Product Overview

The LH28F160BJHE-TTLZE is a high-performance 16M-bit Boot Block Flash memory organized as 1M-word of 16 bits. The 1M-word of data is arranged in two 4K-word boot blocks, six 4K-word parameter blocks and thirty-one 32K-word main blocks which are individually erasable, lockable and unlockable in-system. The memory map is shown in Figure 3.

The dedicated V_{CCW} pin gives complete data protection when $V_{CCW} \leq V_{CCWLK}$.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, word write and lock-bit configuration operations.

A block erase operation erases one of the device’s 32K-word blocks typically within 1.2s (3V V_{CC}, 3V V_{CCW}), 4K-word blocks typically within 0.6s (3V V_{CC}, 3V V_{CCW}) independent of other blocks. Each block can be independently erased minimum 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word increments of the device’s 32K-word blocks typically within 33µs (3V V_{CC}, 3V V_{CCW}), 4K-word blocks typically within 36µs (3V V_{CC}, 3V V_{CCW}). Word write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits, thirty-nine block lock-bits, a permanent lock-bit and WP# pin, to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and word write operations, while the permanent lock-bit gates block lock-bit modification and locked block alternation. Lock-bit configuration operations (Set Block Lock-Bit, Set Permanent Lock-Bit and Clear Block Lock-Bits commands) set and cleared lock-bits.

The status register indicates when the WSM’s block erase, full chip erase, word write or lock-bit configuration operation is finished.

The access time is 90ns (t_{AVQV}) over the operating temperature range (-40°C to +85°C) and V_{CC} supply voltage range of 2.7V-3.6V.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 2µA (CMOS) at 3.0V V_{CC}.

When CE# and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the RP# pin is at GND, reset mode is enabled which minimizes power consumption and provides write protection. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

Please do not execute reprogramming "0" for the bit which has already been programed "0". Overwrite operation may generate unerasable bit. In case of reprogramming "0" to the data which has been programed "1".

- ·Program "0" for the bit in which you want to change data from "1" to "0".
- ·Program "1" for the bit which has already been programmed "0".

For example, changing data from "1011110110111101" to "1010110110111100" requires "1110111111111110" programming.

1.3 Product Description

1.3.1 Package Pinout

LH28F160BJHE-TTLZE Boot Block Flash memory is available in 48-lead TSOP package (see Figure 2).

1.3.2 Block Organization

This product features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100,000 times. For the address locations of the blocks, see the memory map in Figure 3.

Boot Blocks: The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. This boot block 4K words (4,096words) features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental modification. The protection of the boot block is controlled using a combination of the V_{CCW}, RP#, WP# pins and block lock-bit.

Parameter Blocks: The boot block architecture includes parameter blocks to facilitate storage of frequently update small parameters that would normally require an EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. Each boot block component contains six parameter blocks of 4K words (4,096 words) each. The protection of the parameter block is controlled using a combination of the V_{CCW}, RP# and block lock-bit.

Main Blocks: The reminder is divided into main blocks for data or code storage. Each 16M-bit device contains thirty-one 32K words (32,768 words) blocks. The protection of the main block is controlled using a combination of the V_{CCW}, RP# and block lock-bit.

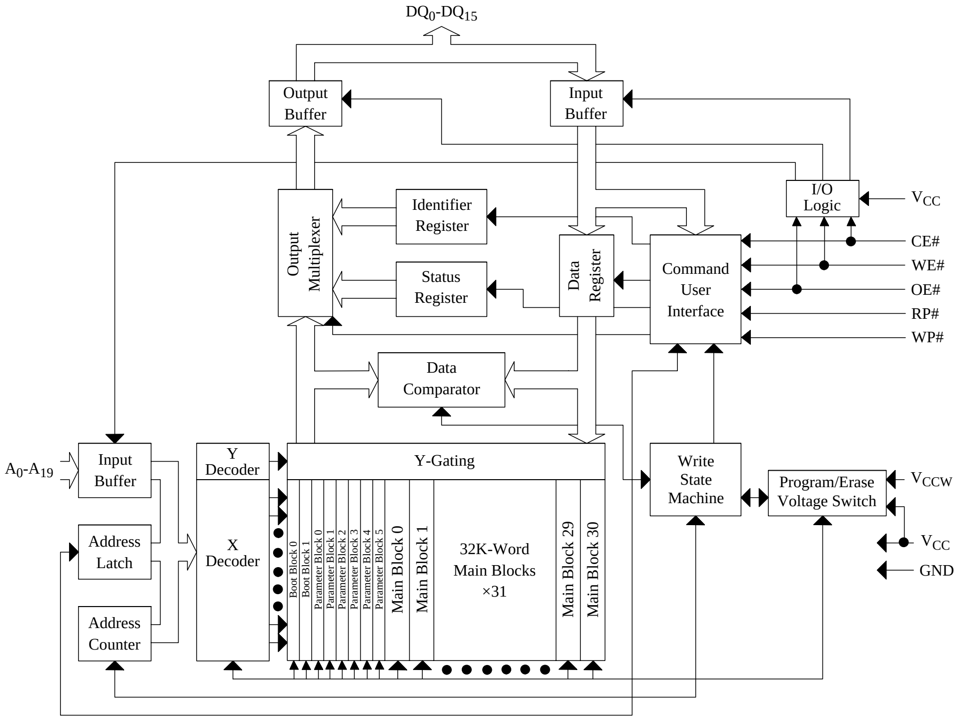


Figure 1. Block Diagram

Figure 2. TSOP 48-Lead Pinou

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A_0-A_{19}	INPUT	ADDRESS INPUTS: Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. A_{15}-A_{19}: Main Block Address. A_{12}-A_{19}: Boot and Parameter Block Address.
DQ_0-DQ_{15}	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	CHIP ENABLE: Activates the device’s control logic, input buffers, decoders and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	RESET: Resets the device internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from reset mode sets the device to read array mode. RP# must be V_{IL} during power-up.
OE#	INPUT	OUTPUT ENABLE: Gates the device’s outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	WRITE PROTECT: When WP# is V_{IL}, boot blocks cannot be written or erased. When WP# is V_{IH}, locked boot blocks can not be written or erased. WP# is not affected parameter and main blocks.
V_{CCW}	SUPPLY	BLOCK ERASE, FULL CHIP ERASE, WORD WRITE OR LOCK-BIT CONFIGURATION POWER SUPPLY: For erasing array blocks, writing words or configuring lock-bits. With $V_{CCW} \leq V_{CCWLK}$, memory contents cannot be altered. Block erase, full chip erase, word write and lock-bit configuration with an invalid V_{CCW} (see 6.2.3 DC Characteristics) produce spurious results and should not be attempted. Applying 12V±0.3V to V_{CCW} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{CCW} may be connected to 12V±0.3V for a total of 80 hours maximum.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY: Do not float any power pins. With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see 6.2.3 DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internal connected; it may be driven or floated.

2 PRINCIPLES OF OPERATION

The LH28F160BJHE-TTLZE flash memory includes an on-chip WSM to manage block erase, full chip erase, word write and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erase, full chip erase, word write and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from reset mode (see section 3 Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{CCW} voltage. High voltage on V_{CCW} enables successful block erase, full chip erase, word write and lock-bit configurations. All functions associated with altering memory contents−block erase, full chip erase, word write, lock-bit configuration, status and identifier codes−are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, word write and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, word write and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspend. Word write suspend allows system software to suspend a word write to read data from any other flash memory array location.

[A_{19}-A_0]		Top Boot	
FFFFF	FF000	4K-word Boot Block	0
FEFFF	FE000	4K-word Boot Block	1
FDFFF	FD000	4K-word Parameter Block	0
FCFFF	FC000	4K-word Parameter Block	1
FBFFF	FB000	4K-word Parameter Block	2
FAFFF	FA000	4K-word Parameter Block	3
F9FFF	F9000	4K-word Parameter Block	4
F8FFF	F8000	4K-word Parameter Block	5
F7FFF	F0000	32K-word Main Block	0
EFFFF	E8000	32K-word Main Block	1
E7FFF	E0000	32K-word Main Block	2
DFFFF	D8000	32K-word Main Block	3
D7FFF	D0000	32K-word Main Block	4
CFFFF	C8000	32K-word Main Block	5
C7FFF	C0000	32K-word Main Block	6
BFFFF	B8000	32K-word Main Block	7
B7FFF	B0000	32K-word Main Block	8
AFFFF	A8000	32K-word Main Block	9
A7FFF	A0000	32K-word Main Block	10
9FFFF	98000	32K-word Main Block	11
97FFF	90000	32K-word Main Block	12
8FFFF	88000	32K-word Main Block	13
87FFF	80000	32K-word Main Block	14
7FFFF	78000	32K-word Main Block	15
77FFF	70000	32K-word Main Block	16
6FFFF	68000	32K-word Main Block	17
67FFF	60000	32K-word Main Block	18
5FFFF	58000	32K-word Main Block	19
57FFF	50000	32K-word Main Block	20
4FFFF	48000	32K-word Main Block	21
47FFF	40000	32K-word Main Block	22
3FFFF	38000	32K-word Main Block	23
37FFF	30000	32K-word Main Block	24
2FFFF	28000	32K-word Main Block	25
27FFF	20000	32K-word Main Block	26
1FFFF	18000	32K-word Main Block	27
17FFF	10000	32K-word Main Block	28
0FFFF	08000	32K-word Main Block	29
07FFF	00000	32K-word Main Block	30

Figure 3. Memory Map

2.1 Data Protection

When $V_{CCW} \leq V_{CCWLK}$, memory contents cannot be altered. The CUI, with two-step block erase, full chip erase, word write or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{CCW}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and word write operations. Refer to Table 5 for write protection alternatives.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes or status register independent of the V_{CCW} voltage. RP# can be at V_{IH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from reset mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component: CE#, OE#, WE#, RP# and WP#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and when active drives the selected memory data onto the I/O bus. WE# must be at V_{IH}, RP# must be at V_{IH}, and WP# must be at V_{IL} or V_{IH}. Figure 14 illustrates read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ_0-DQ_{15}) are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0-DQ_{15} outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, full chip erase, word write or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Reset

RP# at V_{IL} initiates the reset mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100ns. Time t_{PHQV} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, full chip erase, word write or lock-bit configuration modes, RP#-low will abort the operation. SR.7 remains "0" until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, word write or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block and the permanent lock configuration code (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and permanent lock configuration codes identify locked and unlocked blocks and permanent lock-bit setting.

3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When V_{CC}=2.7V-3.6V and V_{CCW}=$V_{CCWH1/2}$, the CUI additionally controls block erase, full chip erase, word write and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Full Chip Erase command requires appropriate command data and an address within the device. The Word Write command requires the command and address of the location to be written. Set Permanent and Block Lock-Bit commands require the command and address within the device (Permanent Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 15 and 16 illustrate WE# and CE# controlled write operations.

4 COMMAND DEFINITIONS

When the V_{CCW} voltage $\leq V_{CCWLK}$, read operations from the status register, identifier codes, or blocks are enabled. Placing $V_{CCWH1/2}$ on V_{CCW} enables successful block erase, full chip erase, word write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 3 defines these commands.

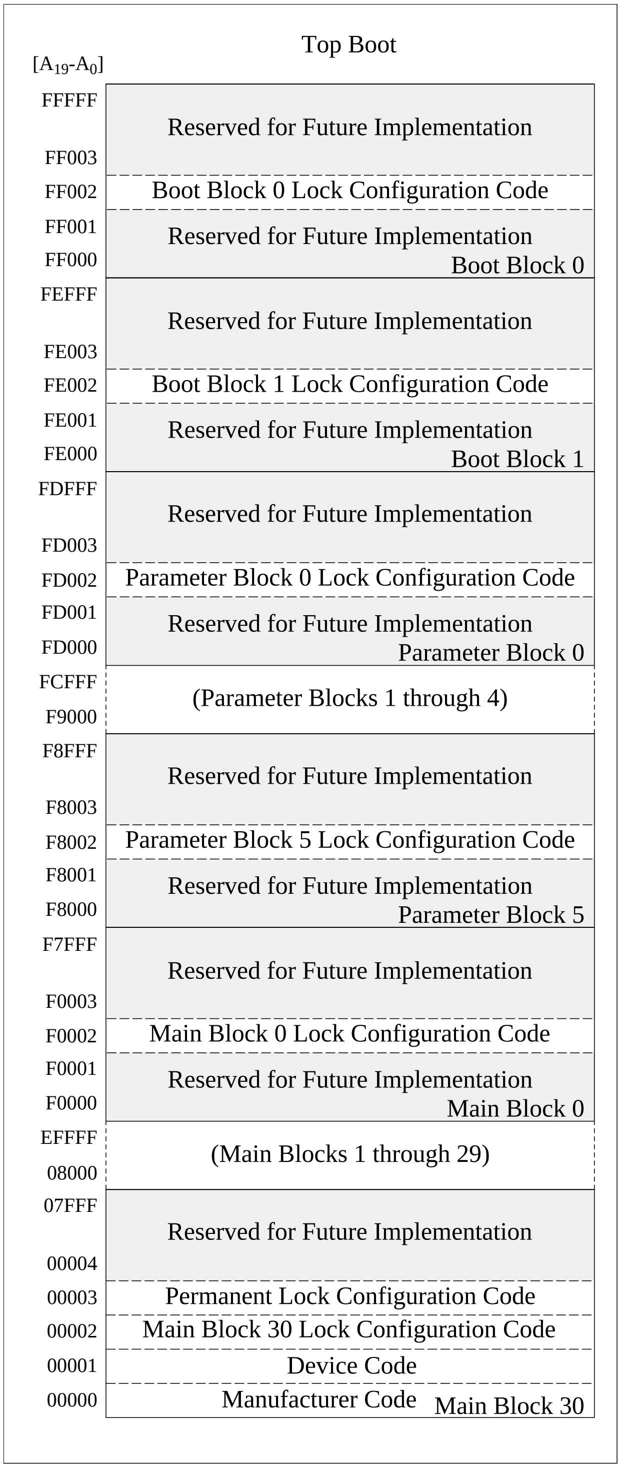


Figure 4. Device Identifier Code Memory Map

Table 2. Bus Operations(1,2)

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{CCW}	DQ_{0-15}
Read	7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	High Z
Reset	3	V_{IL}	X	X	X	X	X	High Z
Read Identifier Codes	7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4	X	Note 4
Write	5,6,7	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}

NOTES:

1. Refer to DC Characteristics. When $V_{CCW} \leq V_{CCWLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{CCWLK} or $V_{CCWH1/2}$ for V_{CCW}. See DC Characteristics for V_{CCWLK} voltages.
3. RP# at GND±0.2V ensures the lowest power consumption.
4. See Section 4.2 for read identifier code data.
5. Command writes involving block erase, full chip erase, word write or lock-bit configuration are reliably executed when $V_{CCW}=V_{CCWH1/2}$ and V_{CC}=2.7V-3.6V.
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. Never hold OE# low and WE# low at the same timing.

Table 3. Command Definitions(10)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	X	20H	Write	BA	D0H
Full Chip Erase	2		Write	X	30H	Write	X	D0H
Word Write	2	5,6	Write	X	40H or 10H	Write	WA	WD
Block Erase and Word Write Suspend	1	5	Write	X	B0H			
Block Erase and Word Write Resume	1	5	Write	X	D0H			
Set Block Lock-Bit	2	8	Write	X	60H	Write	BA	01H
Clear Block Lock-Bits	2	7,8	Write	X	60H	Write	X	D0H
Set Permanent Lock-Bit	2	9	Write	X	60H	Write	X	F1H

NOTES:

1. BUS operations are defined in Table 2.
2. X=Any valid address within the device.
   IA=Identifier Code Address: see Figure 4.
   BA=Address within the block being erased.
   WA=Address of memory location to be written.
3. SRD=Data read from status register. See Table 6 for a description of the status register bits.
   WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID=Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock configuration and permanent lock configuration codes. See Section 4.2 for read identifier code data.
5. If WP# is V_{IL}, boot blocks are locked without block lock-bits state. If WP# is V_{IH}, boot blocks are locked by block lock-bits. The parameter and main blocks are locked by block lock-bits without WP# state.
6. Either 40H or 10H are recognized by the WSM as the word write setup.
7. The clear block lock-bits operation simultaneously clears all block lock-bits.
8. If the permanent lock-bit is set, Set Block Lock-Bit and Clear Block Lock-Bits commands can not be done.
9. Once the permanent lock-bit is set, permanent lock-bit reset is unable.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from reset mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, full chip erase, word write or lock-bit configuration the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word Write Suspend command. The Read Array command functions independently of the V_{CCW} voltage and RP# can be V_{IH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer, device, block lock configuration and permanent lock configuration codes (see Table 4 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{CCW} voltage and RP# can be V_{IH}. Following the Read Identifier Codes command, the following information can be read:

Table 4. Identifier Codes

Code	Address [A_{19}-A_0]	Data [DQ_{15}-DQ_0]
Manufacture Code	00000H	00B0H
Device Code	00001H	00E8H
Block Lock Configuration	BA(1)+2	
•Block is Unlocked		DQ_0=0
•Block is Locked		DQ_0=1
•Reserved for Future Use		DQ_{1-15}
Permanent Lock Configuration	00003H	
•Device is Unlocked		DQ_0=0
•Device is Locked		DQ_0=1
•Reserved for Future Use		DQ_{1-15}

NOTE:

1. BA selects the specific block lock configuration code to be read. See Figure 4 for the device identifier code memory map.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, full chip erase, word write or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{CCW} voltage. RP# can be V_{IH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{CCW} Voltage. RP# can be V_{IH}. This command is not functional during block erase or word write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect block erase completion by analyzing the status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{CCW} \leq V_{CCWLK}$, SR.3 and SR.5 will be set to "1". Successful block erase requires for boot blocks that WP# is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If block erase is attempted when the excepting above conditions, SR.1 and SR.5 will be set to "1".

4.6 Full Chip Erase Command

This command followed by a confirm command erases all of the unlocked blocks. A full chip erase setup (30H) is first written, followed by a full chip erase confirm (D0H). After a confirm command is written, device erases the all unlocked blocks block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect full chip erase completion by analyzing the output data of the status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing. Full chip erase operation start from lower address block, finish the higher address block. Full chip erase can not be suspended.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable full chip erasure can only occur when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If full chip erase is attempted while $V_{CCW} \leq V_{CCWLK}$, SR.3 and SR.5 will be set to "1". Successful full chip erase requires for boot blocks that WP# is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If all blocks are locked, SR.1 and SR.5 will be set to "1".

4.7 Word Write Command

Word write is executed by a two-cycle command sequence. Word write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word write and write verify algorithms internally. After the word write sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect the completion of the word write event by analyzing the status register bit SR.7.

When word write is complete, status register bit SR.4 should be checked. If word write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word writes can only occur when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. In the absence of this high voltage, memory contents are protected against word writes. If word write is attempted while $V_{CCW} \leq V_{CCWLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word write requires for boot blocks that WP# is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If word write is attempted when the excepting above conditions, SR.1 and SR.4 will be set to "1".

4.8 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). Specification t_{WHR12} defines the block erase suspend latency.

When Block Erase Suspend command write to the CUI, if block erase was finished, the device places read array mode. Therefore, after Block Erase Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.6 should be checked for places the device in suspend mode.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word Write Suspend command (see Section 4.9), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0". However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 8). V_{CCW} must remain at $V_{CCWH1/2}$ (the same V_{CCW} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH}. WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for block erase). Block erase cannot resume until word write operations initiated during block erase suspend have completed.

If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than t_{ERES} and both commands are written repeatedly, a longer time is required than standard block erase until the completion of the operation.

4.9 Word Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the Word write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word write operation has been suspended (both will be set to "1"). Specification t_{WHR11} defines the word write suspend latency.

When Word Write Suspend command write to the CUI, if word write was finished, the device places read array mode. Therefore, after Word Write Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.2 should be checked for places the device in suspend mode.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After Word Write Resume command is written to the flash memory, the WSM will continue the word write process. Status register bits SR.2 and SR.7 will automatically clear. After the Word Write Resume command is written, the device automatically outputs status register data when read (see Figure 9). V_{CCW} must remain at $V_{CCWH1/2}$ (the same V_{CCW} level used for word write) while in word write suspend mode. RP# must also remain at V_{IH}. WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for word write).

If the time between writing the Word Write Resume command and writing the Word Write Suspend command is short and both commands are written repeatedly, a longer time is required than standard word write until the completion of the operation.

4.10 Set Block and Permanent Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits, a permanent lock-bit and WP# pin. The block lock-bits and WP# pin gates program and erase operations while the permanent lock-bit gates block-lock bit modification. With the permanent lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Permanent Lock-Bit command, sets the permanent lock-bit. After the permanent lock-bit is set, block lock-bits and locked block contents cannot altered. See Table 5 for a summary of hardware and software write protection options.

Set block lock-bit and permanent lock-bit are executed by a two-cycle command sequence. The set block or permanent lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set permanent lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 10). The CPU can detect the completion of the set lock-bit event by analyzing the status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Permanent Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the permanent lock-bit be cleared. If it is attempted with the permanent lock-bit set, SR.1 and SR.4 will be set to "1" and the operation will fail.

4.11 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the permanent lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the permanent lock-bit is set, block lock-bits cannot cleared. See Table 5 for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 11). The CPU can detect completion of the clear block lock-bits event by analyzing the status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when V_{CC}=2.7V-3.6V and $V_{CCW}=V_{CCWH1/2}$. If a clear block lock-bits operation is attempted while $V_{CCW} \leq V_{CCWLK}$, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the permanent lock-bit is not set. If it is attempted with the permanent lock-bit set, SR.1 and SR.5 will be set to "1" and the operation will fail.

If a clear block lock-bits operation is aborted due to V_{CCW} or V_{CC} transitioning out of valid range or RP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the permanent lock-bit is set, it cannot be cleared.

4.12 Block Locking by the WP#

This Boot Block Flash memory architecture features two hardware-lockable boot blocks so that the kernel code for the system can be kept secure while other blocks are programmed or erased as necessary.

The lockable two boot blocks are locked when WP#=V_{IL}; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two boot blocks are lockable. For the bottom configuration, the bottom two boot blocks are lockable. If WP# is V_{IH} and block lock-bit is not set, boot block can be programmed or erased normally (Unless V_{CCW} is below V_{CCWLK}). WP# is valid only two boot blocks, other blocks are not affected.

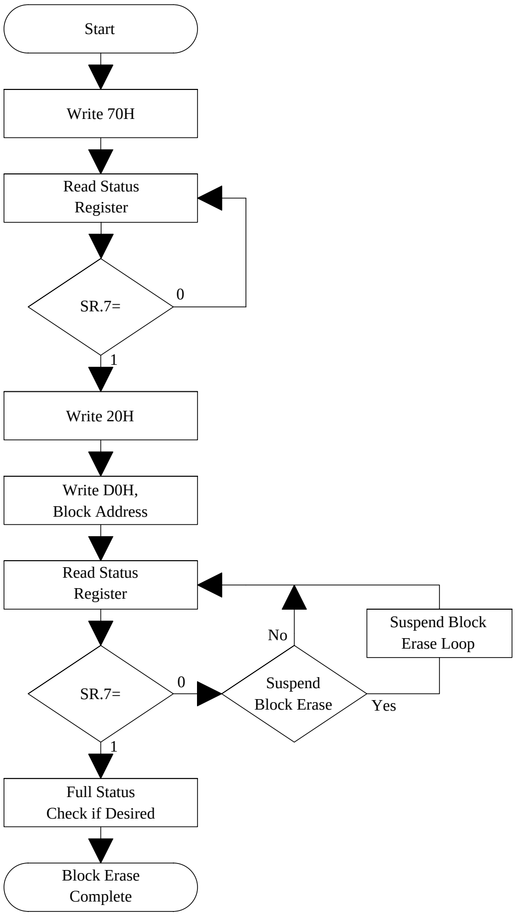
Table 5. Write Protection Alternatives

Operation	V_{CCW}	RP#	Permanent Lock-Bit	Block Lock-bit	WP#	Effect
Block Erase or Word Write	$\leq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	0	V_{IL}	2 Boot Blocks Locked.
					V_{IH}	Block Erase and Word Write Enabled.
				1	V_{IL}	Block Erase and Word Write Disabled.
					V_{IH}	Block Erase and Word Write Disabled.
Full Chip Erase	$\leq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	X	V_{IL}	All Unlocked Blocks are Erased. 2 Boot Blocks and Locked Blocks are NOT Erased.
					V_{IH}	All Unlocked Blocks are Erased, Locked Blocks are NOT Erased.
Set Block Lock-Bit	$\leq V_{CCWLK}$	X	X	X	X	Set Block Lock-Bit Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Set Block Lock-Bit Disabled.
		V_{IH}	0	X	X	Set Block Lock-Bit Enabled.
			1	X	X	Set Block Lock-Bit Disabled.
Clear Block Lock-Bits	$\leq V_{CCWLK}$	X	X	X	X	Clear Block Lock-Bits Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Clear Block Lock-Bits Disabled.
		V_{IH}	0	X	X	Clear Block Lock-Bits Enabled.
			1	X	X	Clear Block Lock-Bits Disabled.
Set Permanent Lock-Bit	$\leq V_{CCWLK}$	X	X	X	X	Set Permanent Lock-Bit Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Set Permanent Lock-Bit Disabled.
		V_{IH}	X	X	X	Set Permanent Lock-Bit Enabled.

Table 6. Status Register Definition

WSMS	BESS	ECBLBS	WWSLBS	VCCWS	WWSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check SR.7 to determine block erase, full chip erase, word write or lock-bit configuration completion. SR.6-0 are invalid while SR.7="0".
SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS (ECBLBS) 1 = Error in Block Erase, Full Chip Erase or Clear Block Lock-Bits 0 = Successful Block Erase, Full Chip Erase or Clear Block Lock-Bits	If both SR.5 and SR.4 are "1"s after a block erase, full chip erase or lock-bit configuration attempt, an improper command sequence was entered.
SR.4 = WORD WRITE AND SET LOCK-BIT STATUS (WWSLBS) 1 = Error in Word Write or Set Block/Permanent Lock-Bit 0 = Successful Word Write or Set Block/Permanent Lock-Bit	
SR.3 = V_{CCW} STATUS (VCCWS) 1 = V_{CCW} Low Detect, Operation Abort 0 = V_{CCW} OK	SR.3 does not provide a continuous indication of V_{CCW} level. The WSM interrogates and indicates the V_{CCW} level only after Block Erase, Full Chip Erase, Word Write or Lock-Bit Configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{CCW} \neq V_{CCWH1/2}$.
SR.2 = WORD WRITE SUSPEND STATUS (WWSS) 1 = Word Write Suspended 0 = Word Write in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Block Lock-Bit, Permanent Lock-Bit and/or WP# Lock Detected, Operation Abort 0 = Unlock	SR.1 does not provide a continuous indication of permanent and block lock-bit and WP# values. The WSM interrogates the permanent lock-bit, block lock-bit and WP# only after Block Erase, Full Chip Erase, Word Write or Lock-Bit Configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set and/or WP# is V_{IL}. Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.



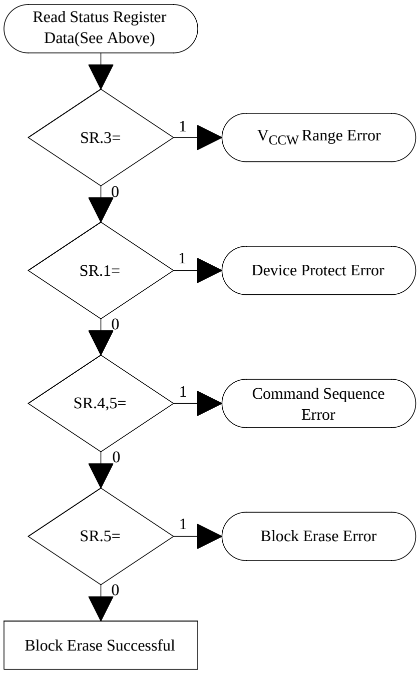
Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Erase Setup	Data=20H Addr=X
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block erasures.

Full status check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

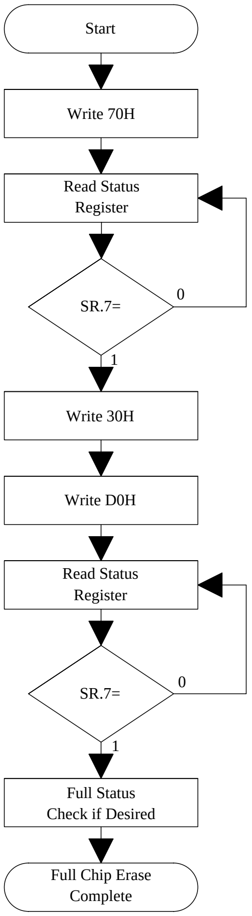


Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 5. Automated Block Erase Flowchart

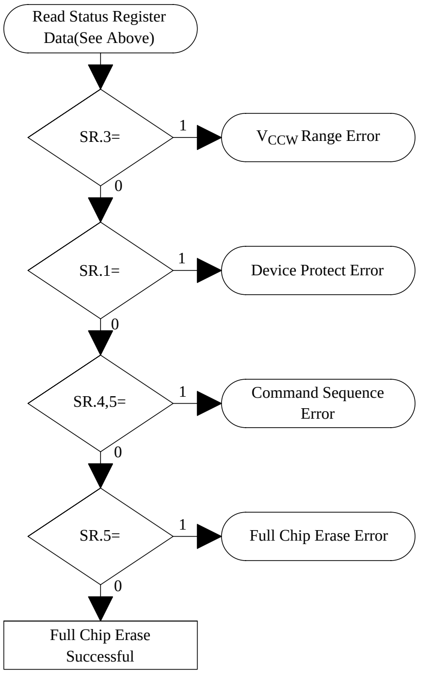


Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Full Chip Erase Setup	Data=30H Addr=X
Write	Full Chip Erase Confirm	Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Full status check can be done after each full chip erase.

Write FFH after the last operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

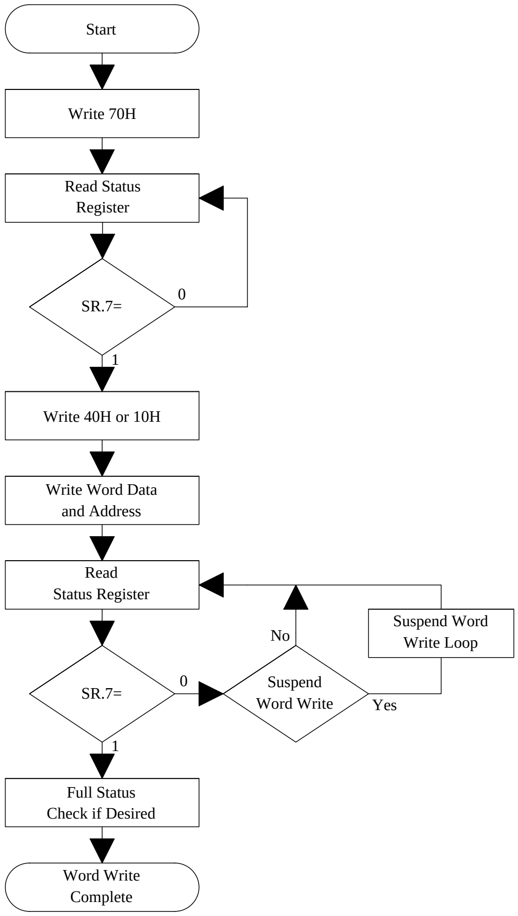


Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect (All Blocks are locked)
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Full Chip Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

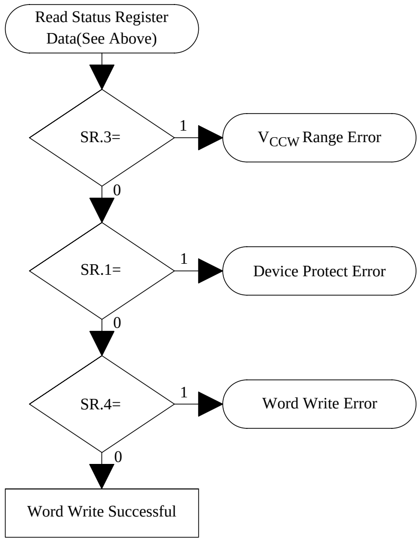
Figure 6. Automated Full Chip Erase Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Setup Word Write	Data=40H or 10H Addr=X
Write	Word Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent word writes.
SR full status check can be done after each word write, or after a sequence of word writes.
Write FFH after the last word write operation to place device in read array mode.

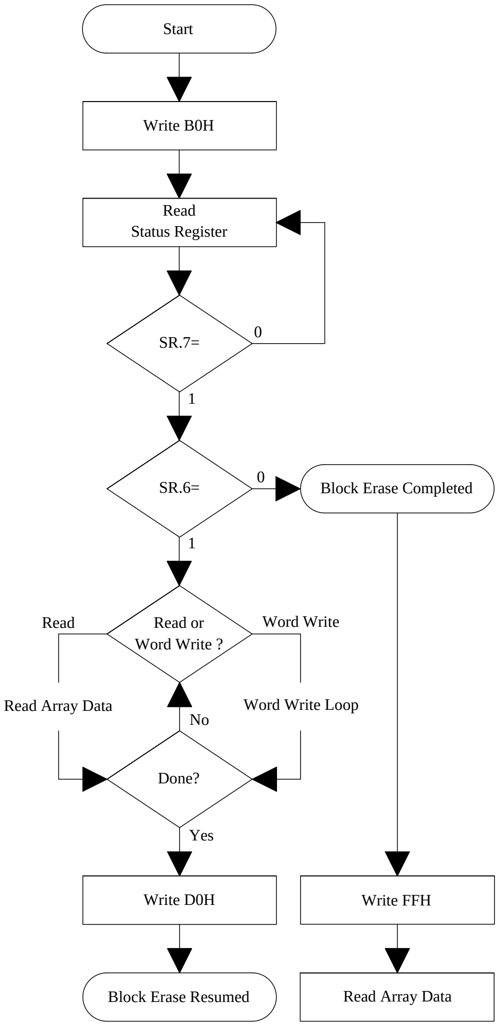
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=Data Write Error

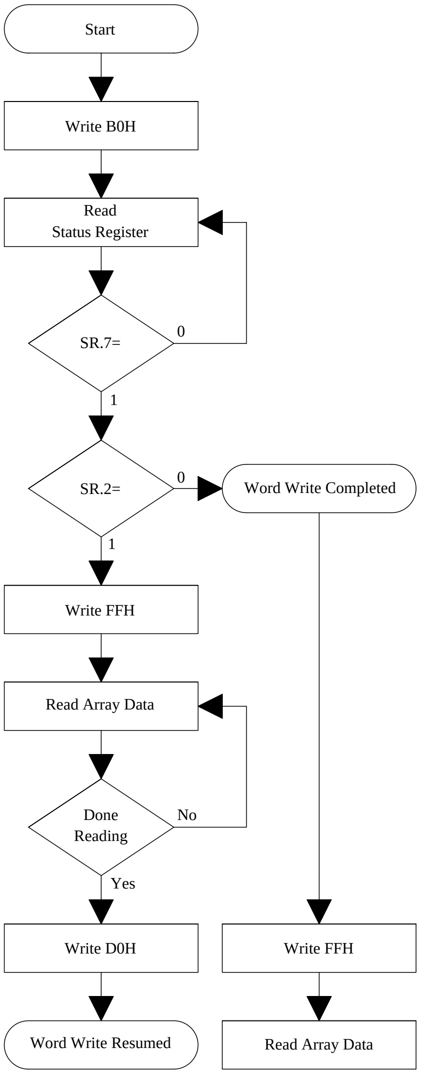
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 7. Automated Word Write Flowchart



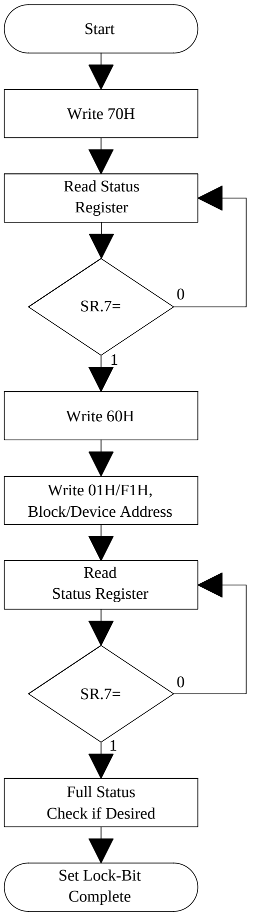
Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Figure 8. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Word Write Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Word Write Suspended 0=Word Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	Word Write Resume	Data=D0H Addr=X

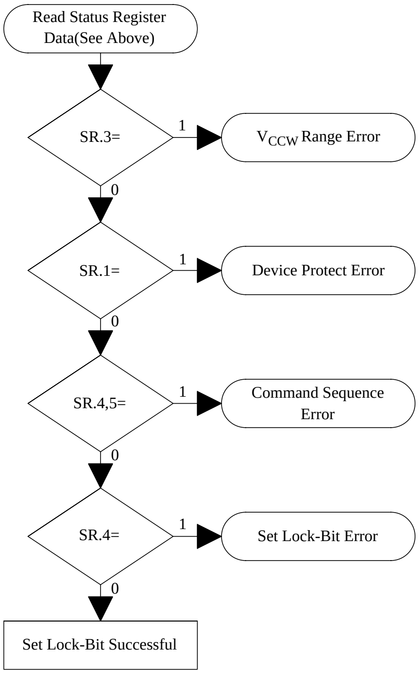
Figure 9. Word Write Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Set Block/Permanent Lock-Bit Setup	Data=60H Addr=X
Write	Set Block or Permanent Lock-Bit Confirm	Data=01H(Block), F1H(Permanent) Addr=Block Address(Block), Device Address(Permanent)
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent lock-bit set operations.
Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations.
Write FFH after the last lock-bit set operation to place device in read array mode.

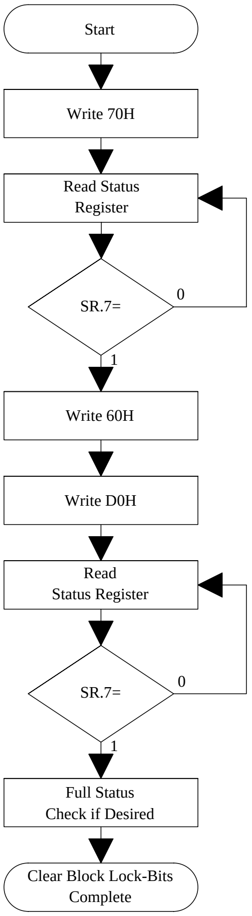
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect Permanent Lock-Bit is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.4 1=Set Lock-Bit Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

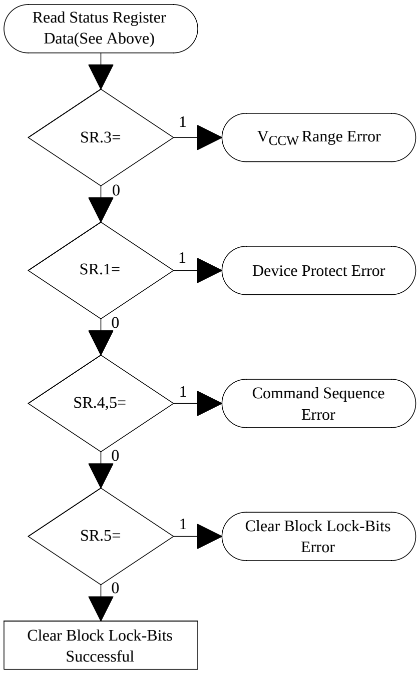
Figure 10. Set Block and Permanent Lock-Bit Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Clear Block Lock-Bits Setup	Data=60H Addr=X
Write	Clear Block Lock-Bits Confirm	Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect Permanent Lock-Bit is Set
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Clear Block Lock-Bits Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 11. Clear Block Lock-Bits Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a. Lowest possible memory power dissipation.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1µF ceramic capacitor connected between its V_{CC} and GND and between its V_{CCW} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.3 V_{CCW} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{CCW} Power supply trace. The V_{CCW} pin supplies the memory cell current for word writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{CCW} supply traces and decoupling will decrease V_{CCW} voltage spikes and overshoots.

5.4 V_{CC}, V_{CCW}, RP# Transitions

Block erase, full chip erase, word write and lock-bit configuration are not guaranteed if V_{CCW} falls outside of a valid $V_{CCWH1/2}$ range, V_{CC} falls outside of a valid 2.7V-3.6V range, or RP#$\neq V_{IH}$. If V_{CCW} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to V_{IL} during block erase, full chip erase, word write or lock-bit configuration, SR.7 will remain "0" until the reset operation is complete. Then, the operation will abort and the device will enter reset mode. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{CCW} or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from reset mode or after V_{CC} transitions below V_{LKO}.

5.5 Power-Up/Down Protection

The device is designed to offer protection against accidental block erase, full chip erase, word write or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{CCW} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{CCW} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while RP#=V_{IL} regardless of its control inputs state.

5.6 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

5.7 Data Protection Method

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto WE# signal or power supply, may be interpreted as false commands, causing undesired memory updating. To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block

When a lock bit is set, the corresponding block (includes the 2 boot blocks) is protected against overwriting. By setting a WP# to low, only the 2 boot blocks can be protected against overwriting. By using this feature, the flash memory space can be divided into the program section (locked section) and data section (unlocked section). The permanent lock bit can be used to prevent false block bit setting. For further information on setting/resetting lock-bit, refer to the specification. (See chapter 4.10 and 4.11.)

2) Data protection through V_{CCW}

When the level of V_{CCW} is lower than V_{CCWLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected. For the lockout voltage, refer to the specification. (See chapter 6.2.3.)

3) Data protection through RP#

When the RP# is kept low during read mode, the flash memory will be reset mode, then write protecting all blocks. When the RP# is kept low during power up and power down sequence such as voltage transition, write operation on the flash memory is disabled, write protecting all blocks. For the details of RP# control, refer to the specification. (See chapter 5.5 and 6.2.7.)

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Operating Temperature
During Read, Block Erase,
Full Chip Erase, Word Write
and Lock-Bit Configuration ....-40°C to +85°C(1)

Storage Temperature
During under Bias .... -40°C to +85°C
During non Bias .... -65°C to +125°C

Voltage On Any Pin
(except V_{CC} and V_{CCW}) .... -0.5V to V_{CC}+0.5V(2)

V_{CC} Supply Voltage................................ -0.2V to +4.6V(2)

V_{CCW} Supply Voltage......................... -0.2V to +13.0V(2,3)

Output Short Circuit Current................................100mA(4)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{CCW} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins are V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Maximum DC voltage on V_{CCW} may overshoot to +13.0V for periods <20ns. Applying 12V±0.3V to V_{CCW} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{CCW} may be connected to 12V±0.3V for a total of 80 hours maximum.
4. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Test Condition
T_A	Operating Temperature	-40	+85	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage (2.7V-3.6V)	2.7	3.6	V	

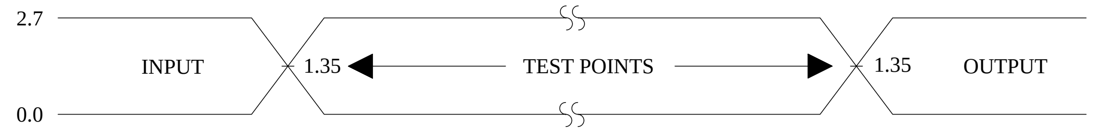
6.2.1 CAPACITANCE(1)

T_A=+25°C, f=1MHz

Symbol	Parameter	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance	7	10	pF	V_{IN}=0.0V
C_{OUT}	Output Capacitance	9	12	pF	V_{OUT}=0.0V

NOTE:
1. Sampled, not 100% tested.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS



AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0". Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 ns.

Figure 12. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

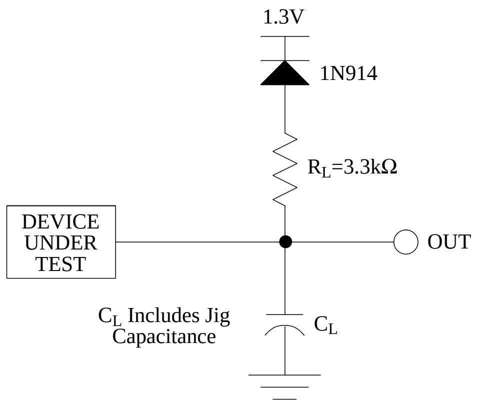


Figure 13. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L(pF)
V_{CC}=2.7V-3.6V	50

6.2.3 DC CHARACTERISTICS

DC Characteristics

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V		Unit	Test Conditions
			Typ.	Max.		
I_{LI}	Input Load Current	1		±0.5	µA	$V_{CC}=V_{CC}$Max. $V_{IN}=V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		±0.5	µA	$V_{CC}=V_{CC}$Max. $V_{OUT}=V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,5	2	15	µA	CMOS Level Inputs $V_{CC}=V_{CC}$Max. CE#=RP#=V_{CC}±0.2V
			0.2	2	mA	TTL Level Inputs $V_{CC}=V_{CC}$Max. CE#=RP#=V_{IH}
I_{CCAS}	V_{CC} Auto Power-Save Current	1,4,5	2	15	µA	CMOS Level Inputs $V_{CC}=V_{CC}$Max. CE#=GND±0.2V
I_{CCD}	V_{CC} Reset Power-Down Current	1	2	15	µA	RP#=GND±0.2V
I_{CCR}	V_{CC} Read Current	1,5	15	25	mA	CMOS Level Inputs $V_{CC}=V_{CC}$Max., CE#=GND f=5MHz, I_{OUT}=0mA
				30	mA	TTL Level Inputs $V_{CC}=V_{CC}$Max., CE#=GND f=5MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} Word Write or Set Lock-Bit Current	1,6	5	17	mA	V_{CCW}=2.7V-3.6V
			5	12	mA	V_{CCW}=11.7V-12.3V
I_{CCE}	V_{CC} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current	1,6	4	17	mA	V_{CCW}=2.7V-3.6V
			4	12	mA	V_{CCW}=11.7V-12.3V
I_{CCWS} I_{CCES}	V_{CC} Word Write or Block Erase Suspend Current	1,2	1	6	mA	CE#=V_{IH}
I_{CCWS}	V_{CCW} Standby or Read Current	1	±2	±15	µA	$V_{CCW} \leq V_{CC}$
I_{CCWR}			10	200	µA	$V_{CCW} > V_{CC}$
I_{CCWAS}	V_{CCW} Auto Power-Save Current	1,4,5	0.1	5	µA	CMOS Level Inputs $V_{CC}=V_{CC}$Max. CE#=GND±0.2V
I_{CCWD}	V_{CCW} Reset Power-Down Current	1	0.1	5	µA	RP#=GND±0.2V
I_{CCWW}	V_{CCW} Word Write or Set Lock-Bit Current	1,6	12	40	mA	V_{CCW}=2.7V-3.6V
				30	mA	V_{CCW}=11.7V-12.3V
I_{CCWE}	V_{CCW} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current	1,6	8	25	mA	V_{CCW}=2.7V-3.6V
				20	mA	V_{CCW}=11.7V-12.3V
I_{CCWWS} I_{CCWES}	V_{CCW} Word Write or Block Erase Suspend Current	1	10	200	µA	$V_{CCW}=V_{CCWH1/2}$

DC Characteristics (Continued)

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V Min.	V_{CC}=2.7V-3.6V Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	6	-0.5	0.8	V	
V_{IH}	Input High Voltage	6	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage	6		0.4	V	V_{CC}=V_{CC} Min. I_{OL}=2.0mA
V_{OH1}	Output High Voltage (TTL)	6	2.4		V	V_{CC}=V_{CC} Min. I_{OH}=-2.0mA
V_{OH2}	Output High Voltage (CMOS)	6	0.85 V_{CC}		V	V_{CC}=V_{CC} Min. I_{OH}=-2.5mA
			V_{CC} -0.4		V	V_{CC}=V_{CC} Min. I_{OH}=-100μA
V_{CCWLK}	V_{CCW} Lockout during Normal Operations	3,6		1.0	V	
V_{CCWH1}	V_{CCW} during Block Erase, Full Chip Erase, Word Write or Lock-Bit Configuration Operations		2.7	3.6	V	
V_{CCWH2}	V_{CCW} during Block Erase, Full Chip Erase, Word Write or Lock-Bit Configuration Operations	7	11.7	12.3	V	
V_{LKO}	V_{CC} Lockout Voltage		2.0		V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A=+25°C.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Block erases, full chip erase, word writes and lock-bit configurations are inhibited when $V_{CCW} \leq V_{CCWLK}$, and not guaranteed in the range between V_{CCWLK}(max.) and V_{CCWH1}(min.), between V_{CCWH1}(max.) and V_{CCWH2}(min.) and above V_{CCWH2}(max.).
4. The Automatic Power Savings (APS) feature is placed automatically power save mode that addresses not switching more than 300ns while read mode.
5. About all of pin except describe Test Conditions, CMOS level inputs are either V_{CC}±0.2V or GND±0.2V, TTL level inputs are either V_{IL} or V_{IH}.
6. Sampled, not 100% tested.
7. Applying 12V±0.3V to V_{CCW} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{CCW} may be connected to 12V±0.3V for a total of 80 hours maximum.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		90		ns
t_{AVQV}	Address to Output Delay			90	ns
t_{ELQV}	CE# to Output Delay	2		90	ns
t_{PHQV}	RP# High to Output Delay			600	ns
t_{GLQV}	OE# to Output Delay	2		40	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# High to Output in High Z	3		40	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# High to Output in High Z	3		15	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns

NOTES:
1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.

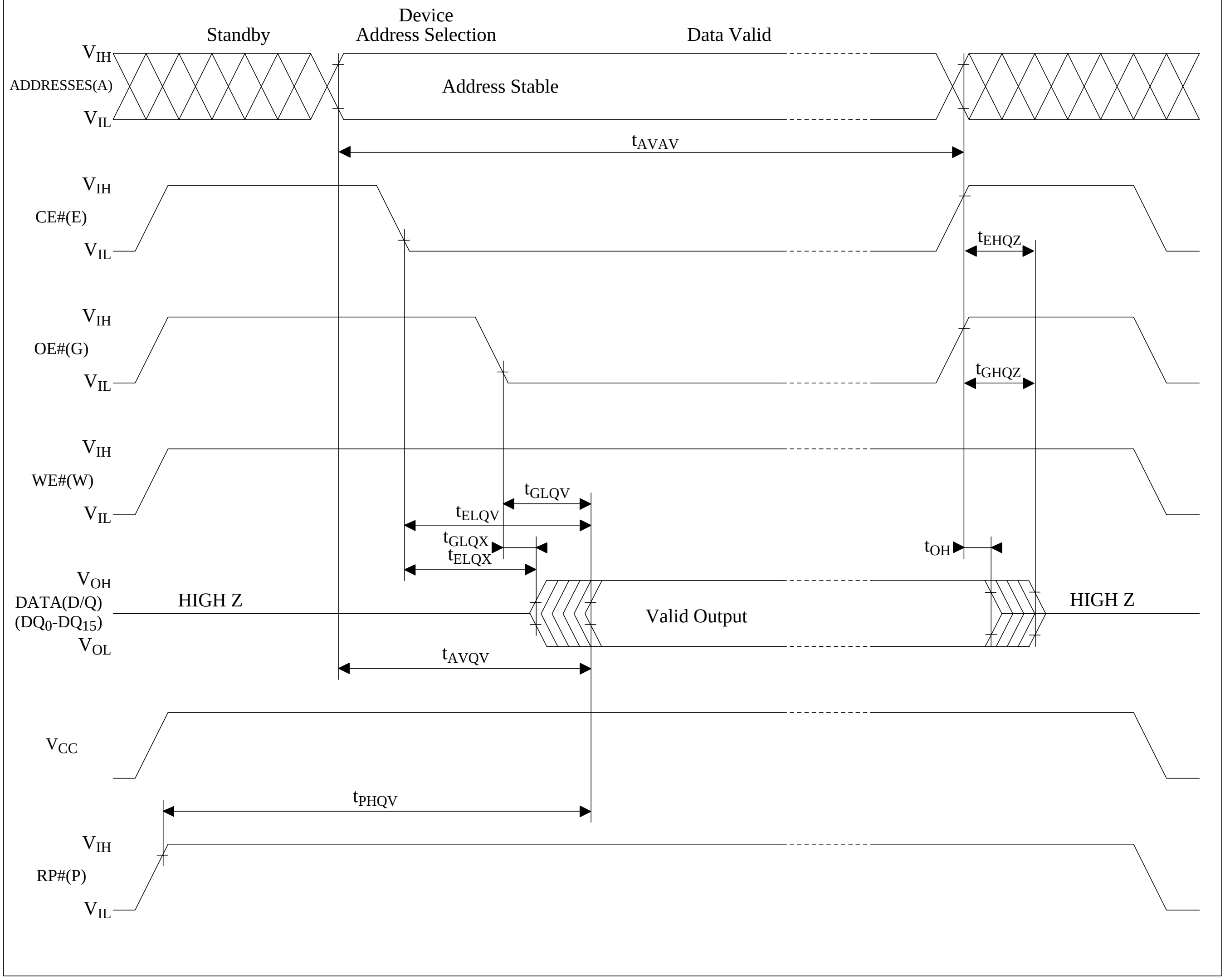


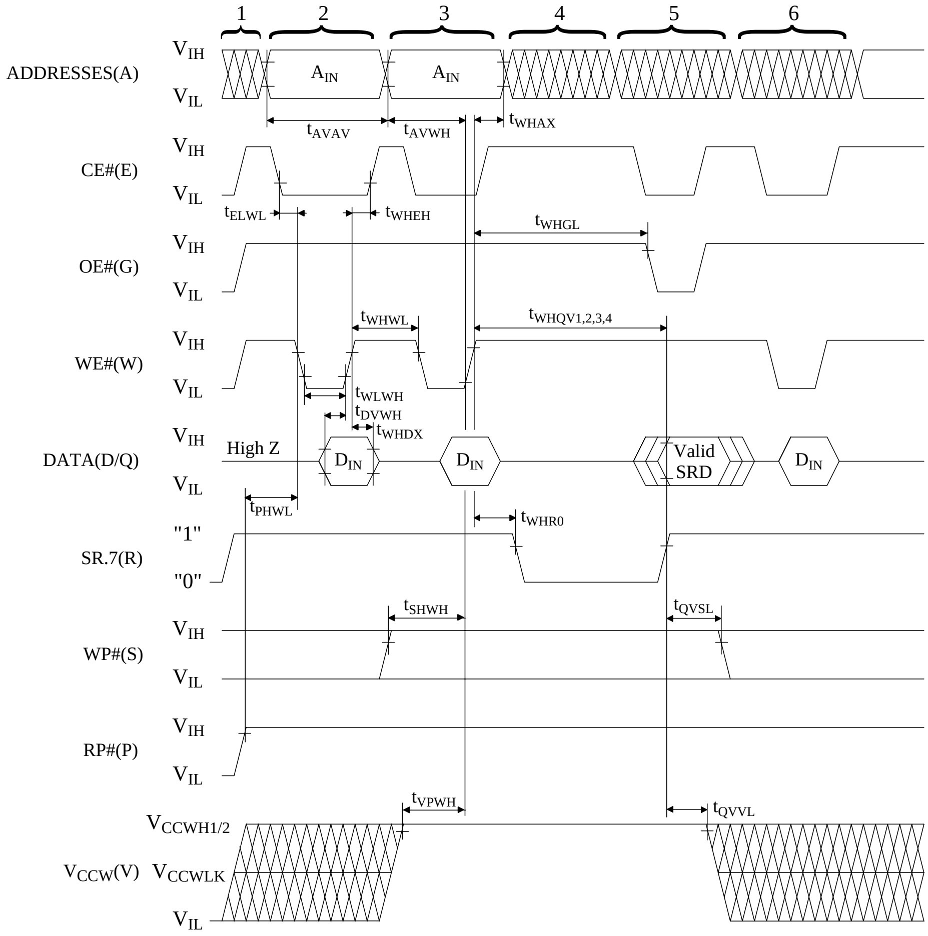
Figure 14. AC Waveform for Read Operations

6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS$^{(1)}$

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		90		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		ns
t_{WLWH}	WE# Pulse Width		50		ns
t_{SHWH}	WP#V_{IH} Setup to WE# Going High	2	100		ns
t_{VPWH}	V_{CCW} Setup to WE# Going High	2	100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		ns
t_{WHDX}	Data Hold from WE# High		0		ns
t_{WHAX}	Address Hold from WE# High		0		ns
t_{WHEH}	CE# Hold from WE# High		10		ns
t_{WHWL}	WE# Pulse Width High		30		ns
t_{WHR0}	WE# High to SR.7 Going "0"			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{CCW} Hold from Valid SRD	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD	2,4	0		ns

NOTES:
1. Read timing characteristics during block erase, full chip erase, word write and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid A_{IN} and D_{IN} for block erase, full chip erase, word write or lock-bit configuration.
4. V_{CCW} should be held at $V_{CCWH1/2}$ until determination of block erase, full chip erase, word write or lock-bit configuration success (SR.1/3/4/5=0).



NOTES:

1. V_{CC} power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

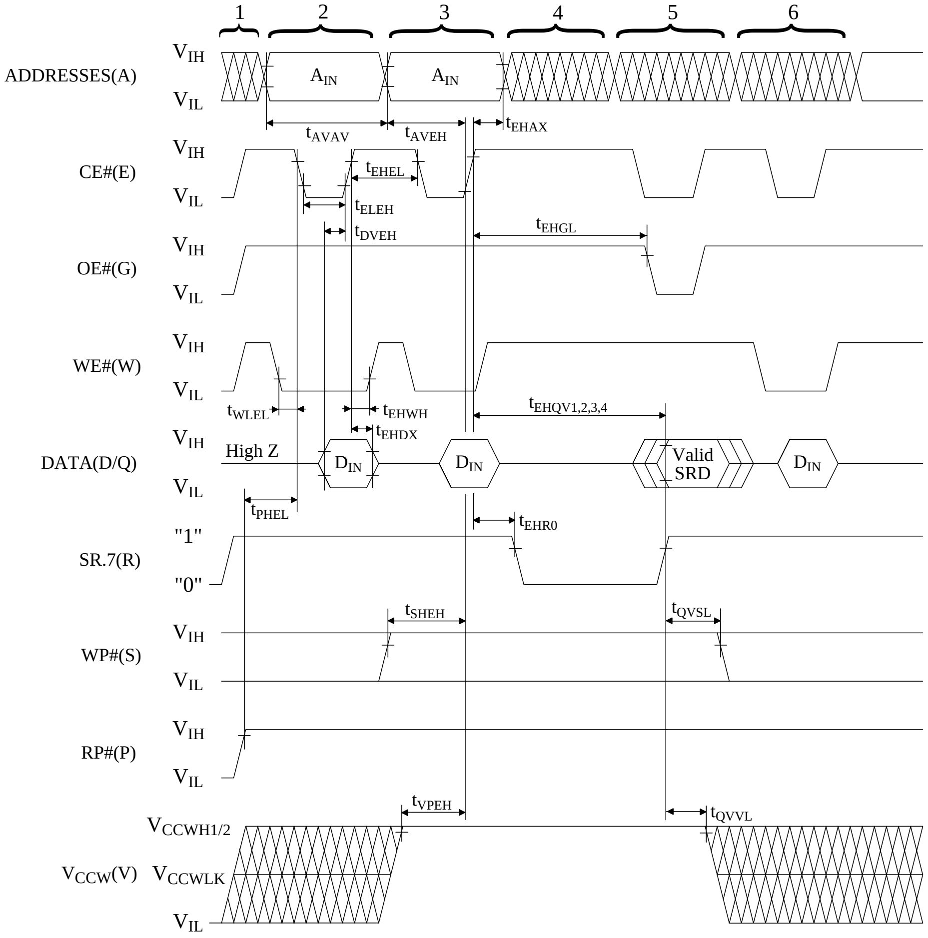
Figure 15. AC Waveform for WE#-Controlled Write Operations

6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		90		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		ns
t_{ELEH}	CE# Pulse Width		65		ns
t_{SHEH}	WP#V_{IH} Setup to CE# Going High	2	100		ns
t_{VPEH}	V_{CCW} Setup to CE# Going High	2	100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		ns
t_{EHDX}	Data Hold from CE# High		0		ns
t_{EHAX}	Address Hold from CE# High		0		ns
t_{EHWH}	WE# Hold from CE# High		0		ns
t_{EHEL}	CE# Pulse Width High		25		ns
t_{EHR0}	CE# High to SR.7 Going "0"			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{CCW} Hold from Valid SRD	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD	2,4	0		ns

NOTES:
1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold, and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid A_{IN} and D_{IN} for block erase, full chip erase, word write or lock-bit configuration.
4. V_{CCW} should be held at $V_{CCWH1/2}$ until determination of block erase, full chip erase, word write or lock-bit configuration success (SR.1/3/4/5=0).



NOTES:
1. V_{CC} power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 16. AC Waveform for CE#-Controlled Write Operations

6.2.7 RESET OPERATIONS

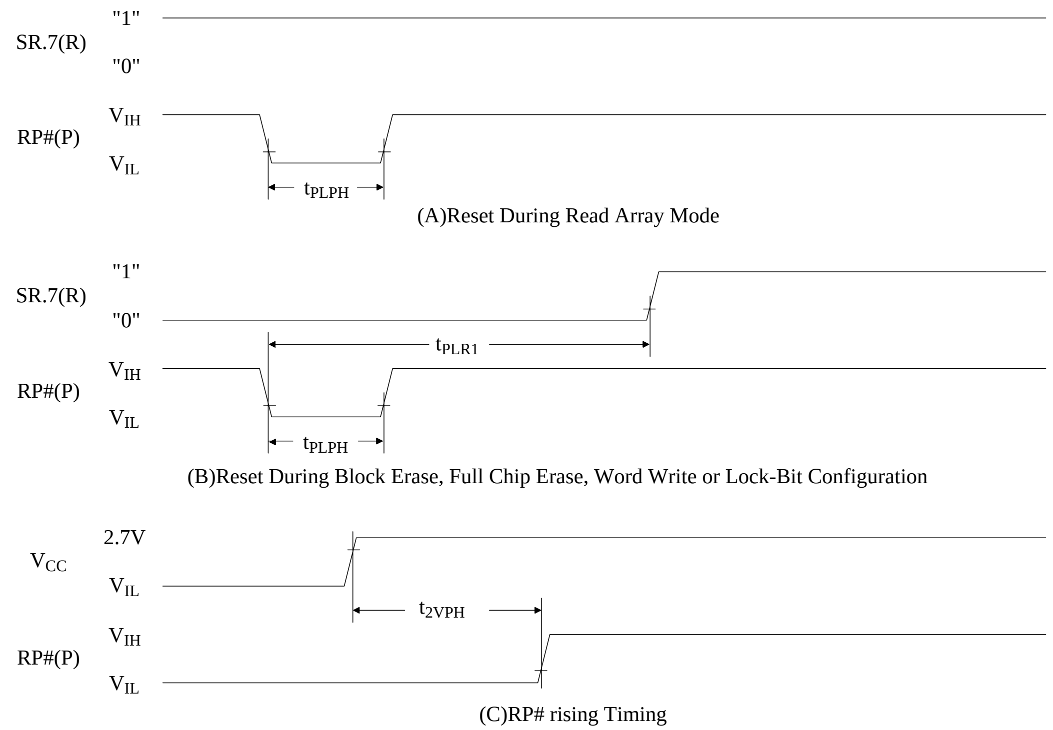


Figure 17. AC Waveform for Reset Operation

Reset AC Specifications

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	RP# Pulse Low Time	2	100		ns
t_{PLR1}	RP# Low to Reset during Block Erase, Full Chip Erase, Word Write or Lock-Bit Configuration	1,2		30	µs
t_{2VPH}	V_{CC} 2.7V to RP# High	2,3	100		ns

NOTES:

1. If RP# is asserted while a block erase, full chip erase, word write or lock-bit configuration operation is not executing, the reset will complete within 100ns.
2. A reset time, t_{PHQV}, is required from the later of SR.7 going "1" or RP# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
3. When the device power-up, holding RP# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.8 BLOCK ERASE, FULL CHIP ERASE, WORD WRITE AND LOCK-BIT CONFIGURATION PERFORMANCE(3)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter		Notes	V_{CCW}=2.7V-3.6V			V_{CCW}=11.7V-12.3V			Unit
				Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word Write Time	32K word Block	2		33	200		20		µs
		4K word Block	2		36	200		27		µs
	Block Write Time	32K word Block	2		1.1	4		0.66		s
		4K word Block	2		0.15	0.5		0.12		s
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block	2		1.2	6		0.9		s
		4K word Block	2		0.6	5		0.5		s
	Full Chip Erase Time		2		42	210		32		s
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time		2		56	200		42		µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time		2		1	5		0.69		s
t_{WHR11} t_{EHR11}	Word Write Suspend Latency Time to Read		4		6	15		6	15	µs
t_{WHR12} t_{EHR12}	Block Erase Suspend Latency Time to Read		4		16	30		16	30	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command		5	600			600			µs

NOTES:

1. Typical values measured at T_A=+25°C and V_{CC}=3.0V, V_{CCW}=3.0V or 12.0V. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.
4. A latency time is required from issuing suspend command(WE# or CE# going high) until SR.7 going "1".
5. If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than t_{ERES} and both commands are written repeatedly, a longer time is required than standard block erase until the completion of the operation.

7 Package and packing specification

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5~40℃
- Normal humidity : 80% R.H. max.

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1, or Manual soldering.)

- Temperature : 5~25℃
- Humidity : 60% R.H. max.
- Period : 72 hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5~25℃。
- Humidity : 60% R.H. max.
- Period : 72 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5~25℃。
- Humidity : 60% R.H. max.
- Period : 72 hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

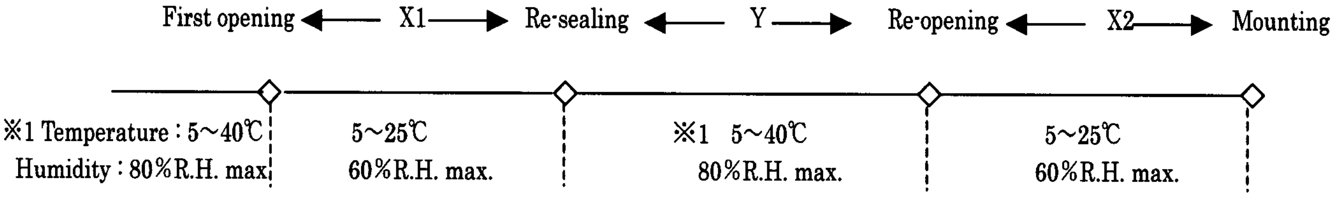
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1+X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened. (Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period : 120°C for 16~24 hours or 150°C for 5~10 hours.
- The above baking conditions do not apply since the embossed carrier tape are not heat-resistant . Replace the devices on heat-resistant carrier .

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

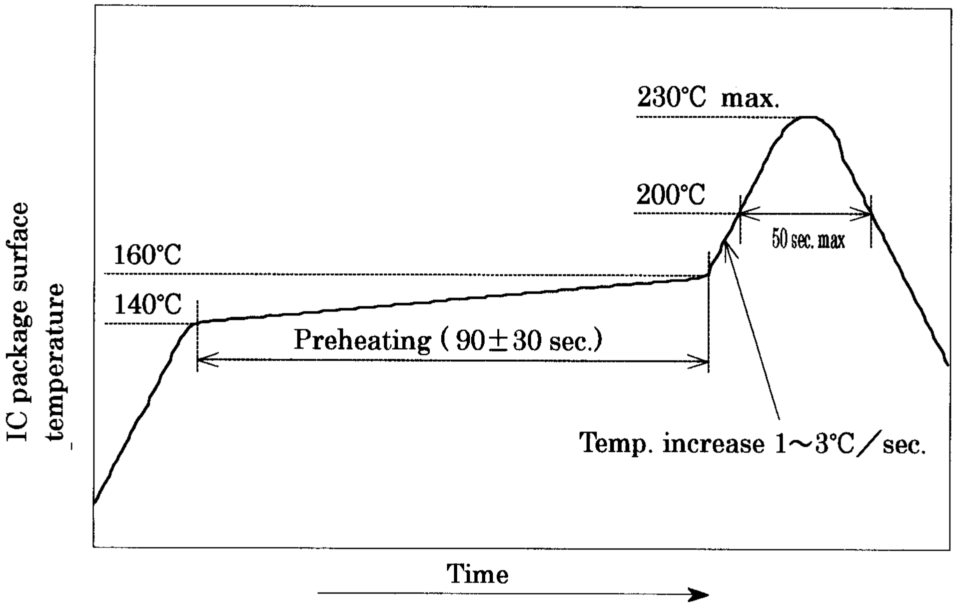
3.Surface mount conditions.

The following soldering condition are recommended to ensure device quality.

3-1.Soldering.

(1) Convection reflow or IR/Convection. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :
  Peak temperature of 230°C max.
  Above 200°C for 50 sec. max.
  Preheat temperature of 140~160°C for 90±30 sec.
  Temperature increase rate of 1~3°C/sec.
- Measuring point : IC package surface.
- Temperature profile :



(2) Manual soldering (soldering iron) (one-time soldering only)

Soldering iron should only touch the IC's outer leads.

- Temperature and period :

  350°C max. for 3 sec. / pin max., or 260°C max. for 10 sec. / pin max.

  (Soldering iron should only touch the IC's outer leads.)

- Measuring point : Soldering iron tip.

4. Condition for removal of residual flax.

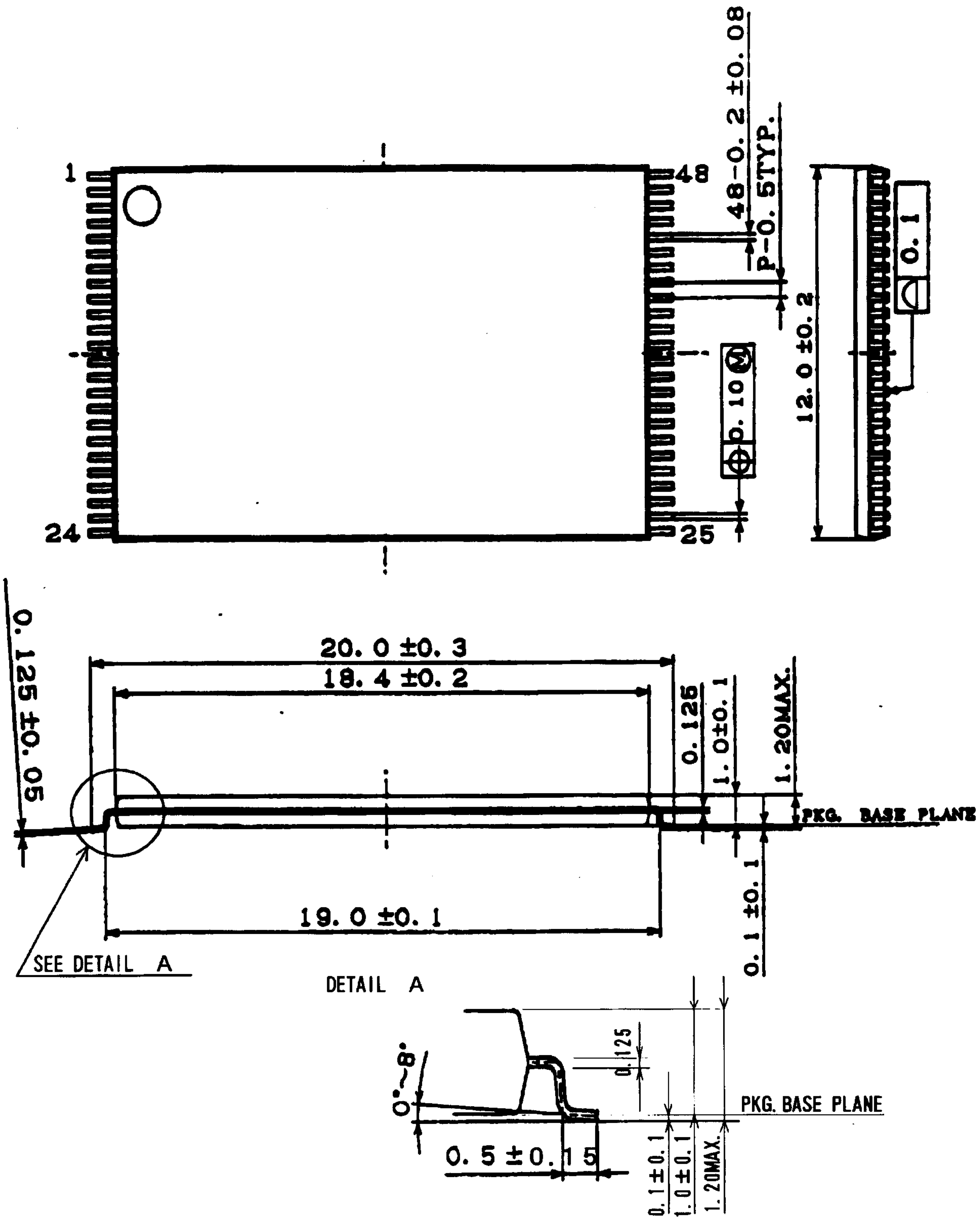
(1) Ultrasonic washing power : 25 watts / liter max.

(2) Washing time : Total 1 minute max.

(3) Solvent temperature : 15~40°C

5. Package outline specification.
   Refer to the attached drawing.

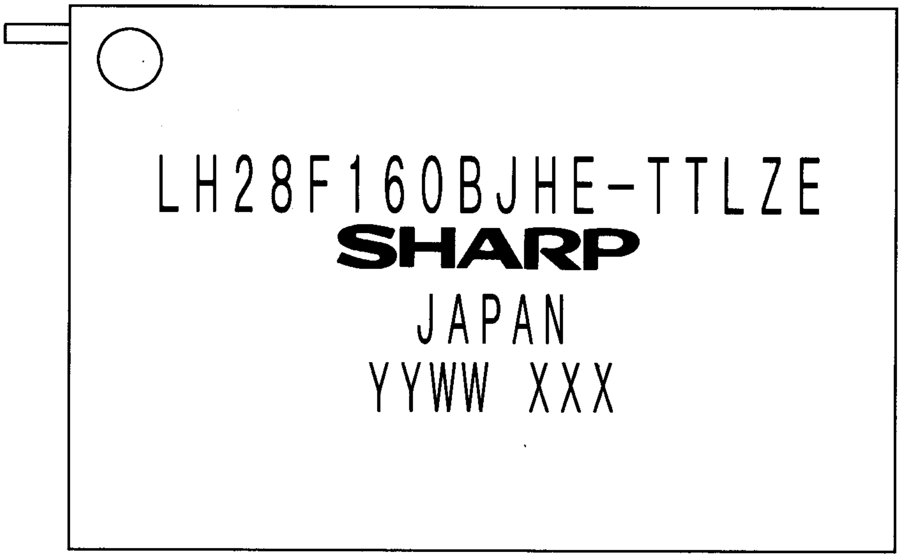
6. Markings.
   6-1.Marking details. (The information on the package should be given as follows.)
   (1) Product name : LH28F160BJHE-TTLZE
   (2) Company name : SHARP
   (3) Date code
   (Example) Z YY WW XXX
   XXX → Denotes the production ref. code (1～3 digits).
   WW → Denotes the production week. (01・02・～・52・53)
   YY → Denotes the production year.
   (Last two digits of the year.)
   Z → Denotes the production ref. code
   (No marking , A , B , C)
   (4) "JAPAN" is marked on the package when both wafer and assembly processes are done in Japan , indicating the country of origin.
   6-2.Marking layout.
   The layout is shown in the attached drawing.
   (However, this layout does not specify the size of the marking character and marking position.)



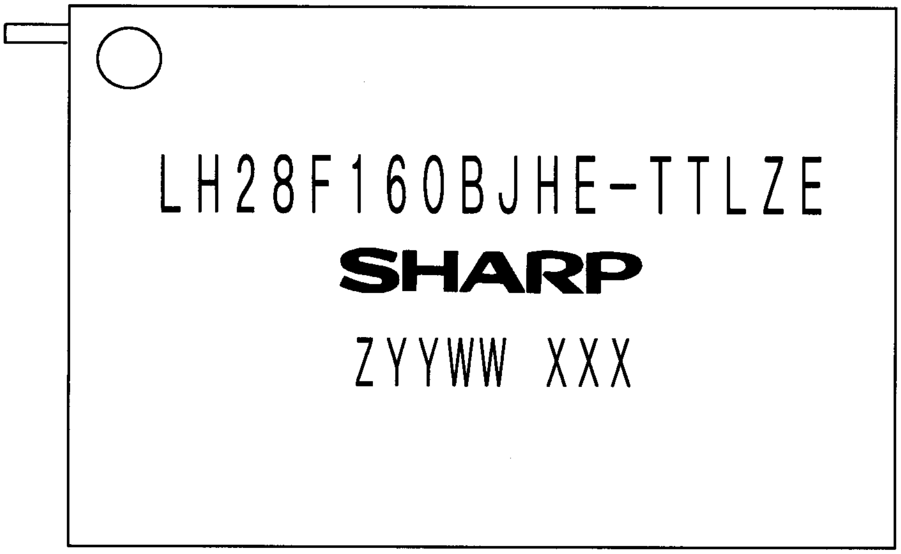
<table>
<tr><td colspan="2">リード表面処理
LEAD FINISH</td><td colspan="2">ハンダメッキ
TIN-LEAD PLATING</td><td>リード材質
LEAD MATERIAL</td><td>42ALLOY</td></tr>
<tr><td>名称
NAME</td><td colspan="3">TSOP048-P-1220</td><td colspan="2" rowspan="2">備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。
NOTE Plastic body dimensions do not include burr of resin.</td></tr>
<tr><td>DRAWING NO.</td><td>AA1142</td><td>単位
UNIT</td><td>mm</td></tr>
</table>

マークレイアウト図
Marking layout

『JAPAN』表記がある場合のマーク仕様
Marking layout when “JAPAN” is indicated.



『JAPAN』表記がない場合のマーク仕様
Marking layout when “JAPAN” is not indicated.



7.Packing specifications (Embossed carrier tape specifications)

This standard applies to the embossed carrier tape specifications for ICs supplied by SHARP CORPORATION. SHARP's embossed carrier tape specifications are generally based on those described in JIS C 0806 (Japanese Industrial Standard) and EIA481A.

7-1.Tape structure

The embossed carrier tape is made of conductive plastic. The embossed portions of the carrier tape are filled with IC packages and a top covering tape is used to enclose them.

7-2.Taping reel and embossed carrier tape size

For the taping reel and embossed carrier tape sizes, refer to the attached drawing.

7-3.IC package enclosure direction in embossed carrier tape

The IC package enclosure direction in the embossed portion relative to the direction in which the tape is pulled is indicated by an index mark on the package (indicating the No. 1 pin) shown in the attached drawing.

7-4.Missing IC packages in embossed carrier tape

The number of missing IC packages in the embossed carrier tape per reel should not exceed Either 1 or 0.1 % of the total contained on the tape per reel, whichever is larger. There should never be more than two consecutive missing IC packages.

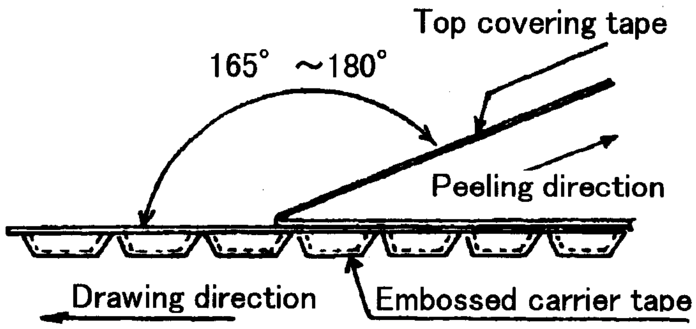
7-5.Tape joints

The embossed carrier tape should have no more than one joint per reel.

7-6.Peeling strength of the top covering tape

Peeling strength must meet the following conditions.

(1) Peeling angle at 165～180° .
(2) Peeling speed at 300mm／min .
(3) Peeling strength at 0.2～0.7N (20～70gf) .



7-7. Packing

(1) The top covering tape (leader side) at the leading edge of the embossed carrier tape, and the trailing edge of the embossed carrier tape, should both be held in place with paper adhesive tape at least 30 mm in length.

(2) The leading and trailing edges of the embossed carrier tape should be left empty (with embossed portions not filled with IC packages) in the attached drawing.

(3) The number of IC packages enclosed in the embossed carrier tape per reel should generally comply with the list given below.

Number of IC Packages/ Reel	Number of IC Packages/ Inner carton	Number of IC Packages/ Outer carton
1000 devices / Reel	1000 devices / Inner carton	5000 devices / Outer carton

7-8.Indications

The following should be indicated on the taping reel and the packing carton.

- Part Number (Product Name) · Storage Quantity · Packed date
- Manufacture's Name (SHARP)

Note : The IC taping direction is indicated by " E2 " suffixed to the part number .

7-9.Protection during transportation

The IC packages should have no deformation and deterioration of their electrical Characteristics resulting from transportation.

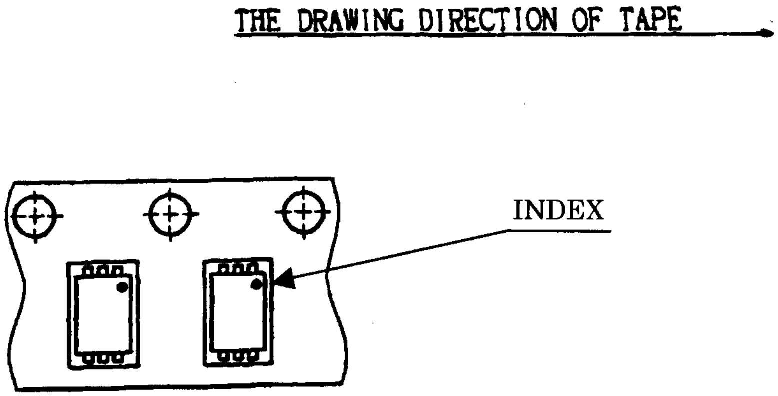
8.Precautions for use.

(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.

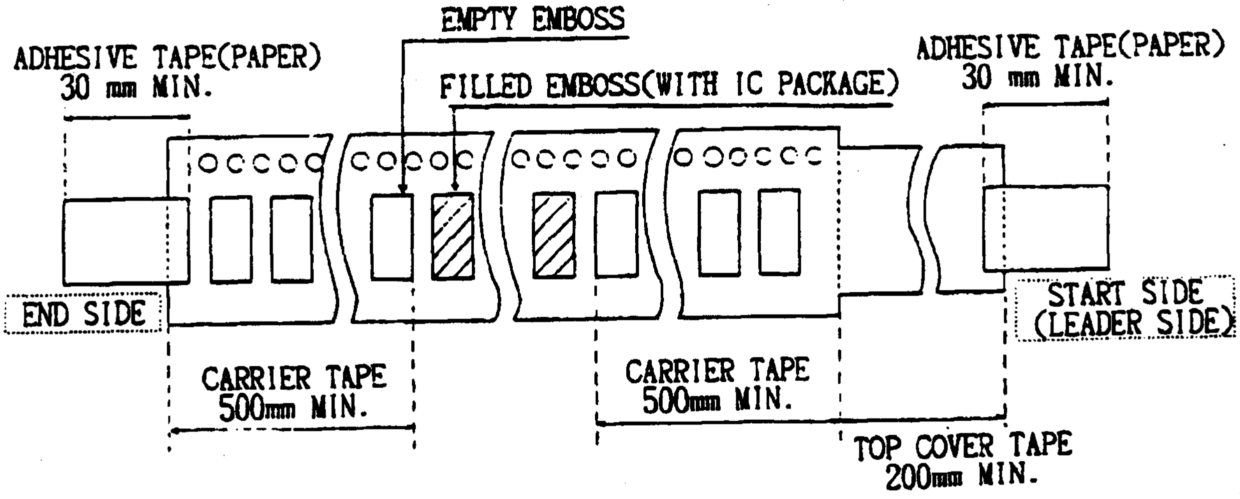
(2) The devices should be mounted the devices within one year of the date of delivery.

EMBOSS TAPING TYPE

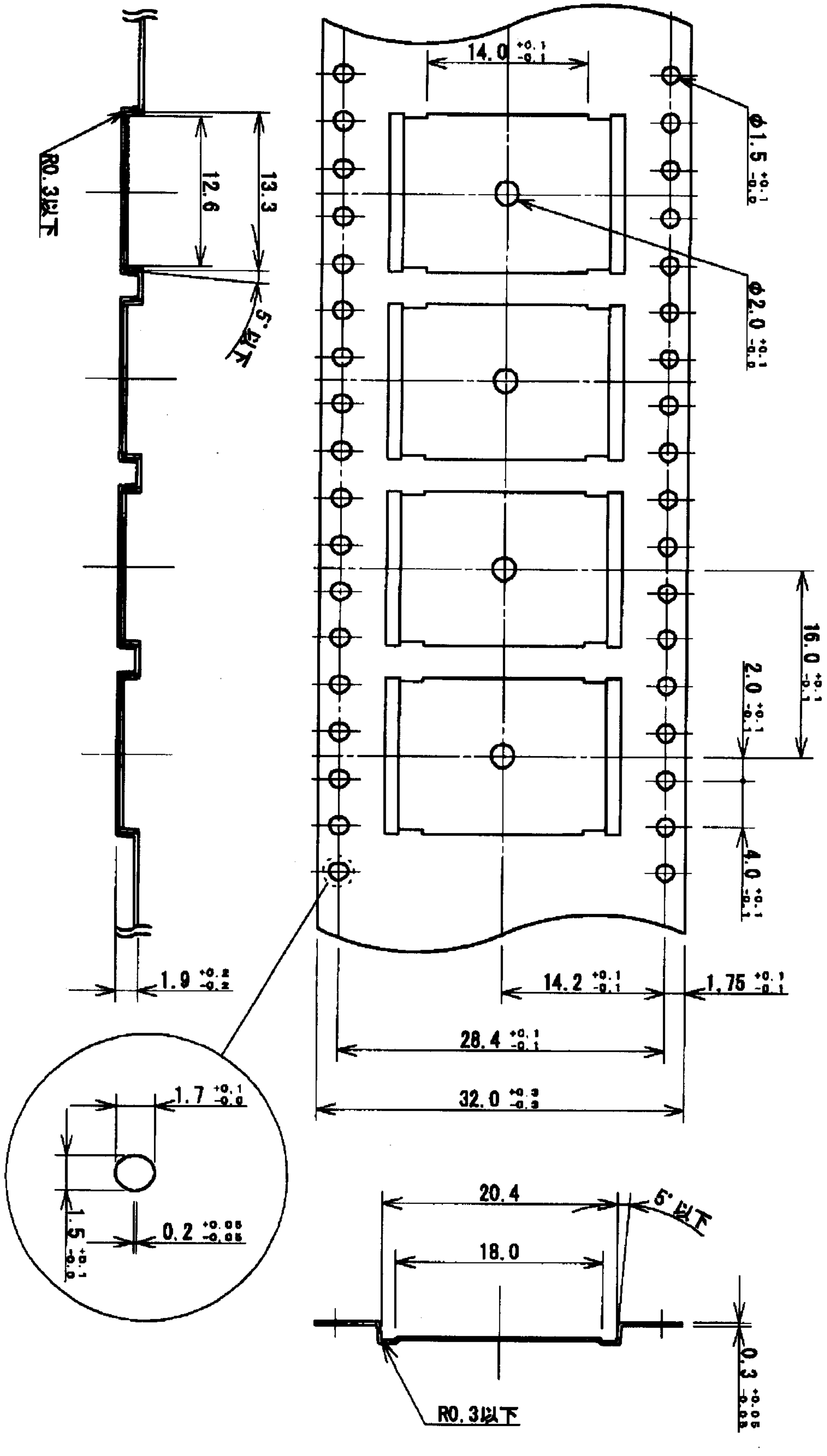
IC TAPING DIRECTION



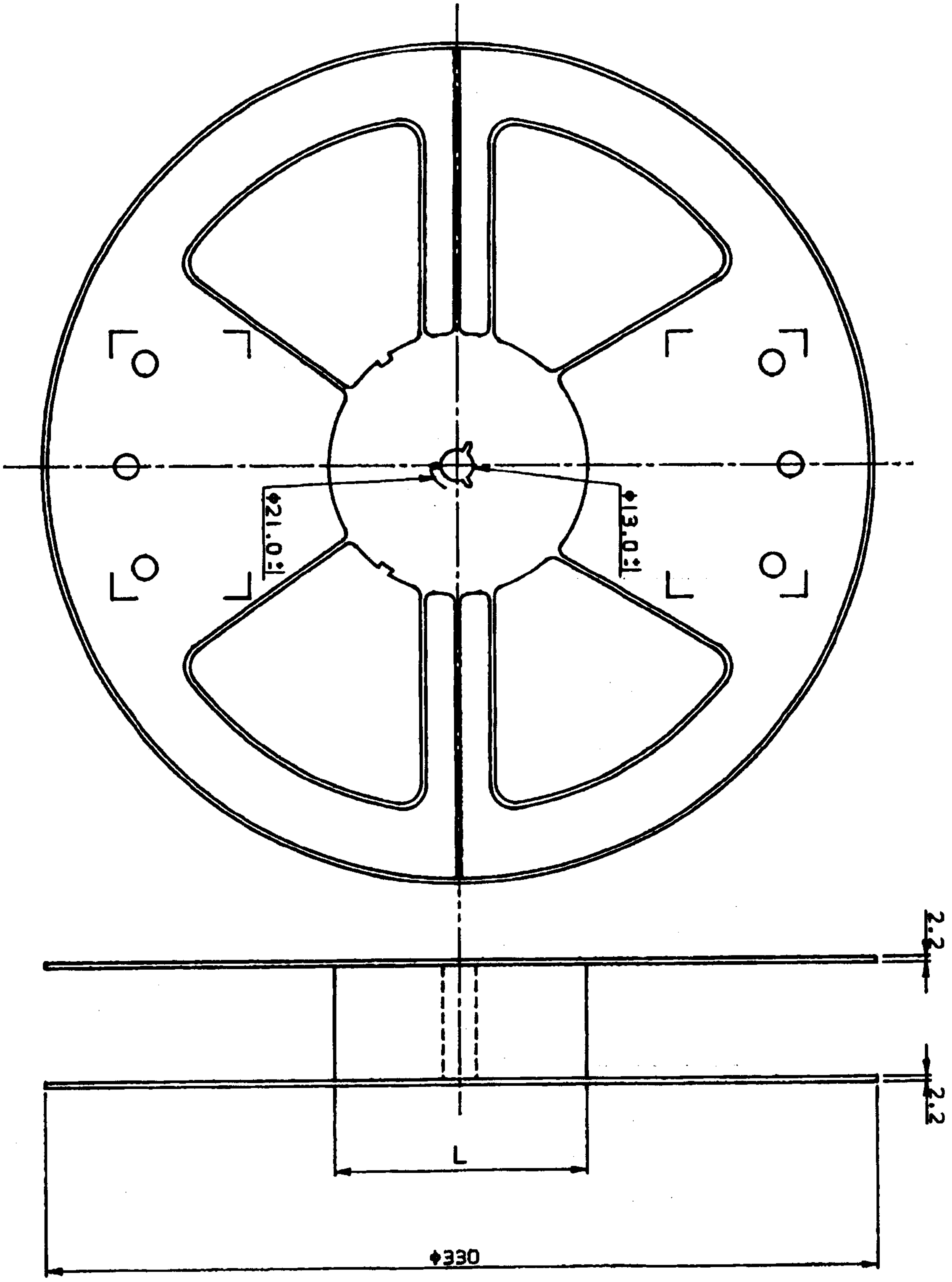
LEADER SIDE AND END SIDE OF TAPE



名称 NAME	Emboss taping type(E2)			備考 NOTE
DRAWING NO.	CV522	単位 UNIT	mm	

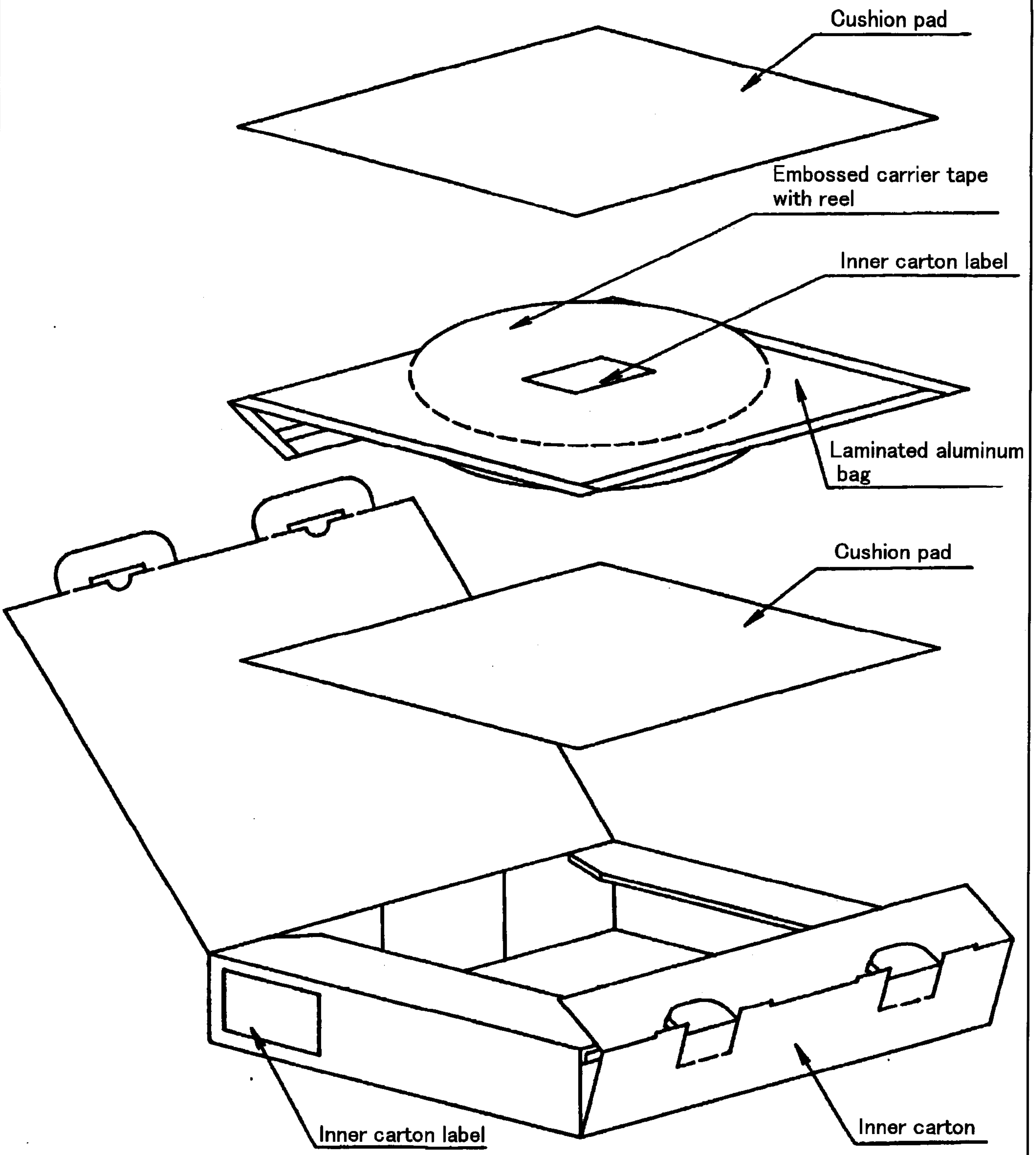


名称 NAME	LEC48-1220TSPTS			備考 NOTE
DRAWING NO.	CV758-01	単位 UNIT	mm	



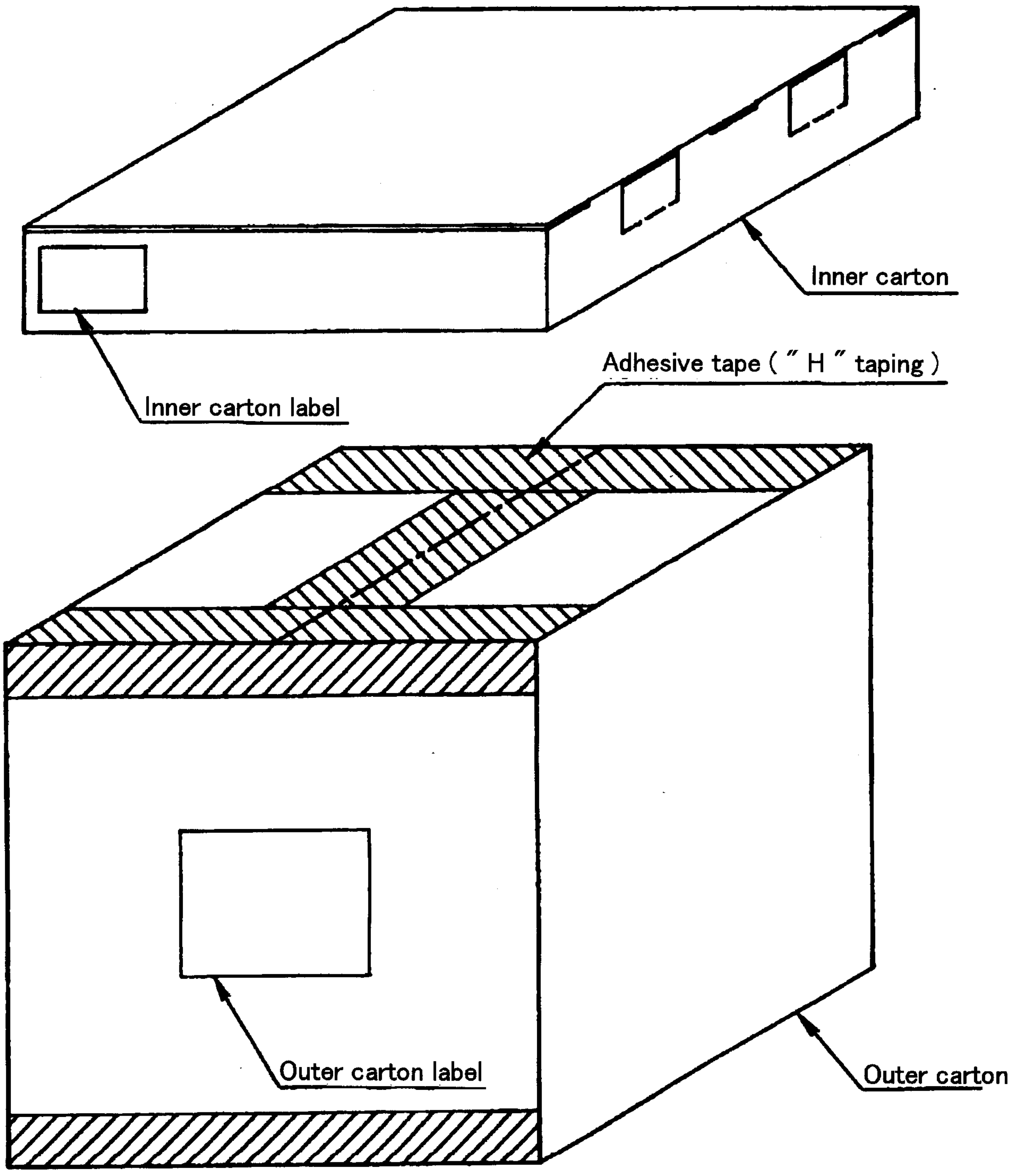
PKG	L(mm)
TSOP048-P-1220	φ100

名称 NAME	Reel for embossed carrier tape		備考 NOTE
DRAWING NO.	CV755	単位 UNIT	mm



	L		W		H
Inner carton . Outer dimensions : :	345	×	345	×	55

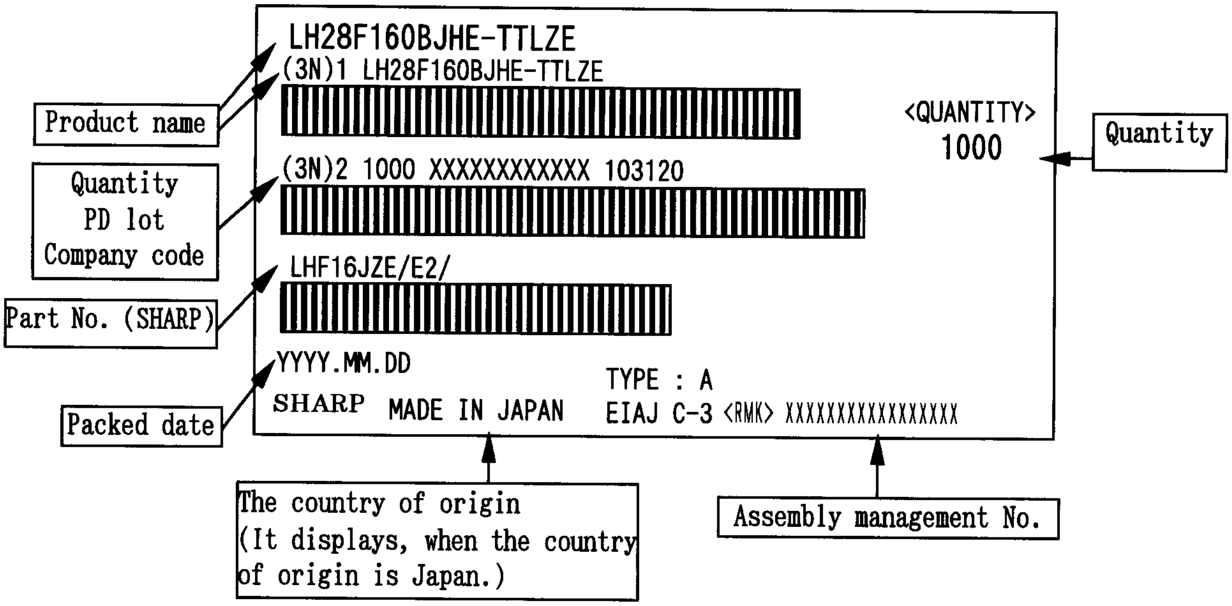
名称 NAME	Packing specifications《1》		備考 NOTE
DRAWING NO.	CV428	単位 UNIT	mm



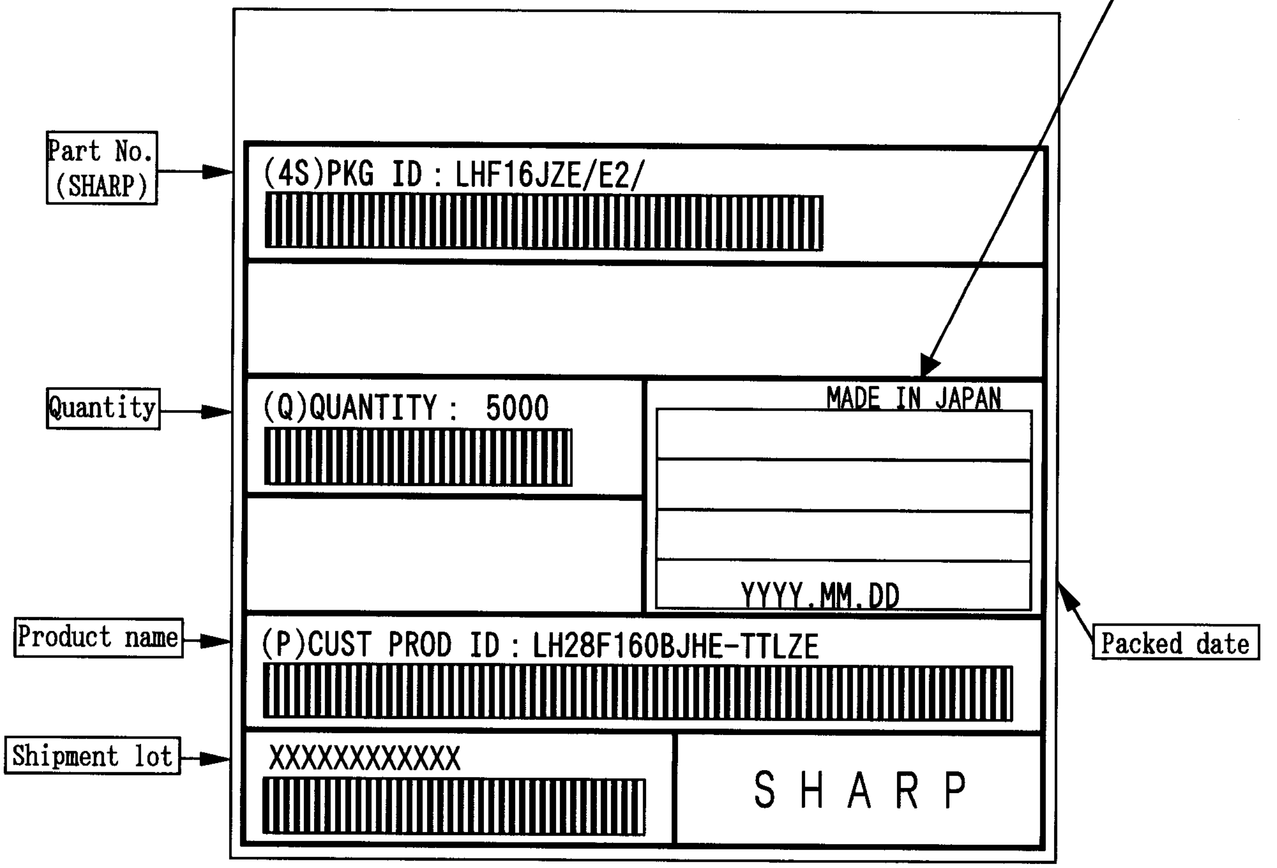
	L		W		H
Inner carton - Outer dimensions :	345	×	345	×	55
Outer carton - Outer dimensions :	365	×	315	×	385

名称 NAME	Packing specifications《2》			備考　出荷数量が端数の場合、本仕様と異なることがあります。 NOTE There is a possibility different from this specification when the number of shipments is fractions.
DRAWING NO.	BJ426	単位 UNIT	mm	

Inner carton label



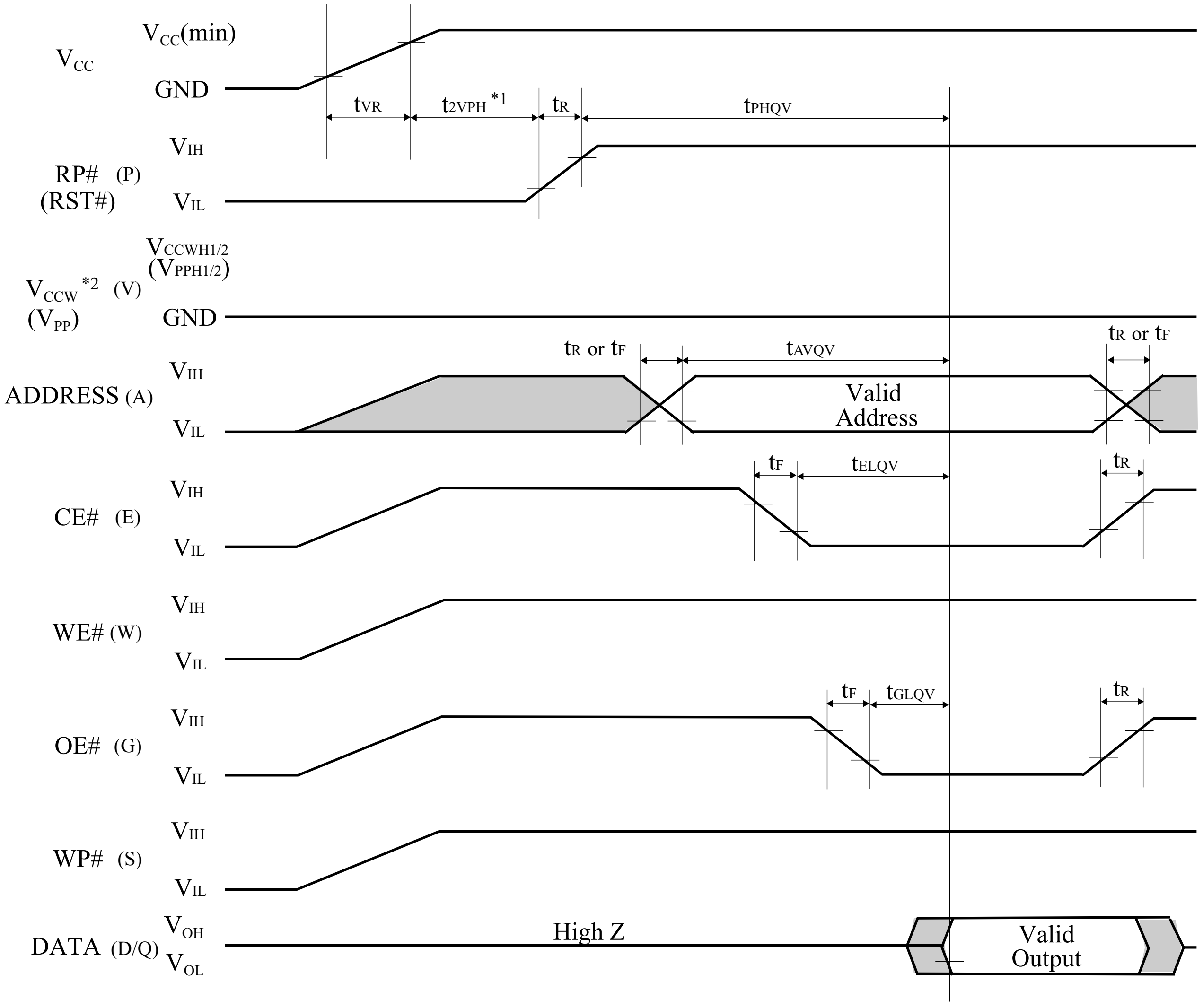
Outer carton label



A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 t_{5VPH} for the device in 5V operations.

*2 To prevent the unwanted writes, system designers should consider the V_{CCW} (V_{PP}) switch, which connects V_{CCW} (V_{PP}) to GND during read operations and $V_{CCWH1/2}$ ($V_{PPH1/2}$) during write or erase operations.
See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS“ described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations. t_R(Max.) and t_F(Max.) for RP# (RST#) are 50µs/V.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

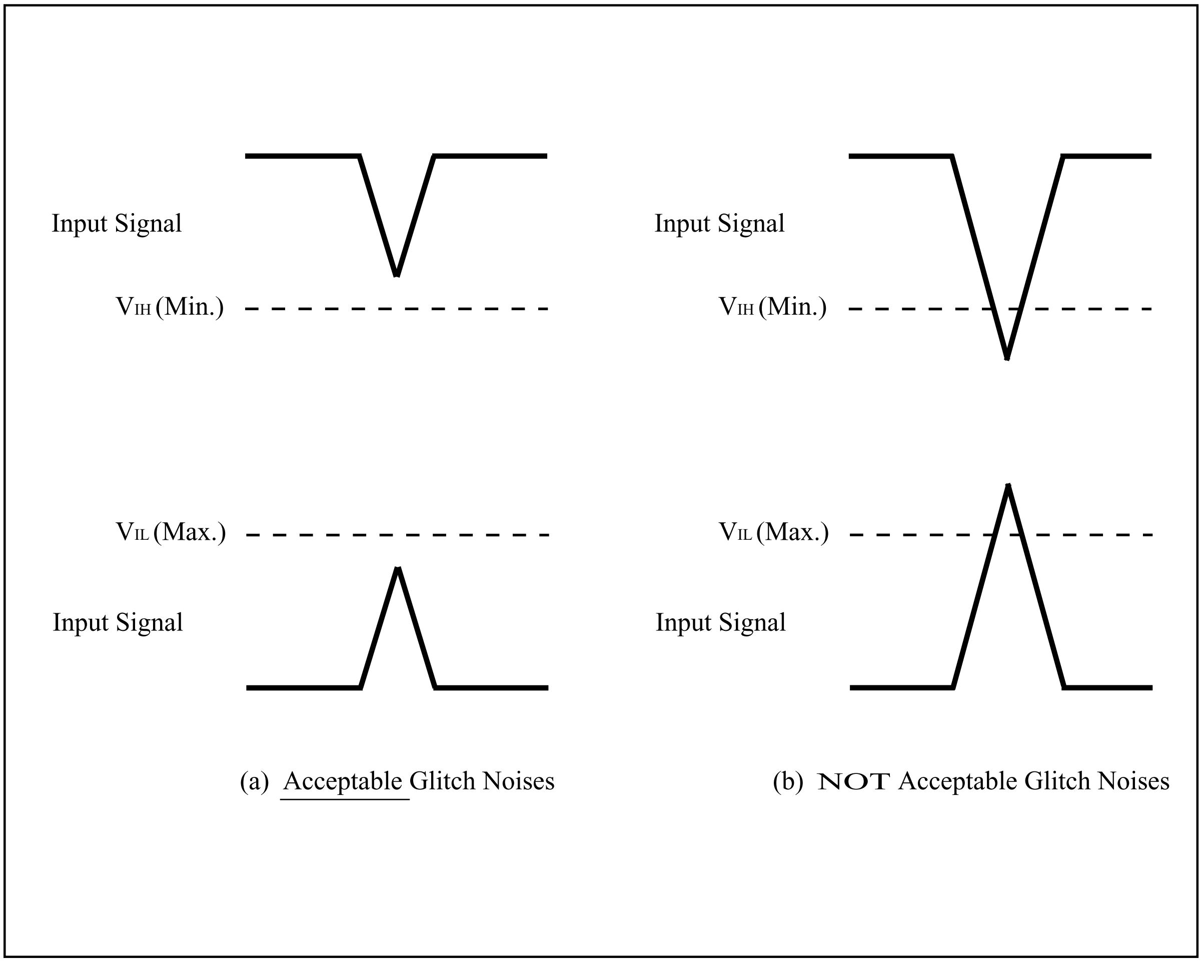


Figure A-2. Waveform for Glitch Noises

See the “DC CHARACTERISTICS“ described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION(1)

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:

1. International customers should contact their local SHARP or distribution sales office.

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