National Semiconductor

LH4012/LH4012C Wideband Buffer

General Description

The LH4012 is a very high speed buffer designed to provide high current drive at frequencies from DC to over 400 MHz. The LH4012/LH4012C will provide ±200 mA into 50Ω loads at slew rates of 11500 V/μs. In addition, it exhibits excellent phase linearity.

The LH4012 is intended to fulfill a wide range of buffer applications. Due to its high speed it does not degrade the system performance. Its high output current makes it adequate for most loads. Only a single +10V supply is needed for a 5 V_{PP} video signal.

These devices are constructed using specially selected bipolar transistors to achieve guaranteed performance specifications. The LH4012K is specified for operation from −55°C to +125°C; the LH4012CK is specified from −25°C to +85°C. Both devices are available in an 8-pin TO-3 package.

Features

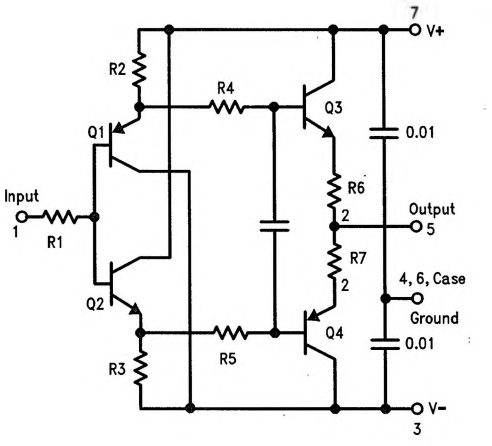
- Internal supply bypass capacitors
- Ultra fast slewing — 11500 V/μs
- Wide range single or dual supply operation
- Wide bandwidth — DC to 490 MHz
- High output drive — ±10V with 50Ω load
- Low phase non-linearity — 1 deg.
- Fast rise times — 1.2 ns

Applications

- High speed line drivers
- Video impedance transformation
- Op amp isolation buffers
- Yoke driver for high resolution CRT

Schematic Diagram

LH4012



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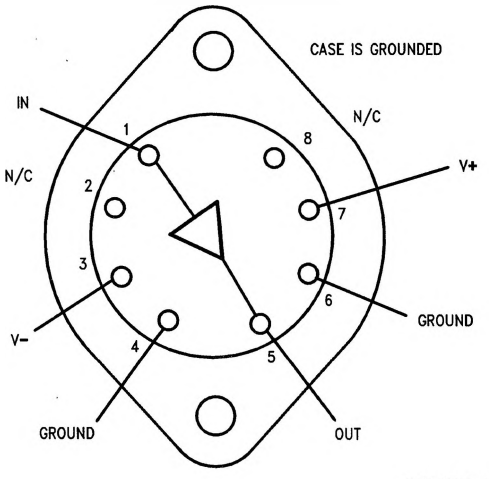
Metal Can Package (TO-3)



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Top View

Case is Electrically Tied to Pins 4 and 6 (Ground)

Order Number LH4012K or LH4012CK
See NS Package Number K08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V^+, $-V^-$)	40V
Maximum Power Dissipation (See Curves)	3W
Maximum Junction Temperature	175°C
Input Voltage	$\lvert V_{OUT} \pm V_{IN} \rvert < 3V$
Output Current, Continuous	±200 mA
Peak	±400 mA
Operating Temperature Range	
LH4012	−55°C to +125°C
LH4012C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD	TBD

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = R_L = 50\Omega$, $T_A = +25°C$, unless otherwise specified (Note 1)

Symbol	Parameter	Conditions	LH4012			Units (Max unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset		±20	±50 **±55**		mV
$\Delta V_{OS}/\Delta T$	Aver. Temp. Coeffic. of Output Offset Voltage	$T_{MIN} < T_A < T_{MAX}$	30			μV/°C
I_B	Input Bias Current (Note 4)		0.2	0.7		mA
A_V	Voltage Gain	$V_{IN} = \pm 10V$, $R_L = 1\ k\Omega$	0.98	0.95		V/V (Min)
A_V	Voltage Gain	$V_{IN} = \pm 10V$	0.93	0.9 **0.9**		V/V (Min)
C_{IN}	Input Capacitance		7			pF
R_{OUT}	Output Impedance	$V_{OUT} = \pm 10V$	2.3	4.5		Ω
V_O	Output Voltage Swing		11.4	10 **9**		V (Min)
PSRR	Power Supply Rejection Ratio		70			dB
LSA_V	Low Supply Voltage Gain	$V_S = \pm 5V$, $V_{IN} = \pm 2.5V$	0.92	0.85 **0.85**		V/V (Min)
LSV_O	Low Supply Output Voltage Swing	$V_S = \pm 5V$	3.4	2.5		V (Min)
I_S	Supply Current	$R_L = \infty$, $V_S = \pm 15V$	65	75 **80**		mA
LVI_S	Low Voltage Supply Current	$V_S = \pm 5V$	21	30		mA
P_D	Power Consumption	$R_L = \infty$, $V_S = \pm 15V$	1.95	2.25		W
P_D	Power Consumption	$R_L = \infty$, $V_S = \pm 5.0V$	0.21	0.3		W

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = R_L = 50\Omega$, $T_A = +25°C$, unless otherwise specified (Note 1)

Symbol	Parameter	Conditions	LH4012C			Units (Max unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset		±20	±50		mV
$\Delta V_{OS}/\Delta T$	Aver. Temp. Coeffic. of Output Offset Voltage	$T_{MIN} < T_A < T_{MAX}$	30			μV/°C
I_B	Input Bias Current (Note 4)		0.2	0.7		mA
A_V	Voltage Gain	$V_{IN} = \pm 10V$, $R_L = 1\ k\Omega$	0.98	0.95		V/V (Min)
A_V	Voltage Gain	$V_{IN} = \pm 10V$	0.93	0.9		V/V (Min)
C_{IN}	Input Capacitance		7			pF
R_{OUT}	Output Impedance	$V_{OUT} = \pm 10V$	2.3	4.5		Ω
V_O	Output Voltage Swing		11.4	10		V (Min)
PSRR	Power Supply Rejection Ratio		70			db (Min)
LSA_V	Low Supply Voltage Gain	$V_S = \pm 5V$, $V_{IN} = \pm 2.5V$	0.92	0.85		V/V (Min)
LSV_O	Low Supply Output Voltage Swing	$V_S = \pm 5V$	3.4	2.5		V (Min)
I_S	Supply Current	$R_L = \infty$, $V_S = \pm 15V$	65	75		mA
LVI_S	Low Voltage Supply Current	$V_S = \pm 5V$	21	30		mA
P_D	Power Consumption	$R_L = \infty$, $V_S = \pm 15V$	1.95	2.25		W
P_D	Power Consumption	$V_S = \pm 5.0V$	0.21	0.3		W

AC Electrical Characteristics

$T_J = +25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$ (Note 5)

Symbol	Parameter	Conditions	LH4012/LH4012C			Units (Max unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
SR	Slew Rate	$V_{IN} = 20\ V_{P-P}$	11500			V/μs
SSBW	Small Signal Bandwidth	$V_{IN} = 0.223$ Vrms	460	400		MHz (Min)
PBW	Power Bandwidth	$R_L = 50\Omega$, $V_{IN} = 10\ V_{P-P}$	230	200		MHz
	Phase Non-Linearity	BW = 1.0 MHz to 100 MHz	1			Degrees
	Rise Time	$V_{IN} = 20\ V_{P-P}$, $t_r = 500$ ps	1.2			ns
	Propagation Delay	$V_{IN} = 20\ V_{P-P}$	1			ns
	Harmonic Distortion	$V_{IN} = 10\ V_{P-P}$, f = 100 MHz	0.5			%

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4012C is −25°C to +85°C, and LH4012 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

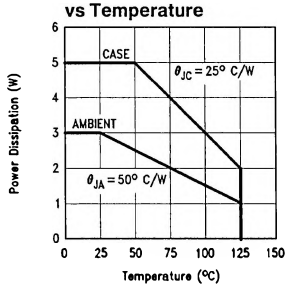
Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

Note 4: Specifications is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J = 25°C$.

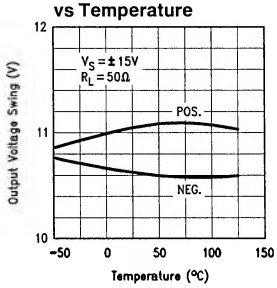
Note 5: For test circuits see *Figures 1, 2.*

Typical Performance Characteristics

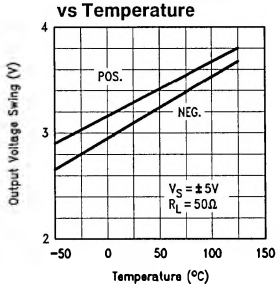
Power Dissipation vs Temperature



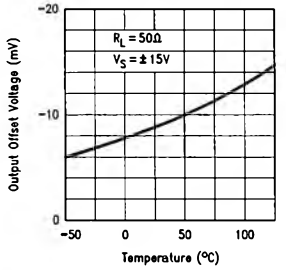
Output Voltage Swing vs Temperature



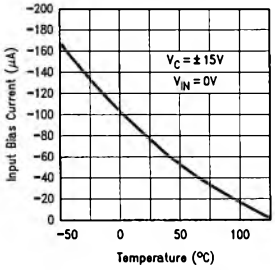
Output Voltage Swing vs Temperature



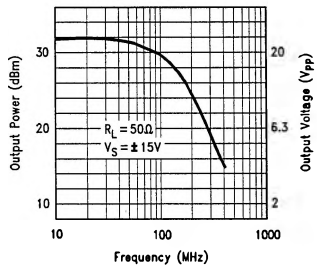
Output Offset Voltage vs Temperature



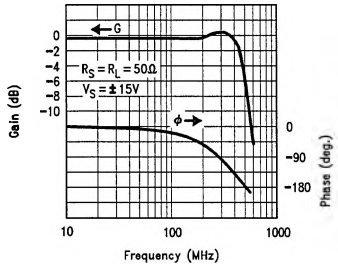
Input Bias Current vs Temperature



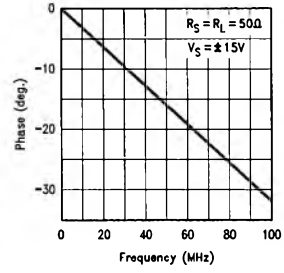
1 dB Compression vs Frequency



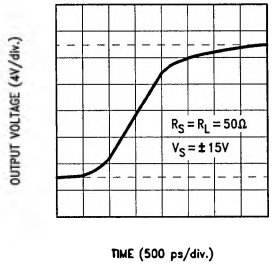
Gain and Phase vs Frequency



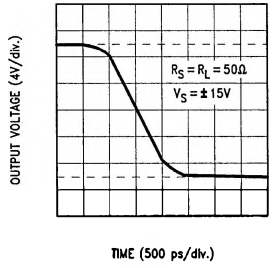
Phase vs Frequency



Rise Time



Fall Time



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Typical S Parameters $V_S = \pm 15V$, $R_L = R_S = 50\Omega$

f	S11		S21		S12		S22	
MHz	Mag	Ang	dB	Ang	dB	Ang	Mag	Ang
10	0.99	−3	5.27	−3.7	−60	54	0.87	176
100	0.99	−26	5.20	−33	−32	129	0.92	167
250	1.0	−82	5.15	−94	−14	69	0.94	138
500	0.80	−170	1.20	−182	−10	−22	0.60	96

Small Signal Bandwidth Test Circuit

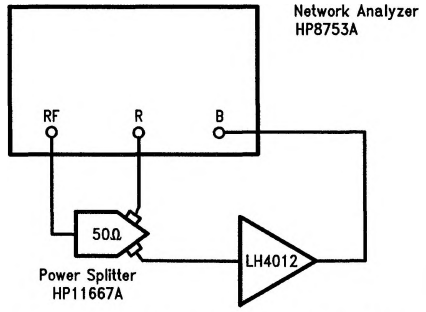


FIGURE 1. Small Signal Bandwidth Test Circuit

Power Bandwidth Test Circuit

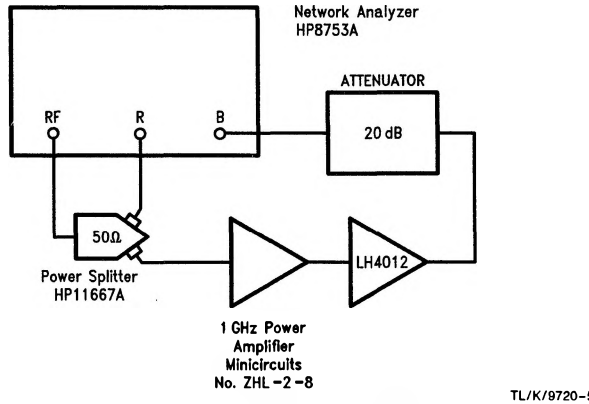


FIGURE 2. Power Bandwidth Test Circuit

Application Information

LAYOUT: Breadboards should have a solid ground plane and short point-to-point wiring. Do not use wire wrap boards or techniques. PC boards should have short connections and as much ground plane as possible.

It is best to have a layout without sockets, but sockets with shortpins and receptacles do not significantly degrade the performance.

The LH4012 has built-in 0.01 μF power supply bypass capacitors, but additional 4.7 μF tantalum capacitors are needed a maximum of 1" distant from the pins.

Input and output signals should be fed by coax or microstrip if the distances are more than a few inches to avoid impedance mismatches and resulting reflections. However, inside a feedback loop all connections should be short to avoid time delays and the associated phase shifts.

SOURCE RESISTANCE: The LH4012 is designed to work from a 50Ω or higher source impedance. If driven from a low source impedance, especially if it is inductive, a series input resistor is recommended that brings the source impedance to 50Ω, or instabilities could result.

CAPACITIVE LOADING: As with all buffers, capacitive loading can lead to instabilities. This can be minimized by reducing the phase angle of the load with a resistor either in series or in parallel with the capacitor or with a combination of both.

The charge current of the load capacitor,

$$C\ \text{Load} \times \frac{dV}{dT}$$

should be considered when the load current is checked against its absolute maximum limit.

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below the package power rating.

$P_{AC} + P_{DC} < P_{Pkg.\ Diss.}$

$P_{AC} = (V_{PP})^2 \times f \times C\ \text{load}$

$P_{DC} = (V^+ - V^-) \times I_S$

where V_{PP} = output voltage swing
f = Frequency

OPERATION WITHIN AN OP AMP LOOP: The device may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LM6161, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of the LH4012. The wide bandwidth and high slew rate of the LH4012 assures that the loop has the characteristics of the op amp and that additional frequency compensation is not required.

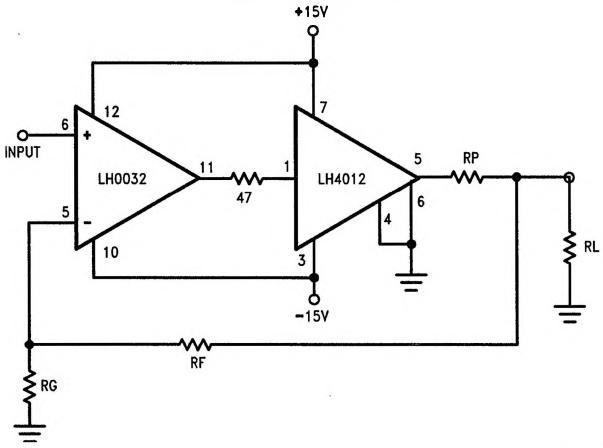
HEATSINK: In order to utilize the full drive capabilities of both the LH4012K or the LH4012CK, the device should be mounted with a heatsink, particularly for extended temperature operation.

VOLTAGE SWING: Input voltage is allowed to swing between positive and negative supply voltage levels, but it must be within $\pm$3V of the output voltage. If the voltage differential from input to output is greater than $\pm$3V the base-to-emitter diode of one of the input transistors will be broken down in reverse and the transistor will be degraded and could be destroyed.

SHORT CIRCUIT PROTECTION: In the interest of high performance the LH4012 has been designed without built-in protection. The simplest protection is a series resistor in the output. This approach has the advantage that input and output voltage of the buffer stay close together even during a shorted load. The main disadvantage is that the output voltage swing is reduced. Accuracy is normally not a problem, since the voltage drop across the protection resistor can be compensated for by more gain somewhere else in the circuit. This is especially true if the buffer is used within the feedback loop of an opamp.

Application Information (Continued)

Output Short Circuit Protection Using a Series Resistor



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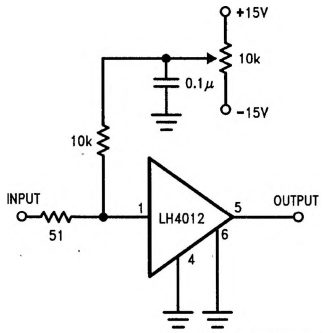
Offset Adjust



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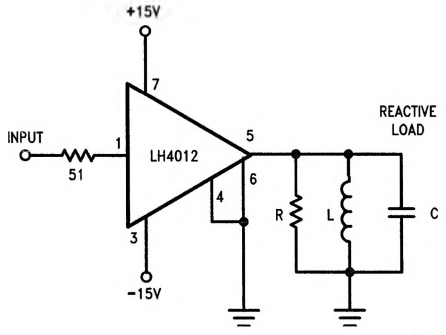
Isolation Buffer



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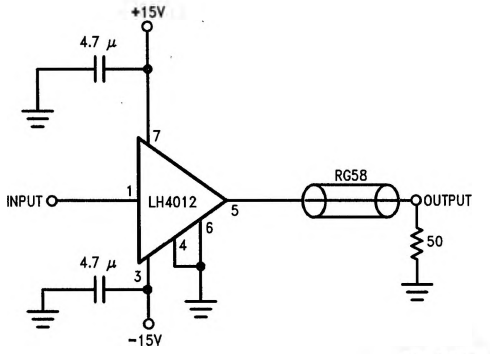
Coaxial Cable Driver



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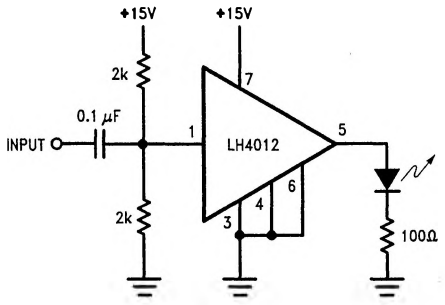
Application Information (Continued)

Laser Diode Transmitter



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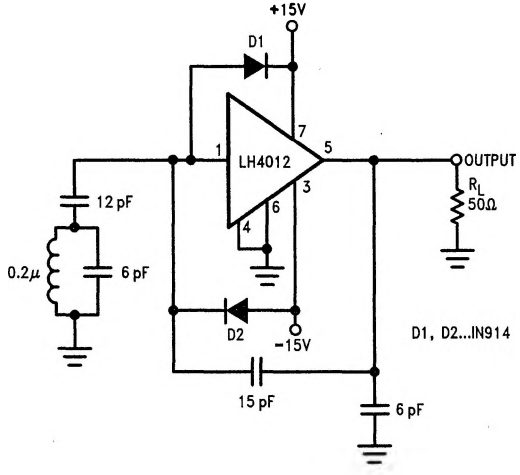
VHF Power Oscillator 100 MHz 1W



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