National Semiconductor

LH4033C/LH4063C Fast and Ultra Fast Buffer Amplifiers

General Description

The LH4033C and LH4063C are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH4033C will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500 V/μs. The LH4063C will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates of up to 6000 V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffer for driving reactive loads and high impedance input buffers for high speed ADCs and comparators. In addition, the LH4063C can continuously drive 50Ω coaxial cables or be used as a diddle yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH4033C and LH4063C are specified from −25°C to +85°C. The LH4033C is available in a 16-pin plastic DIP. The LH4063C is available in an 11-lead TO-220 package.

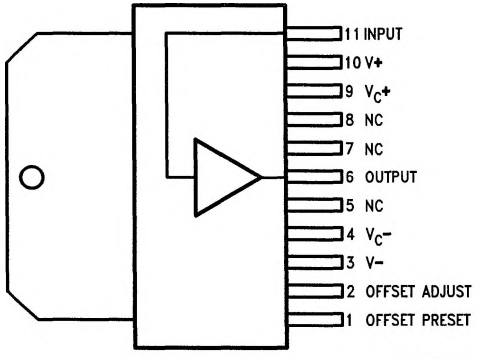
Features

- Fast (LH4063) 6000 V/μs
- Wide range single or dual supply operation
- Wide power bandwidth DC to 100 MHz
- High output drive ±10V with 50Ω load
- Low phase non-linearity 2°
- Fast rise times 2 ns
- High current gain 120 dB
- High input resistance $10^{10}\Omega$

Applications

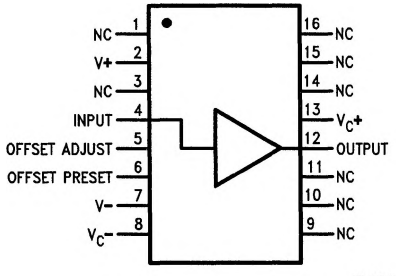
- High speed ATE
- Coaxial cable driver
- Isolation buffer
- High speed S/H amplifier
- High frequency filter
- Flash A/D buffer

Connection Diagrams



TL/K/10008–1

11-Lead TO-220
Order Number LH4063CT
See NS Package Number TA11A



TL/K/10008–2

16-Lead Molded Dual-In-Line Package
Order Number LH4033CN
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$) 40V

Maximum Power Dissipation (See Curves)
- LH4063C 5W
- LH4033C 1.5W

Maximum Junction Temperature 175°C

Input Voltage $\pm V_S$

Continuous Output Current
- LH4063C ±250 mA
- LH4033C ±100 mA

Peak Output Current
- LH4063C ±500 mA
- LH4033C ±250 mA

Operating Temperature Range
- LH4033C and LH4063C −25°C to +85°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) 300°C

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	Limits LH4033C Min	Limits LH4033C Typ	Limits LH4033C Max	Units
Output Offset Voltage	$R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ $R_S = 100\Omega$ (Note 2)		12	20 25	mV mV
Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3)		50	100	µV/°C
Input Bias Current	$V_{IN} = 0V$ $T_J = 25°C$ (Note 2) $T_A = 25°C$ (Note 4) $T_J = T_A = T_{MAX}$			500 5.0 20	pA nA nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0\ k\Omega$	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1\ k\Omega$	10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k$		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k$ $V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±12 ±9.0			V V
Supply Current	$V_{IN} = 0V$ (Note 5), No Load		21	24	mA
Power Consumption	$V_{IN} = 0V$ (No Load)		630	720	mW

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0\ k\Omega$ (Note 6)

Parameter	Conditions	Limits LH4033C Min	Limits LH4033C Typ	Limits LH4033C Max	Units
Slew Rate	$V_{IN} = \pm 10V$	1000	1400		V/µs
Bandwidth	$V_{IN} = 1.0\ V_{rms}$		100		MHz
Phase Non-Linearity	BW = 1.0 to 20 MHz		2.0		Degrees
Rise Time	$\Delta V_{IN} = 0.5V$		3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.5		ns
Harmonic Distortion	f > 1 kHz		<0.1		%

Note 1: LH4033C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs. temperature graph for expected values.

Note 3: LH4033C is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{max}.

Note 4: Measured in still air 7 minutes after application of Power. Guaranteed through correlated automatic pulse testing.

Note 5: Guaranteed through automatic pulse testing at $T_J = 25°C$.

Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	Limits LH4063C Min	Limits LH4063C Typ	Limits LH4063C Max	Units
Output Offset Voltage	$R_S \leq 100\ k\Omega$, $T_J = 25°C$ $R_L = 100\Omega$ (Note 2)		10	50 100	mV mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100\ k\Omega$		300		$\mu V/°C$
Input Bias Current	$T_J = 25°C$ (Note 2)		10	30 100	nA nA
Voltage Gain	$V_{IN} = \pm 10V$, $R_S = 100\ k\Omega$, $R_L = 1.0\ k\Omega$	0.94	0.96	1.0	V/V
	$V_{IN} = \pm 10V$, $R_S = 100\ k\Omega$, $R_L = 50\Omega$, $T_J = 25°C$	0.91	0.93	0.98	V/V
Input Capacitance	Case Shorted to Output		8.0		pF
Output Impedance	$V_{OUT} = \pm 10V$, $R_S \leq 100\ k\Omega$ $R_L = 50\Omega$		1.0	4.0	Ω
Output Current Swing	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$	0.2	0.25		Amps
Output Voltage Swing	$R_L = 50\Omega$	± 10	± 13		V
	$V_S = \pm 5.0V$, $R_L = 50\Omega$, $T_J = 25°C$	5.09	7.0		V_{P-P}
Supply Current	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$ (Note 3)		35	65	mA
	$V_S = \pm 5.0V$ (Note 3)		50		mA
Power Consumption	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		1.05	1.95	W
	$V_S = \pm 5.0V$		500		mW

AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_L = 50\Omega$ (Note 4), $R_S = 50\Omega$

Parameter	Conditions	Limits LH4063C Min	Limits LH4063C Typ	Limits LH4063C Max	Units
Slew Rate	$R_L = 1.0\ k\Omega$, $V_{IN} = \pm 10V$		6000		$V/\mu s$
	$V_{IN} = \pm 10V$, $T_J = 25°C$	2000	2400		$V/\mu s$
Bandwidth	$V_{IN} = 1.0\ V_{rms}$		200		MHz
Phase Non-Linearity	BW = 1.0 to 20 MHz		2.0		Degrees
Rise Time	$\Delta V_{IN} = 0.5V$		1.9		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		2.1		ns
Harmonic Distortion			<0.1		%

Note 1: LH4063C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

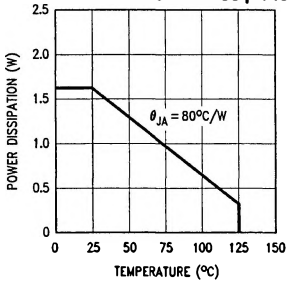
Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are $\pm 15V$, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 3: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

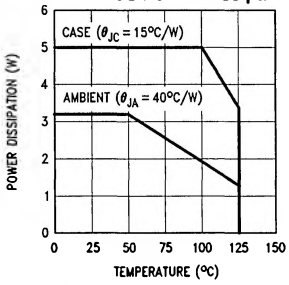
Note 4: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Typical Performance Characteristics

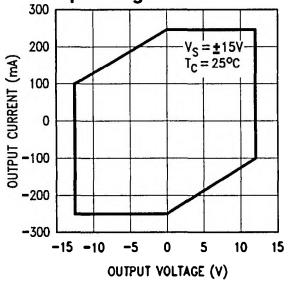
LH4033C Power Dissipation



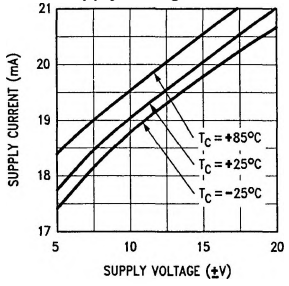
LH4063C Power Dissipation



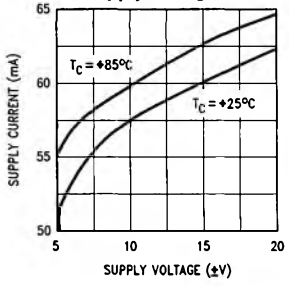
LH4063C DC Safe Operating Area



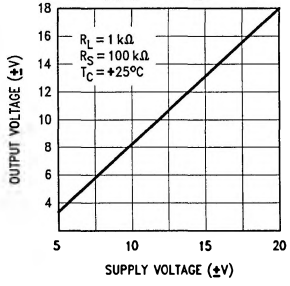
LH4033C Supply Current vs Supply Voltage



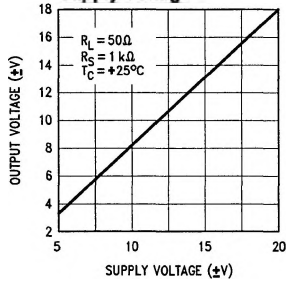
LH4063C Supply Current vs Supply Voltage



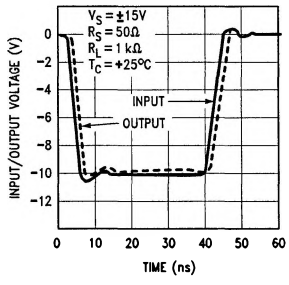
LH4033C Output Voltage vs Supply Voltage



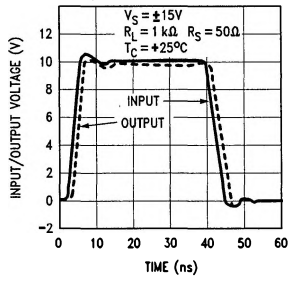
LH4063C Output Voltage vs Supply Voltage



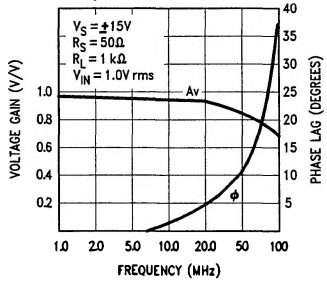
LH4033C Negative Pulse Response



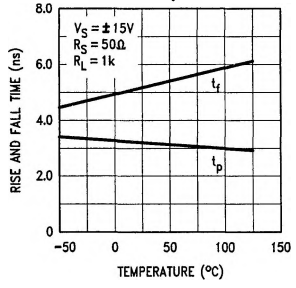
LH4033C Positive Pulse Response



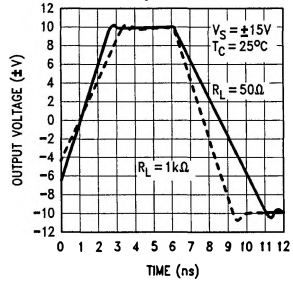
LH4033C Frequency Response



LH4033C Rise and Fall Time vs Temperature



LH4063C Large Signal Pulse Response



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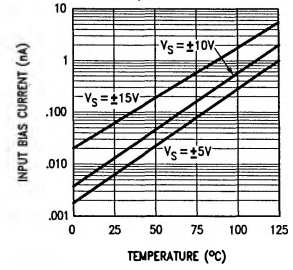
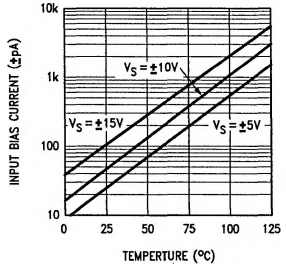
Typical Performance Characteristics (Continued)

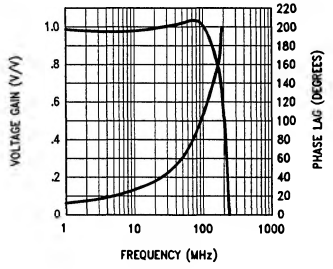
LH4033C Input Bias Current vs Temperature



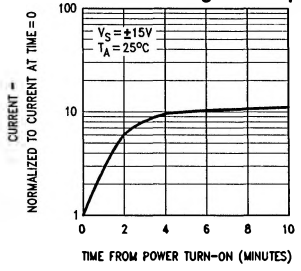
LH4063C Input Current vs Temperature



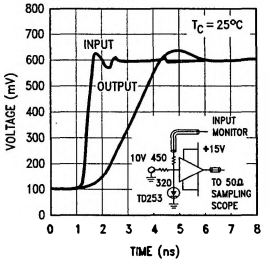
LH4063C Frequency Response



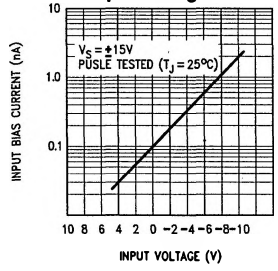
LH4033C Normalized Input Bias Current During Warm-Up



LH4063C Small Signal Rise Time



LH4033C Input Bias Current vs Input Voltage



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Application Hints

Recommended Layout Precautions: RF/video printed circuit board layout rules should be followed when using the LH4033C and LH4063C since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors.

Offset Voltage Adjustment: Both the LH4033C's and LH4063C's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 200Ω for the LH4033C or 1 kΩ for the LH4063C between the offset adjust pin and V^- as illustrated in *Figures 1* and *2*.

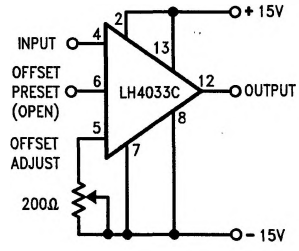

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FIGURE 1. Offset Zero Adjust for LH4033C

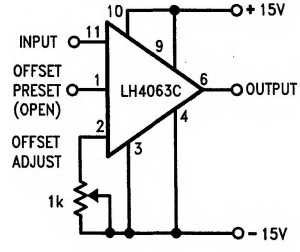

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FIGURE 2. Offset Zero Adjust for LH4063C

Application Hints (Continued)

Operation from Single or Asymmetrical Power Supplies: Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.005\,(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.99
V^+ = Positive supply voltage
V^- = Negative suply voltage

For the above example, ΔV_O would be -35 mV. This may be adjusted to zero by offset voltage adjustment described earlier. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the "typical applications" section.

Short Circuit Protection: In order to optimize transient response and output swing, output current limit has been omitted from the LH4033 and LH4063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in *Figures 3* and *4*. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for LH4033C
$I_{SC} \leq 250$ mA for LH4063C

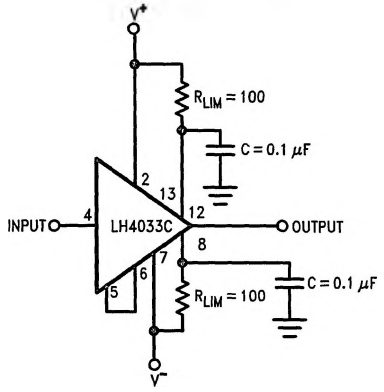

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FIGURE 3. LH4033C Using Resistor Current Limiting

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in *Figures 5, 6* and *7*. In *Figures 5* and *6*, the current sources are saturated during normal operation thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload. For *Figure 5*:

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\text{ mA}} = 10\Omega$$

In *Figure 6*, quad transistor arrays are used to minimize part count and:

$$R_{LIM} = \frac{V_{BE}}{1/3\,(I_{SC})} = \frac{0.6V}{1/3\,(200\text{ mA})} = 8.2\Omega$$

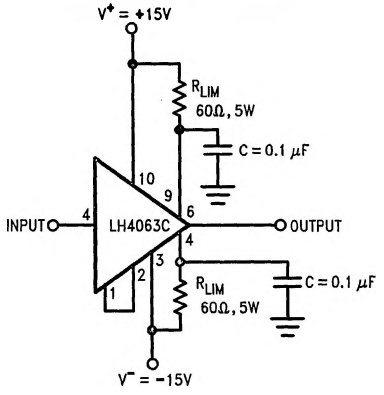

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FIGURE 4. LH4063C Using Resistor Current Limiting

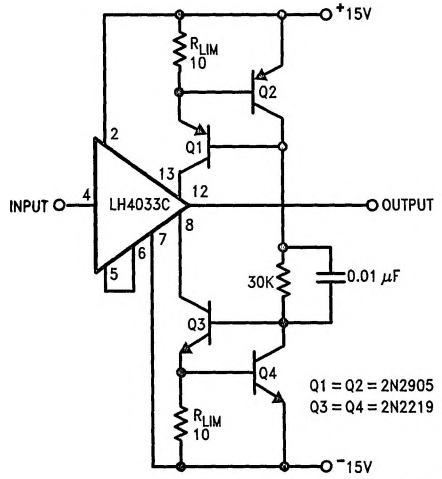

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FIGURE 5. LH4033C Current Limiting Using Current Sources

Application Hints (Continued)

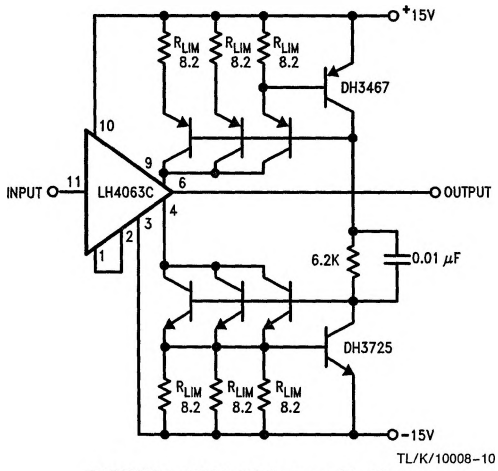

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FIGURE 6. LH4063C Current Limiting Using Current Sources

Capacitance Loading: Both the LH4033C and LH4063C are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from (CdV/dt) should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH4033C:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

and for the LH4063C:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below total package power rating:

$$P_{\substack{diss \\ pkg}} \geq P_{DC} + P_{AC}$$

$$\geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{P\text{-}P})^2 \times f \times C_L$$

where $V_{P\text{-}P}$ = Peak-to-peak output voltage swing
f = Frequency
C_L = Load Capacitance

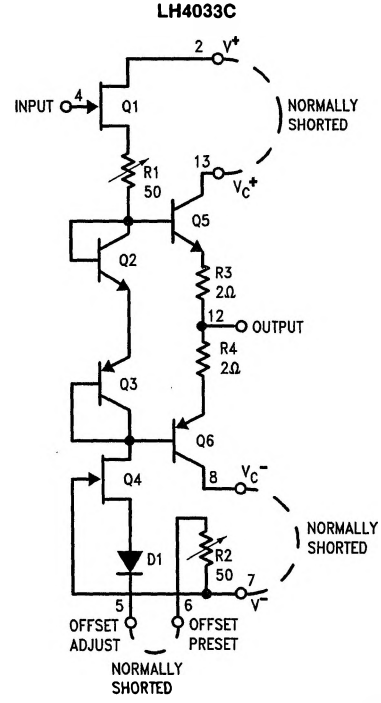
Operation Within an Op Amp Loop: Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LH0062, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH4033C. The wide bandwidths and high slew rates of the LH4033C and LH4063C assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

Hardware: In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation.

DESIGN PRECAUTION

Power supply bypassing is necessary to prevent oscillation with both the LH4033C and LH4063C in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within <¼" to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel for the LH4033C; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances. For the LH4063C, two 0.1 μF ceramic and one 4.7 μF solid tantalum capacitors in parallel will be necessary on each supply lead.

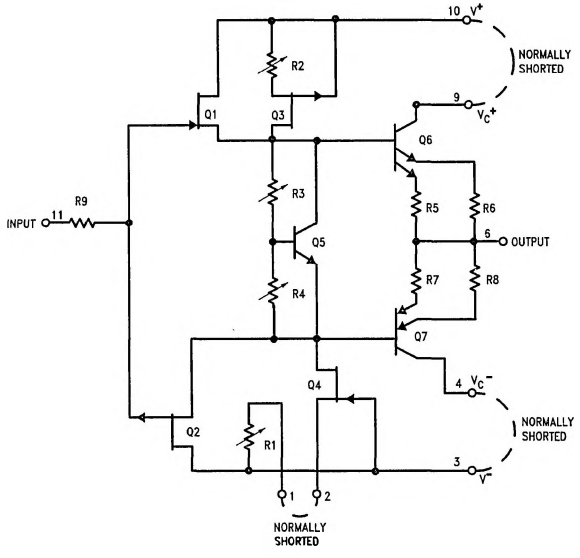
Schematic Diagrams



TL/K/10008–11

Schematic Diagrams (Continued)

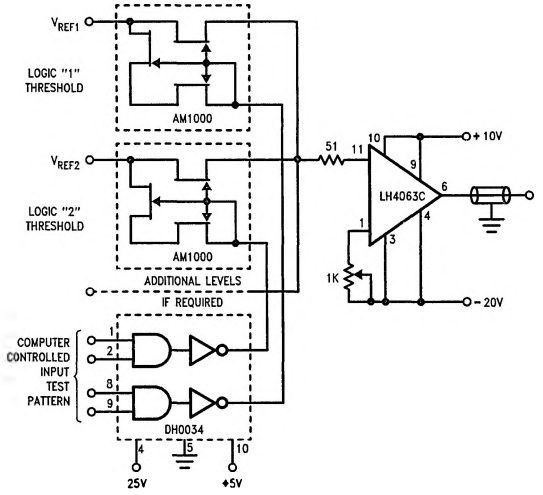
LH4063C



TL/K/10008–12

Typical Applications

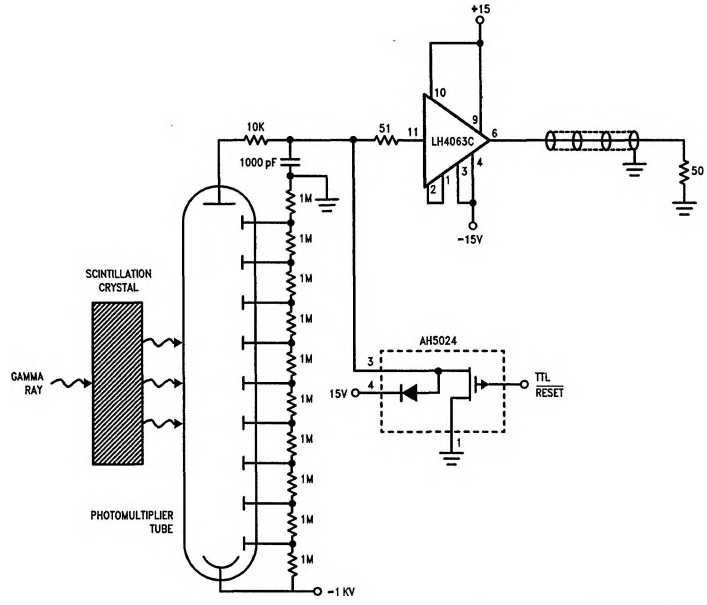
High Speed Automatic Test Equipment
Forcing Function Generator



TL/K/10008–13

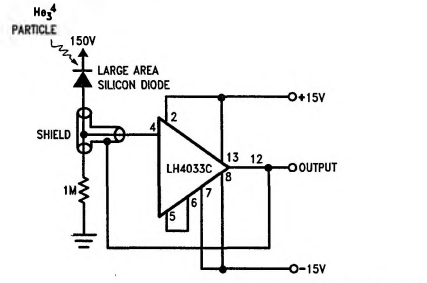
Typical Applications (Continued)

Gamma Ray Pulse Integrator



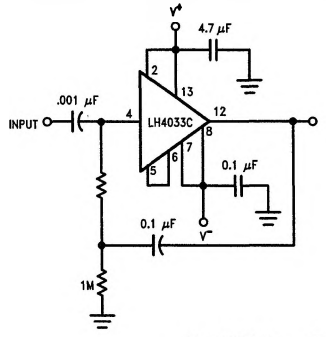
TL/K/10008–14

Nuclear Particle Detector



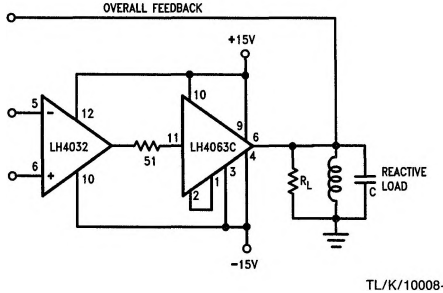
TL/K/10008–15

High Input Impedance AC Coupled Amplifier



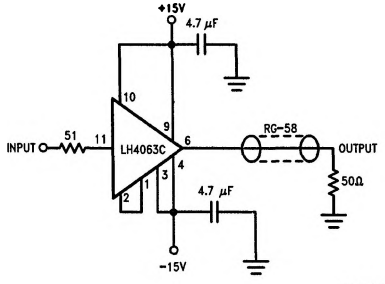
fH > 100 MHz TL/K/10008–16

Isolation Buffer



TL/K/10008–17

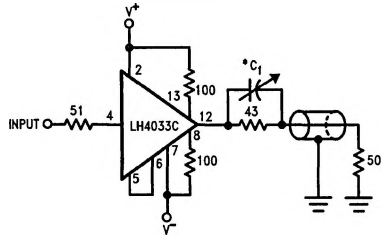
Coaxial Cable Driver



TL/K/10008–18

Typical Applications (Continued)

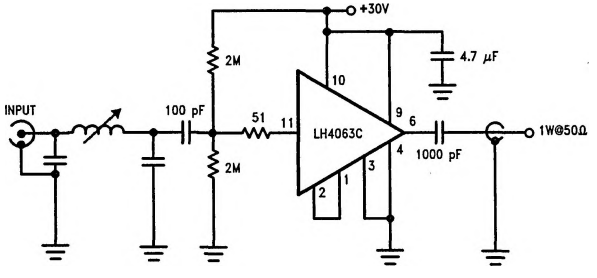
Coaxial Cable Driver



*Select C_1 For Optimum Pulse Response.

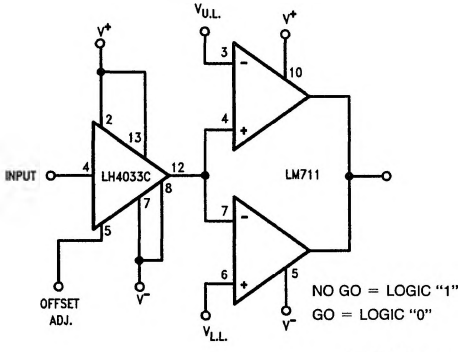
TL/K/10008-19

1W CW Final Amplifier



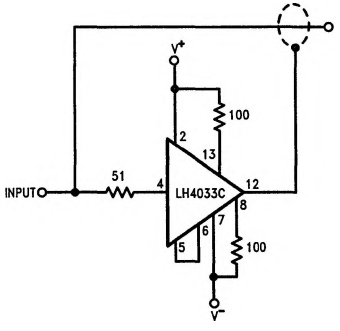
TL/K/10008-20

High Input Impedance Comparator With Offset Adjust



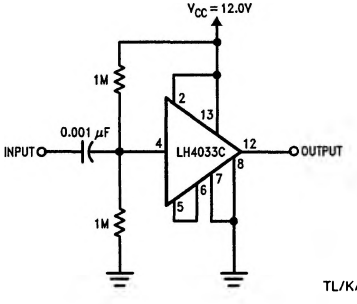
TL/K/10008-21

Instrumentation Shield/Line Driver



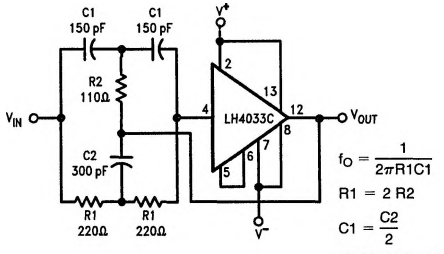
TL/K/10008-22

Single Supply AC Amplifier



TL/K/10008-23

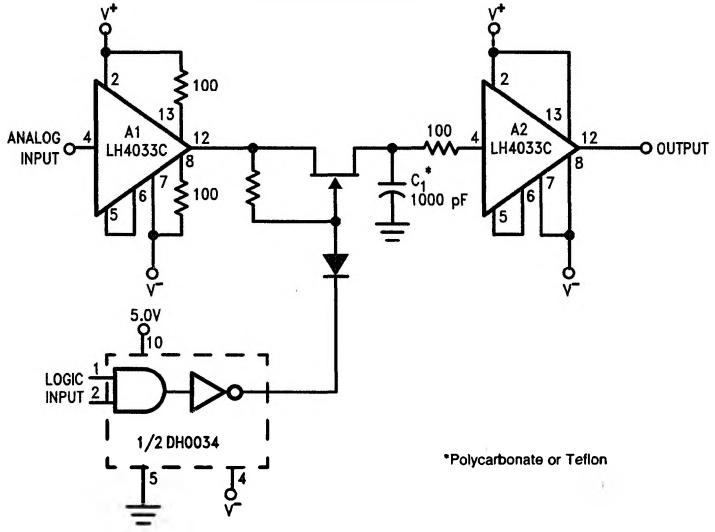
4.5 MHz Notch Filter



TL/K/10008-24

Typical Applications (Continued)

High Speed Sample & Hold



*Polycarbonate or Teflon

TL/K/10008–25