National Semiconductor

PRELIMINARY

LH4161A/LH4161/LH4161C High Speed Operational Amplifier

General Description

The LH4161 high-speed amplifier exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's new VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high-speed performance without the need for complex and expensive dielectric isolation.

In addition, they are precision laser trimmed to guarantee low offset voltage.

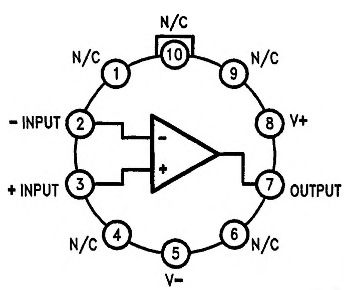
Features

- High slew rate 300 V/μs
- High unity gain freq 50 MHz
- Low supply current 5 mA
- Fast settling 120 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase 0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved, easy to apply
- Low offset voltage ±1 mV
- Pin compatible with LM6161

Applications

- Low differential gain and phase amplifier
- Fast pulse amplifier
- High frequency filters and oscillators

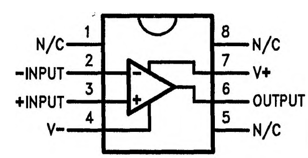
Connection Diagrams



TL/K/9767-1

Top View

Order Number LH4161AH, LH4161H or LH4161CH
See NS Package Number H10F



TL/K/9767-2

Top View

Order Number LH4161AJ, LH4161J or LH4161CJ
See NS Package Number J08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
CM Voltage	(V^+ − 0.7V) to (V^- − 7V)
Output Short Circuit to GND (Note 1)	Continuous
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range (Note 2)	
LH4161A/LH4161	−55°C to +125°C
LH4161C	−25°C to +85°C
Max. Junction Temperature	150°C
ESD Tolerance (Notes 8 and 9)	±700V
Operating Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LH4161A		LH4161		LH4161C		Units
			Tested Limit (Note 4)	**Design Limit (Note 5)**	**Tested Limit (Note 4)**	**Design Limit (Note 5)**	**Tested Limit (Note 4)**	**Design Limit (Note 5)**	
Input Offset Voltage		0.5	1 **3**		2 **5**		4	**6**	mV Max
Input Offset Voltage Average Drift		10							µV/°C
Input Bias Current		2	3 **6**		3 **6**		5	**6**	µA Max
Input Offset Current		150	350 **800**		350 **800**		1500	**1900**	nA Max
Input Offset Current Average Drift		0.4							nA/°C
Input Resistance	Differential	325							kΩ
Input Capacitance	A_V = +1 @ 10 MHz	1.5							pF
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 11)	750	550 **300**		550 **300**		400	**350**	V/V Min
	R_L = 10 kΩ	2900							V/V
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9 **+13.8**		+13.8	**+13.7**	V Min
		−13.2	−12.9 **−12.7**		−12.9 **−12.7**		−12.8	**−12.7**	V Min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9 **3.8**		3.8	**3.7**	V Min
		1.8	2.0 **2.2**		2.0 **2.2**		2.1	**2.2**	V Max
Common-Mode Rejection Ratio	−10V ≤ V_{CM} ≤ +10V	94	80 **74**		80 **74**		72	**70**	dB Min
Power Supply Rejection Ratio	±10V ≤ $V^\pm$ ≤ ±16V	90	80 **74**		80 **74**		72	**70**	dB Min
Output Voltage Swing	Supply = ±15V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**		+13.5 **+13.3**		+13.4	**+13.3**	V Min
		−13.4	−13.0 **−12.7**		−13.0 **−12.7**		−12.9	**−12.8**	V Min
	Supply = +5V and R_L = 2 kΩ (Note 6)	4.2	3.5 **3.3**		3.5 **3.3**		3.4	**3.3**	V Min
		1.3	1.7 **2.0**		1.7 **2.0**		1.8	**1.9**	V Max
Output Short Circuit Current	Source	65	30 **20**		30 **20**		30	**25**	mA Min
	Sink	65	30 **20**		30 **20**		30	**25**	mA Min
Supply Current		5.0	6.5 **6.8**		6.5 **6.8**		6.8	**6.9**	mA Max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LH4161A		LH4161		LH4161C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@F = 20 MHz	50	40		40		35		MHz
	Supply = ±5V	35							Min
Slew Rate	A_V = +1 (Note 10)	300	225		225		200		V/µs Min
	Supply = ±5V	200							V/µs
Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5							MHz
Settling Time	10V Step to 0.1% A_V = −1, R_L = 2 kΩ	120							ns
Phase Margin		45							Deg
Differential Gain	NTSC, A_V = +4	<0.1							%
Differential Phase	NTSC, A_V = +4	0.1							Deg
Input Noise Voltage	f = 10 kHz	15							$nV/\sqrt{Hz}$
Input Noise Current	f = 10 kHz	1.5							$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the cerdip (J) package is 125°C/W, and the TO-5 (H) package is 155°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_A = T_J$ = 25°C with supply voltage = ±15V, V_{CM} = 0V, and R_L ≥ 100 kΩ. **Boldface** limits apply over the range listed under "Operating Temperature Range" with $T_A = T_J$ in the "Absolute Maximum Ratings" section.

Note 4: Guaranteed and 100% production tested. These limits are used to calculate outgoing AQL levels.

Note 5: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 6: For single supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V.

Note 7: C_L ≤ 5 pF.

Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS} and Noise).

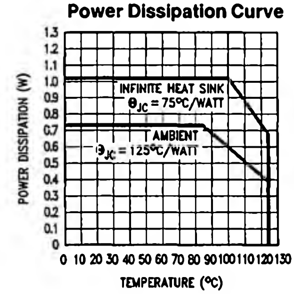
Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 10: V_{IN} = 8V step. For supply = ±5V, V_{IN} = 5V step.

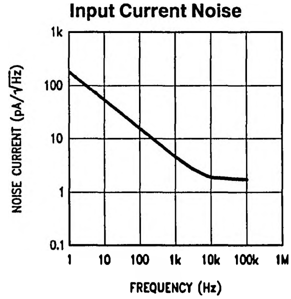
Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Typical Performance Characteristics R_L = 10k and T_A = 25°C unless otherwise specified

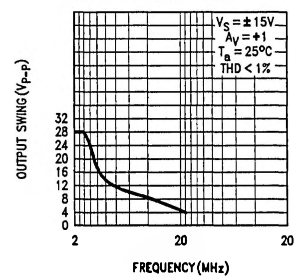
Power Dissipation Curve



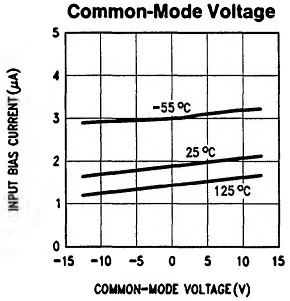
Input Current Noise



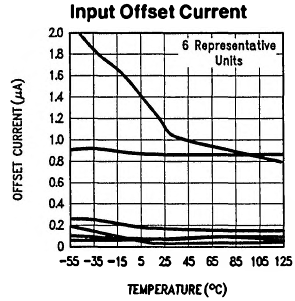
Power Bandwidth



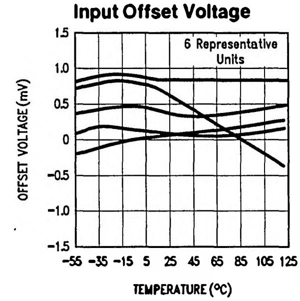
Bias Current vs Common-Mode Voltage



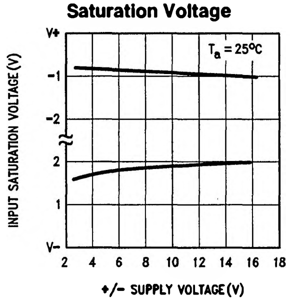
Input Offset Current



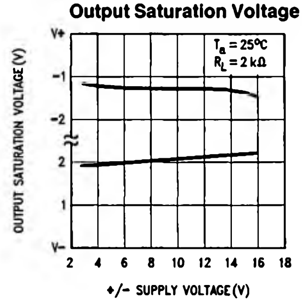
Input Offset Voltage



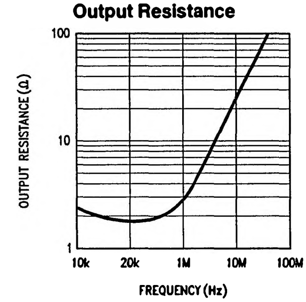
Common-Mode Input Saturation Voltage



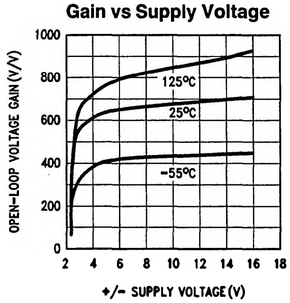
Output Saturation Voltage



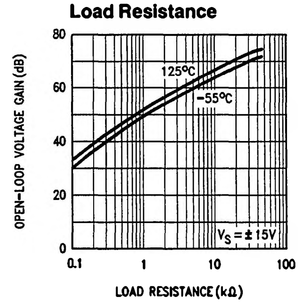
Output Resistance



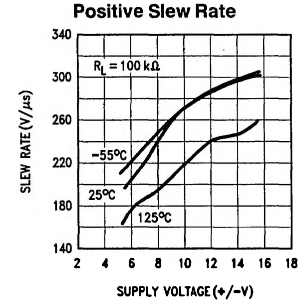
Gain vs Supply Voltage



Voltage Gain vs Load Resistance



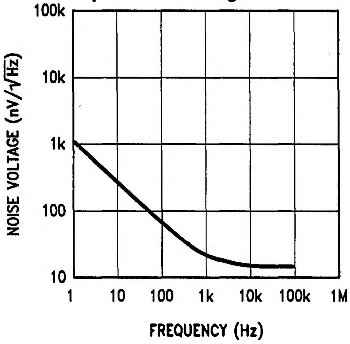
Positive Slew Rate



TL/K/9767–5

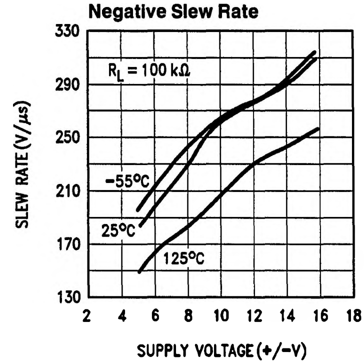
Typical Performance Characteristics (Continued)

Input Noise Voltage



TL/K/9767-4

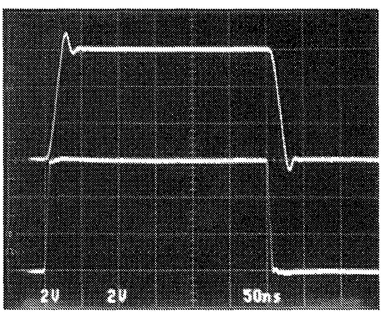
Negative Slew Rate



TL/K/9767-6

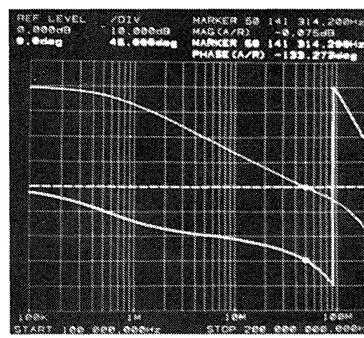
Typical AC Characteristics

Step Response; $A_V = +1$



TL/K/9767-7

Gain & Phase; $A_V = +100$



TL/K/9767-8

Application Hints

The LH4161 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains.

The LH4161 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). However, load capacitance on the LH4161 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth.

Power supply bypassing is not as critical for the LH4161 as it is for other op amps in its speed class. However, bypassing will improve the stability and transient response of the LH4161, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 to 10 μF of tantalum may be required for extra noise reduction.

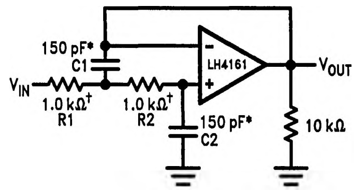
Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling from one pin, input or lead to another, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

Typical Applications

1 MHz Low-Pass Filter

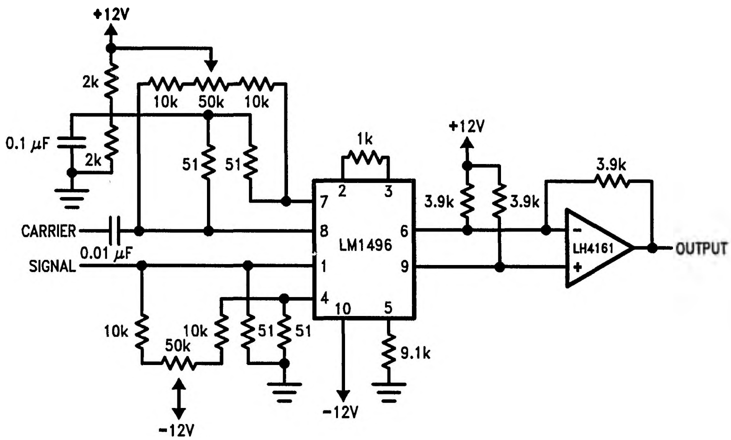
$f_C = 1/2\pi\sqrt{(R_1R_2C_1C_2)}$



† 1% tolerance
*Matching determines filter precision

TL/K/9767-9

Modulator with Differential-to-Single-Ended Converter



TL/K/9767-10