National Semiconductor Corporation

LM1038 Dual Four-Channel Analog Switch

General Description

The LM1038 is a dual, electronically controlled, four-channel analog switch with an internal muting facility.

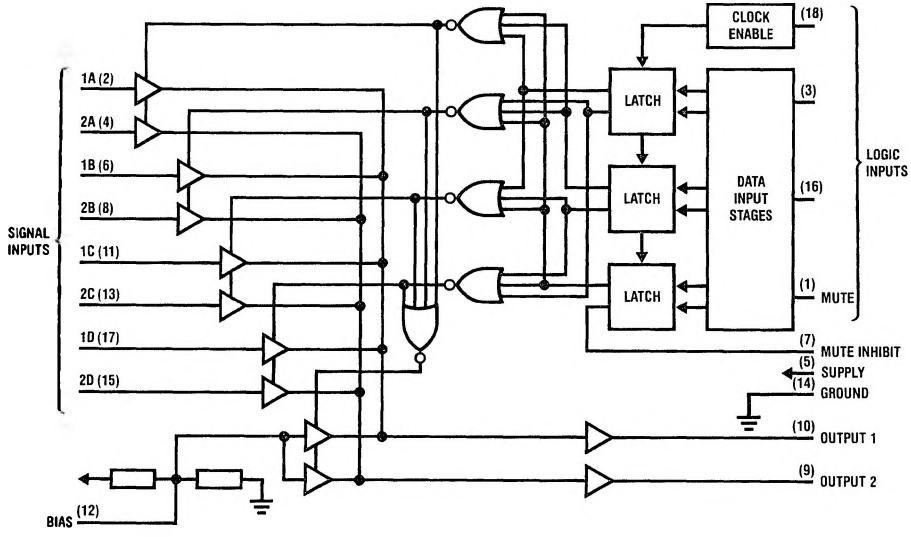
Its features make it ideal for stereo source selection in audio equipment and for use in a wide range of industrial, automotive, multiplexing or sampling applications.

Channel selection is achieved via two logic data pins with clock enabled latches. Muting is also selectable under clock control.

Features

- Wide supply voltage range, 5V-28V
- Low distortion, 0.04% typical
- High input impedance
- Low output impedance
- TTL compatible control Inputs
- Very low control current
- 2 control pins accept BCD input pulses
- Clock enable input may be strobed from a bus

Block Diagram



TL/H/5200–1

Order Number LM1038N
See NS Package Number N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

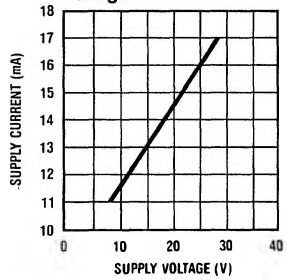
Supply Voltage	28V
Pin 7 Input Current	5 mA
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (Note 1)	1.3W
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics $V_S = 12V$, $T_A = 25°C$.

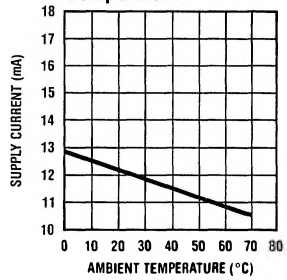
Parameter	Conditions	Typ	Tested Limit (Note 7)	Design Limit (Note 8)	Units (Limits)
Supply Voltage			28		$V_{(max)}$
Supply Voltage				5	$V_{(min)}$
Supply Current	$V_{SUPPLY} = 12V$	12	17		$mA_{(max)}$
	$V_{SUPPLY} = 28V$	17	28		$mA_{(max)}$
Voltage Gain		0	±0.7		dB
Signal Handling (Notes 2, 6)	$V_{SUPPLY} = 12V$	3.0	2.8		$Vrms_{(MIN)}$
Small-Signal Bandwidth		300			kHz
Distortion THD	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	0.04	0.1		$\%_{(max)}$
Noise Voltage at Output (Note 3)	CCIR/ARM $R_S = 0\Omega$	5		20	$\mu V_{(max)}$
Channel Separation (Note 4)	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−95		−70	$dB_{(min)}$
Relative Output in Muted State	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−90	−70		$dB_{(min)}$
Output Impedance		10			Ω
Signal Input Impedance		30			MΩ
Logic Low Input Level				0.8	$V_{(max)}$
Logic High Input Level				2.0	$V_{(min)}$
Logic High Input Level				V_{SUPPLY}	$V_{(max)}$

Typical Performance Characteristics ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

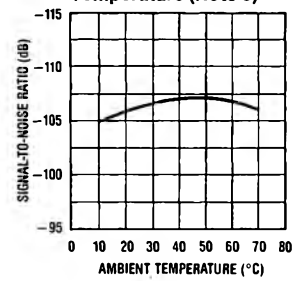
Supply Current vs Supply Voltage



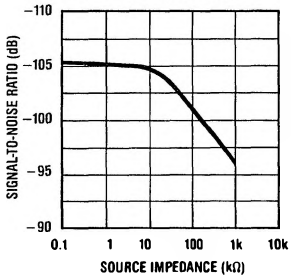
Supply Current vs Temperature



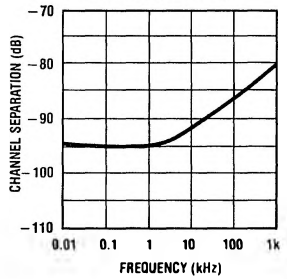
Signal-to-Noise vs Temperature (Note 3)



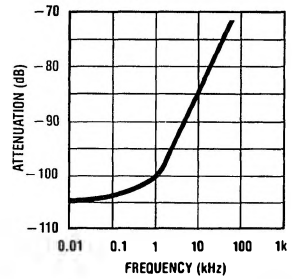
Signal-to-Noise vs Source Impedance (Note 3)



Channel Separation vs Frequency (Note 4)



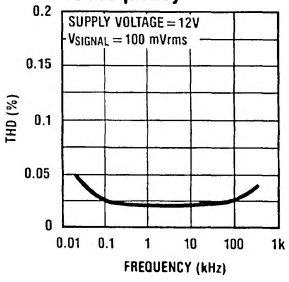
Attenuation of Unselected Inputs vs Frequency (Note 5)



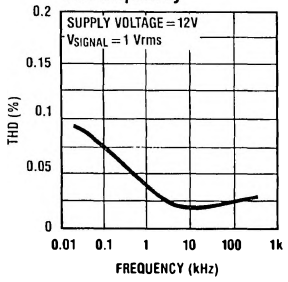
TL/H/5200–2

Typical Performance Characteristics (Continued) ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

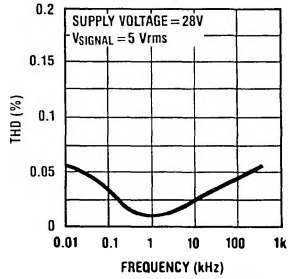
Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency

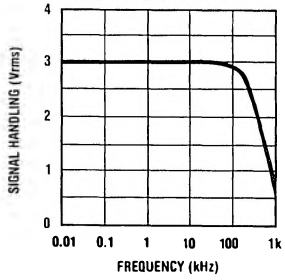


Total Harmonic Distortion vs Frequency



TL/H/5200–3

Signal Handling vs Frequency (Note 6)



TL/H/5200–4

Note 1: Above $T_A = 25°C$ derate based on T_J max = 150°C and $\theta_{JA} = 90°C/W$.

Note 2: The instantaneous maximum voltage difference between any two input pins of one channel is 9.6V. Voltages in excess of this level may cause increased distortion and degraded channel separation.

Note 3: Gaussian noise, monitored over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz, and an average responding meter. Signal-to-noise ratios are referenced to a 1 Vrms input signal.

Note 4: The level of output signal of a selected undriven amplifier with respect to the output level of a selected driven amplifier. For test purposes, signal is applied to only one input and all other inputs are decoupled to eliminate stray pick-up through external components. Channel separation is then defined as the ratio of signal levels of the two output pins.

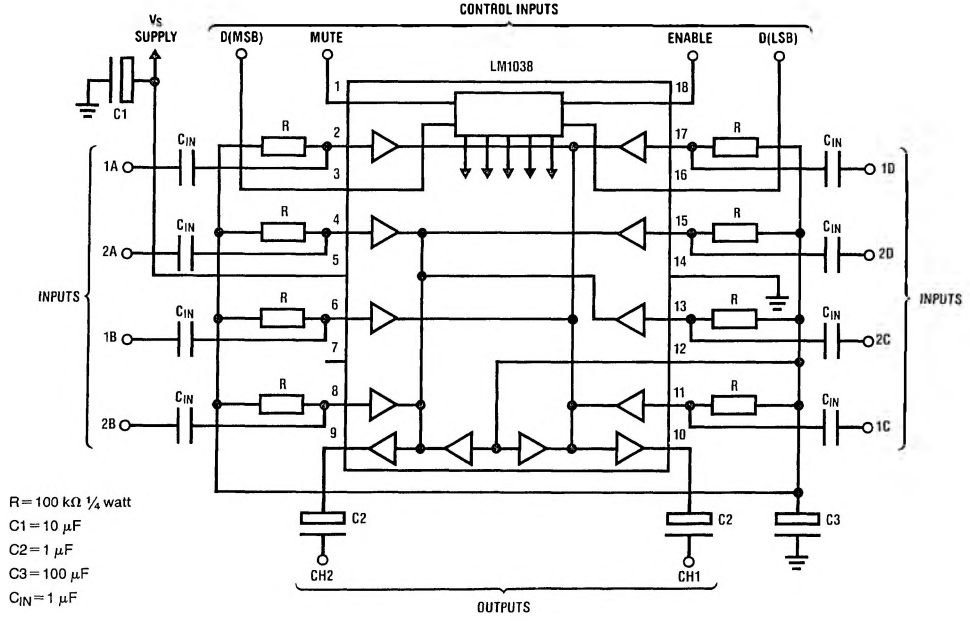
Note 5: For test purposes, signals are connected to three unselected input pins of one channel group and all other inputs are decoupled to eliminate stray pick-up through external components.

Note 6: Supply voltage 12V; signal handling defined at 1% distortion, 1 kHz.

Note 7: Guaranteed and 100% production tested.

Note 8: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Application



R = 100 kΩ ¼ watt
C1 = 10 μF
C2 = 1 μF
C3 = 100 μF
C_{IN} = 1 μF

TL/H/5200–5

Truth Table

Logic Inputs				Input Pin Selected	
Latch Enable Pin 18	Mute Pin 1	Channel Select Data Pin 3	Pin 16	Output 1 Pin 10	Output 2 Pin 9
1	0	0	0	D Pin 17	D Pin 15
1	0	0	1	A Pin 2	A Pin 4
1	0	1	0	B Pin 6	B Pin 8
1	0	1	1	C Pin 11	C Pin 13
1	1	X	X	Pin 12 Mute Bias	
0	X	X	X	Inputs Previously Selected are Retained	

Low (0) < 0.8V
High (1) > 2.0V, up to V_{SUPPLY}

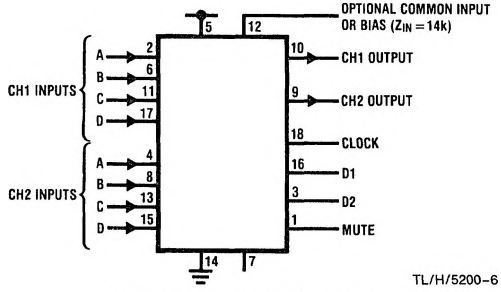
Pin Function Description

Device Pins	Description
Pin 1—Mute	A high level on this input will select the muted condition (outputs = pin 12 voltage) if the latch enable input is low provided pin 7 (mute enable) is open.
Pin 3—Channel Address (MSB) Pin 16—Inputs (LSB)	Binary information on these pins selects the required channel if the mute select input, pin 1, is low.
Pin 18—Latch Enable	With a high level on this pin the data on the channel select pins controls the channel enabled. When the input is low the channel select data is latched. The mute input pin 1 is also controlled by this input. A minimum enable pulse width of typically 3 μs is required.
Pins 2, 6, 11, 17—Inputs for Output 1 (Pin 10) Pins 4, 8, 13, 15—Inputs for Output 2 (Pin 9)	Two sets of four high impedance channel inputs for the connection of signals to be switched.
Pin 12—Mute Bias Level	The DC level at this pin is applied to the outputs when the mute input, pin 1, is activated. The level is internally set by a 25 kΩ and 33 kΩ potential divider to 0.6 V_S. This level may be adjusted by means of external resistors. Pin 12 may also be used as an additional common signal input.
Pin 7—Mute Inhibit	This is a current input and any control current into this pin must be externally limited to 5 mA maximum. With this pin open the mute input, pin 1, is enabled. With a current into this pin the mute facility is disabled and with no signal channel selected the output emitter-followers are disabled.
Pin 9—Output 2 Pin 10—Output 1	These are common output pins for each channel. There are three possible output conditions: 1) Signal selected from 1 of 4 inputs. 2) Mute level output. 3) Device not selected—internal 6 kΩ pull-down resistors to ground.
Pin 5	Positive supply voltage.
Pin 14	Negative or ground supply voltage.

Application Hints

The basic circuit arrangement with minimum external components for use with DC coupled signals is shown in *Figure 1*. This arrangement may be used in a normal signal selection system or in the feedback path of DC coupled amplifiers for example to make a simple dual programmable power supply. By switching feedback connections dual programmable gain or frequency response amplifiers may be obtained.

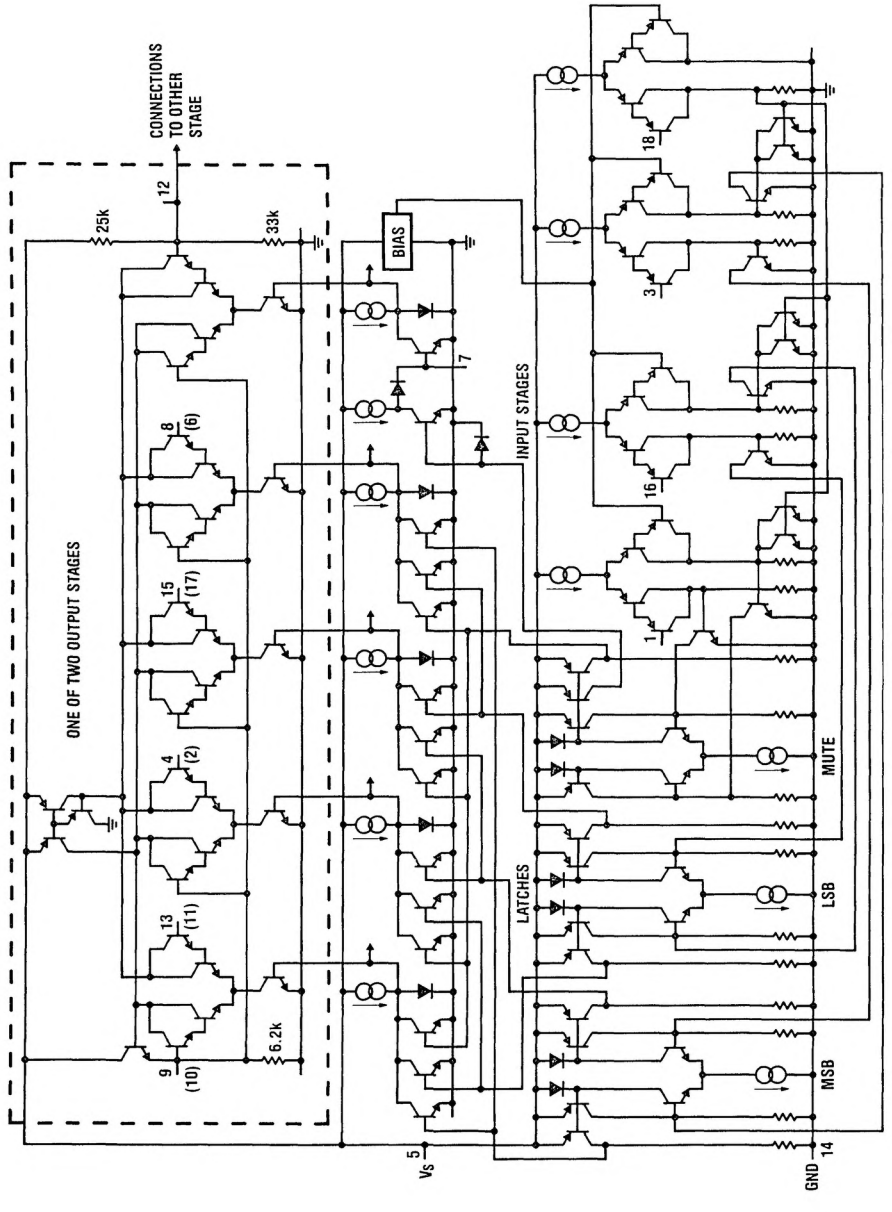
For switching between signal sources in stereo systems the LM1038 may be connected as shown in the typical application circuit. The input bias is obtainable from pin 12 or an alternative source may be used. If split supply operation is required, pin 12 may be grounded and the signals referenced to ground.



DC coupled signals $1.2V < V_{IN} < V_S - 1V$

FIGURE 1

Equivalent Schematic Diagram



TL/H/5200–7