LOW POWER LOW OFFSET VOLTAGE QUAD COMPARATORS

Check for Samples: LM139AQML, LM139QML

FEATURES

- **Available With Radiation Ensured**
  - **Total Ionizing Dose 100 krad(Si)**
  - **ELDRS Free 100 krad(Si)**
- **Wide Supply Voltage Range**
- **LM139/139A Series 2 to 36 V_{DC} or ±1 to ±18 V_{DC}**
- **Very Low Supply Current Drain (0.8 mA) — Independent of Supply Voltage**
- **Low Input Biasing Current: 25 nA**
- **Low Input Offset Current: ±5 nA**
- **Offset Voltage: ±1 mV**
- **Input Common-mode Voltage Range Includes GND**
- **Differential Input Voltage Range Equal to the Power Supply Voltage**
- **Low Output Saturation Voltage: 250 mV at 4 mA**
- **Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS Logic Systems**

ADVANTAGES

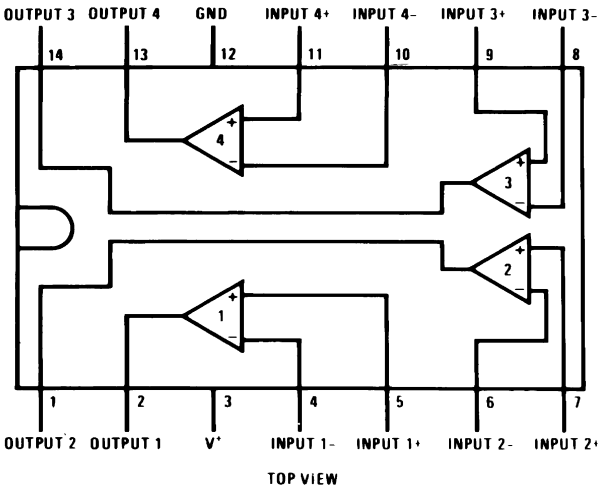
- **High Precision Comparators**
- **Reduced V_{OS} Drift Over Temperature**
- **Eliminates Need for Dual Supplies**
- **Allows Sensing Near GND**
- **Compatible with all Forms of Logic**
- **Power Drain Suitable for Battery Operation**

DESCRIPTION

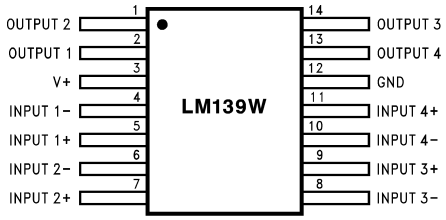
The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM139/LM139A is a distinct advantage over standard comparators.

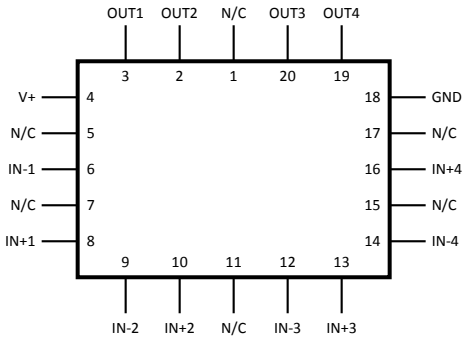
Connection Diagrams



Dual-In-Line Package
See Package Number J(R-GDIP-14)



See Package Number NAD0014B, NAC0014A



See Package Number NAJ002A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

			LM139 / LM139A
Supply Voltage, V^+			36 V_{DC} or ±18 V_{DC}
Differential Input Voltage(2)			36 V_{DC}
Input Voltage			−0.3 V_{DC} to +36 V_{DC}
Input Current (V_{IN} < −0.3 V_{DC})(3)			50 mA
Power Dissipation(4)(5)			
LCCC			1250 mW
CDIP			1200 mW
CLGA (NAD)			680 mW
CLGA (NAC)			680 mW
Sink Current (approx)(6)			20mA
Output Short-Circuit to GND(7)			Continuous
Storage Temperature Range			-65°C ≤ T_A ≤ +150°C
Maximum Junction Temperature (T_J)			+150°C
Lead Temperature (Soldering, 10 seconds)			300°C
Operating Temperature Range			-55°C ≤ T_A ≤ +125°C
Thermal Resistance	θ_{JA}	LCCC (Still Air)	100°C/W
		LCCC (500LF / Min Air flow)	73°C/W
		CDIP (Still Air)	103°C/W
		CDIP (500LF / Min Air flow)	65°C/W
		CLGA (NAD) (Still Air)	183°C/W
		CLGA (NAD) (500LF / Min Air flow)	120°C/W
		CLGA (NAC) (Still Air)	183°C/W
		CLGA (NAC) (500LF / Min Air flow)	120°C/W
	θ_{JC}	LCCC	28°C/W
		CDIP	23°C/W
		CLGA (NAD)	23°C/W
		CLGA (NAC)	23°C/W
Package Weight (typical)	LCCC		470mg
	CDIP		2,190mg
	CLGA (NAD)		460mg
	CLGA (NAC)		410mg
ESD rating(8)			600V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensured specific performance limits. For ensured specifications and test conditions, see, the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC}below the magnitude of the negative power supply, if used) (at 25°C).

(3) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°)C.

(4) The low bias dissipation and the ON-OFF characteristics of the outputs keeps the chip dissipation very small (P_D ≤ 100mW), provided the output transistors are allowed to saturate.

(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (Package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} — T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(6) SMD 5962–8773901 only

(7) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

(8) Human Body model, 1.5 KΩ in series with 100 pF

Recommended Operating Conditions

Supply Voltage	5.0 V_{DC} to +30 V_{DC}
Ambient Operating Temperature Range	−55°C ≤ T_A ≤ +125°C

Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LM133 883 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			2.0	mA	1, 2, 3
	Supply Current	+V = 30V, R_L = Infinity			2.0	mA	1, 2, 3
V_{IO}	Input Offset Voltage	+V = 30V		-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V		-5.0	5.0	mV	1
		+V = 30V, V_{CM} = 28.0V		-9.0	9.0	mV	2, 3
				-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
CMRR	Common Mode Rejection Ratio	+V = 30V, V_{CM} = 0V to 28.5V		60		dB	1
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V		60		dB	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	See (1)	-100	-1.0	nA	1
			See (1)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
I_{CEX}	Output Leakage Current	+V = 30V, V_O = 30V			1.0	µA	1, 2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V		6.0		mA	1
V_{Sat}	Saturation Voltage	I_{Sink} = 4mA			400	mV	1
					700	mV	2, 3
A_V	Voltage Gain	+V = 15V, R_L ≥ 15ΩK, V_I = 1V to 11V		50		V/mV	1

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

LM133 883 Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{CM}	Common Mode Voltage Range	+V = 30V	See (2)	0	V^+ - (1.5)	V	1
			See (2)	0	V^+ - (2.0)	V	2, 3
V_{Diff}	Differential Input Voltage	+V = 30V, -V = 0V, $+V_I$ = 36V, $-V_I$ = 0V	See (3)		500	nA	1, 2, 3
		+V = 30V, -V = 0V, $+V_I$ = 0V, $-V_I$ = 36V	See (3)		500	nA	1, 2, 3

(2) Parameter ensured by V_{IO} tests
(3) The value for V_{Diff} is not data logged during Read and Record.

LM139 883 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	9
		V_{OD} = 50mV			0.8	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	9
		V_{OD} = 50mV			0.8	µS	9

LM139A SMD 5962–8773901 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	+V = 30V, R_L = Infinity			3.0	mA	1, 2, 3
		R_L = Infinity			3.0	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, $-V_I$ = 0V, $+V_I \geq$ 1V, V_O = 30V			0.5	µA	1
					1.0	µA	2, 3
V_{Sat}	Saturation Voltage	$I_{Sink} \leq$ 4mA, $-V_I$ = 1V, $+V_I$ = 0V			400	mV	1
					700	mV	2, 3
I_{Sink}	Output Sink Current	$V_O \geq$ 1.5V, $-V_I$ = 1V, $+V_I$ = 0V		6.0		mA	1
V_{IO}	Input Offset Voltage	R_S = 0Ω		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, R_S = 0Ω		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28V, V_O = 1.4V, R_S = 0Ω		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
$\pm I_{IB}$	Input Bias Current	V_O = 1.5V	See (1)	-100	-1.0	nA	1
			See (1)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V		70		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	+V = 30V, V_{CM} = 0V to 28V, $R_L \geq$ 15KΩ		70		dB	1, 2, 3
A_V	Voltage Gain	+V = 15V, $R_L \geq$ 15KΩ, V_O = 1V to 11V		50		V/mV	4
				25		V/mV	5, 6

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

LM139A SMD 5962–8773901 Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{CM}	Common Mode Voltage Range	+V = 30V	See (2)	0	V^+ - (2.0)	V	1, 2, 3
		+V = 5V	See (2)	0	V^+ - (2.0)	V	1, 2, 3

(2) Parameter ensured by V_{IO} tests

LM139A SMD 5962–8773901 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV, R_L = 5.1KΩ			5.0	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV, R_L = 5.1KΩ			2.5	µS	9

LM139A 883, QMLV & RH, SMD 5962–9673801 Electrical Characteristics DC Parameters (1) (2)

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			2.0	mA	1, 2, 3
		+V = 30V, R_L = Infinity			2.0	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, V_O = 30V			1.0	µA	1, 2, 3
V_{Sat}	Saturation Voltage	I_{Sink} = 4mA			400	mV	1
					700	mV	2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V		6.0		mA	1
V_{IO}	Input Offset Voltage			-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-2.0	2.0	mV	1
		+V = 30V, V_{CM} = 28.0V, V_O = 1.5V		-4.0	4.0	mV	2, 3
± I_{Bias}	Input Bias Current	V_O = 1.5V	See (3)	-100	-1.0	nA	1
			See (3)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V		60		dB	1
CMRR	Common Mode Rejection Ratio	+V = 30V, V_{CM} = 0V to 28.5V		60		dB	1
A_V	Voltage Gain	+V = 15V, R_L ≥ 15KΩ, V_O = 1V to 11V		50		V/mV	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the “Post Radiation Limits” table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.

(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019, condition D, MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect. Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics, except as listed in the “Post Radiation Limits” table. Radiation end point limits for the noted parameters are ensured for only the conditions as specified in MIL-STD-883, Method 1019, condition D.

(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

LM139A 883, QMLV & RH, SMD 5962–9673801 Electrical Characteristics DC Parameters(1)(2) (continued)

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{CM}	Common Mode Voltage Range	+V = 30V	See(4) See(5)	0	V^+ - (1.5)	V	1
			See(4) See(5)	0	V^+ - (2.0)	V	2, 3
V_{Diff}	Differential Input Voltage	+V = 30V, -V =0V, $+V_I$ = 36V, $-V_I$ = 0V	(6)		500	nA	1, 2, 3
		+V = 30V, -V = 0V, $+V_I$ = 0V, $-V_I$ = 36V	(6)		500	nA	1, 2, 3

(4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ −1.5V for Subgroup 1, or V^+ −2.0V for Subgroup 2 & 3. Either or both inputs can go to +30 V_{DC} without damage, independent of the magnitude of V^+.
(5) Parameter ensured by V_{IO} tests
(6) The value for V_{Diff} is not data logged during Read and Record.

LM139A 883, QMLV & RH, SMD 5962–9673801 Electrical Characteristics AC Parameters(1)(2)

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	4
		V_{OD} = 50mV			0.8	µS	4
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	4
		V_{OD} = 50mV			0.8	µS	4

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the “Post Radiation Limits” table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.
(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019, condition D, MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect. Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics, except as listed in the “Post Radiation Limits” table. Radiation end point limits for the noted parameters are ensured for only the conditions as specified in MIL-STD-883, Method 1019, condition D.

LM139A 883, QMLV & RH, SMD 5962–9673801 Electrical Characteristics DC Parameters Delta Values

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V
Deltas required for S-Level, MLS (as specified on Internal Processing instructions (IPI)), and QMLV product at Group B, Subgroup 5.

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			-1.0	1.0	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	See(1)	-15	15	nA	1
I_{IO}	Input Offset Current	V_O = 1.5V		-10	+10	nA	1

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

LM139A 883, QMLV & RH, SMD 5962–9673801 Electrical Characteristics DC/AC Parameters 50K Post Rad Limits +25°C(1)

The following conditions apply, unless otherwise specified.
DC: +V = 5V, V_{CM} = 0V
AC: +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 5V, V_{CM} = 0		-2.5	2.5	mV	1
		+V = 30V, V_{CM} = 0		-2.5	2.5	mV	1
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-2.5	2.5	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	See(2)	-110	-1.0	nA	1
t_{RLH}	Response Time	V_{OD} (Overdrive) = 50mV			0.9	µS	4

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the “Post Radiation Limits” table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.
(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

LM139A 883, QMLV & RH, SMD 5962–9673801 Electrical Characteristics DC/AC Parameters 100K Post Rad Limits +25°(1)(2)

The following conditions apply, unless otherwise specified.
DC: +V = 5V, V_{CM} = 0V
AC: +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 5V, V_{CM} = 0		-4.0	4.0	mV	1
		+V = 30V, V_{CM} = 0		-4.0	4.0	mV	1
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-4.0	4.0	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	See(3)	-110	-1.0	nA	1
t_{RLH}	Response Time	V_{OD} (Overdrive) = 50mV			1.0	µS	4

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the “Post Radiation Limits” table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.
(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019, condition D, MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect. Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics, except as listed in the “Post Radiation Limits” table. Radiation end point limits for the noted parameters are ensured for only the conditions as specified in MIL-STD-883, Method 1019, condition D.
(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

TYPICAL PERFORMANCE CHARACTERISTICS

LM139, LM139A

Supply Current

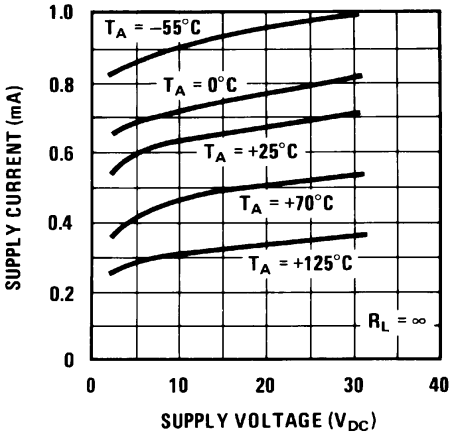


Figure 1.

Input Current

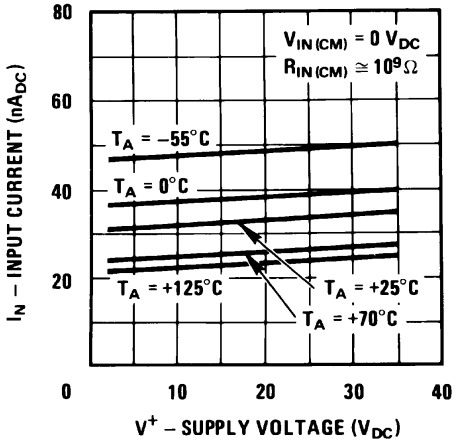


Figure 2.

Output Saturation Voltage

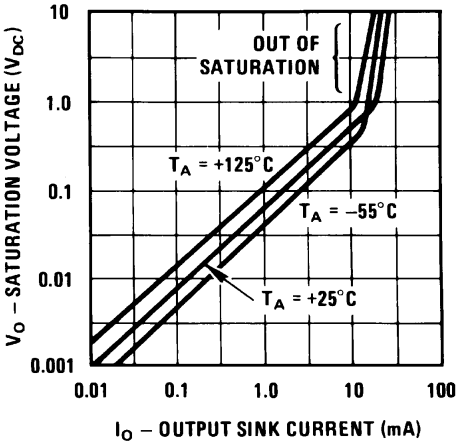


Figure 3.

Response Time for Various Input Overdrives —Negative Transition

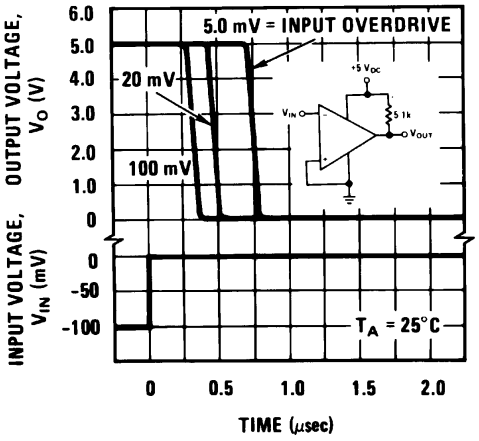


Figure 4.

Response Time for Various Input Overdrives —Positive Transition

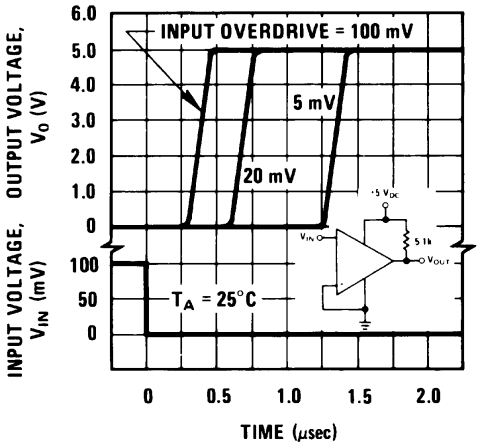


Figure 5.

APPLICATION HINTS

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be tied to the negative supply.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the Typical Applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications

(V^+ = 5.0 V_{DC})

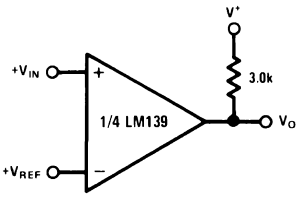


Figure 6. Basic Comparator

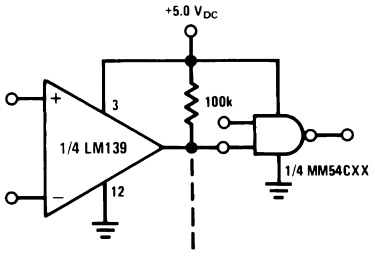


Figure 7. Driving CMOS

(V^+ = 5.0 V_{DC})

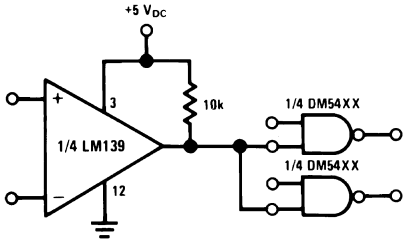


Figure 8. Driving TTL

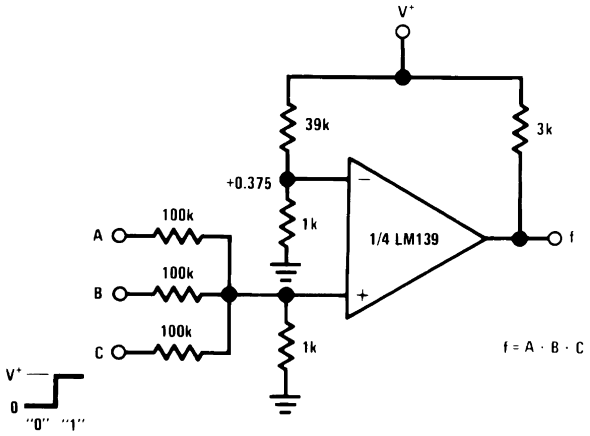


Figure 9. AND Gate

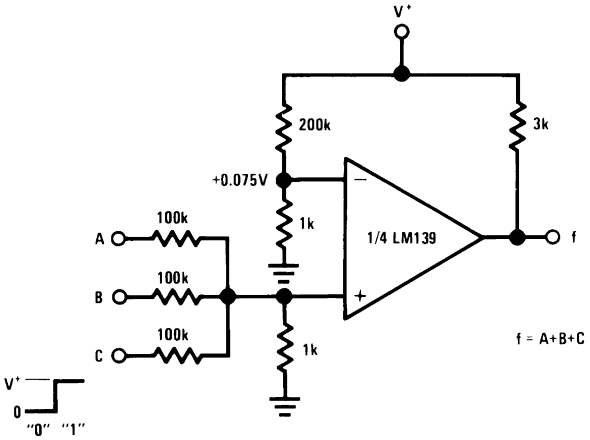


Figure 10. OR Gate

Typical Applications

(V^+= 15 V_{DC})

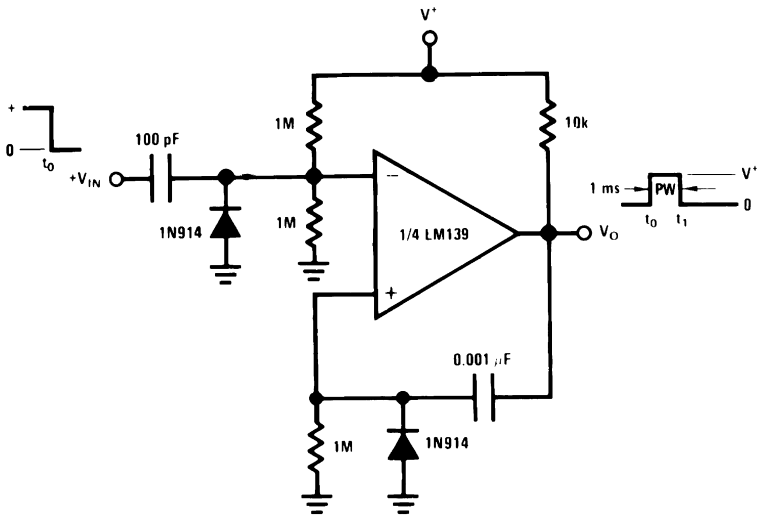


Figure 11. One-Shot Multivibrator

(V^+= 15 V_{DC})

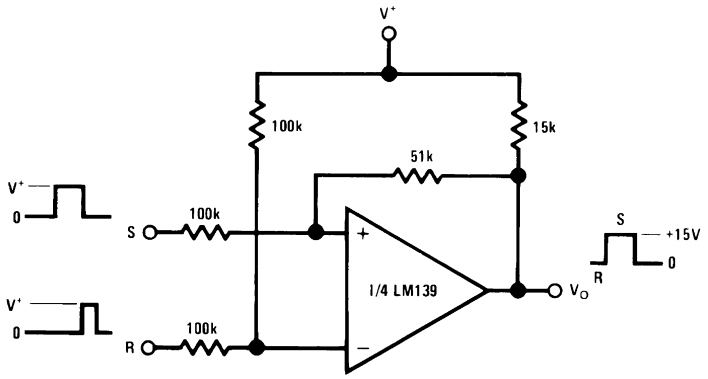


Figure 12. Bi-Stable Multivibrator

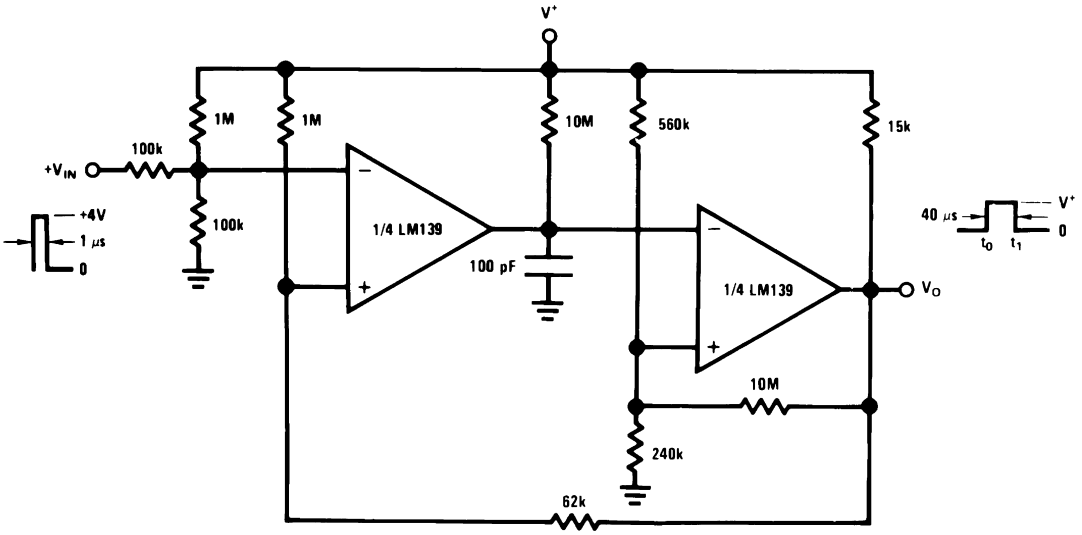


Figure 13. One-Shot Multivibrator with Input Lock Out

(V^+= 15 V_{DC})

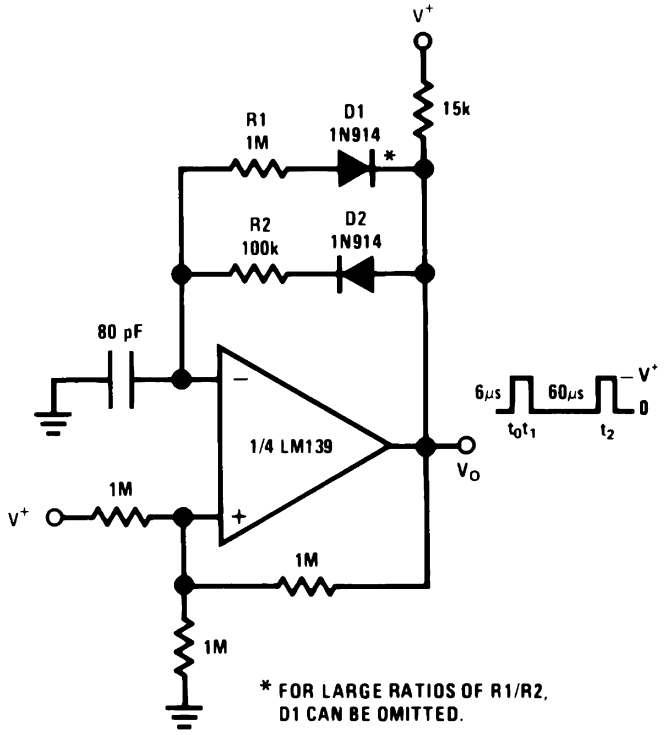


Figure 14. Pulse Generator

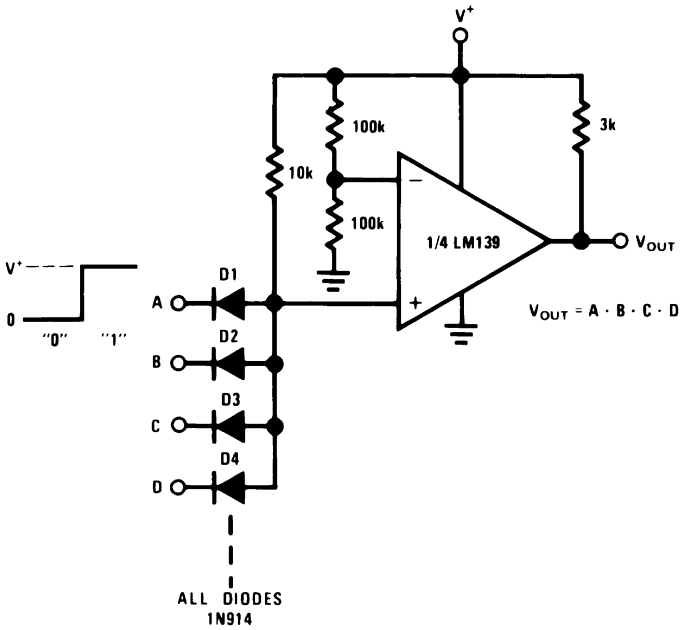


Figure 15. Large Fan-In AND Gate

(V^+= 15 V_{DC})

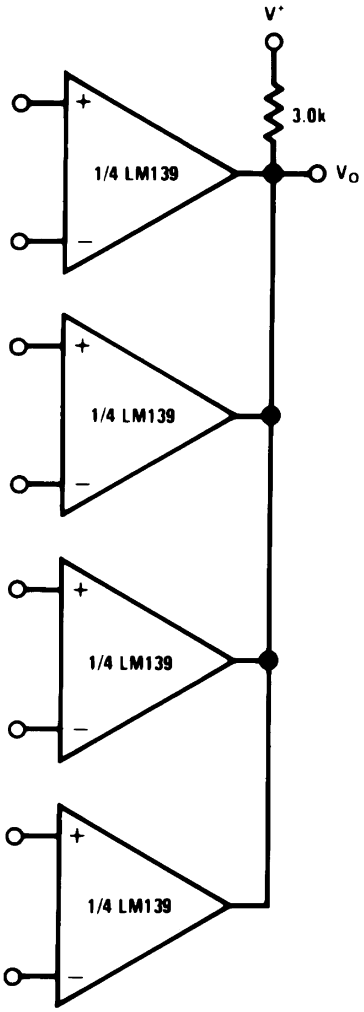


Figure 16. ORing the Outputs

(V^+= 15 V_{DC})

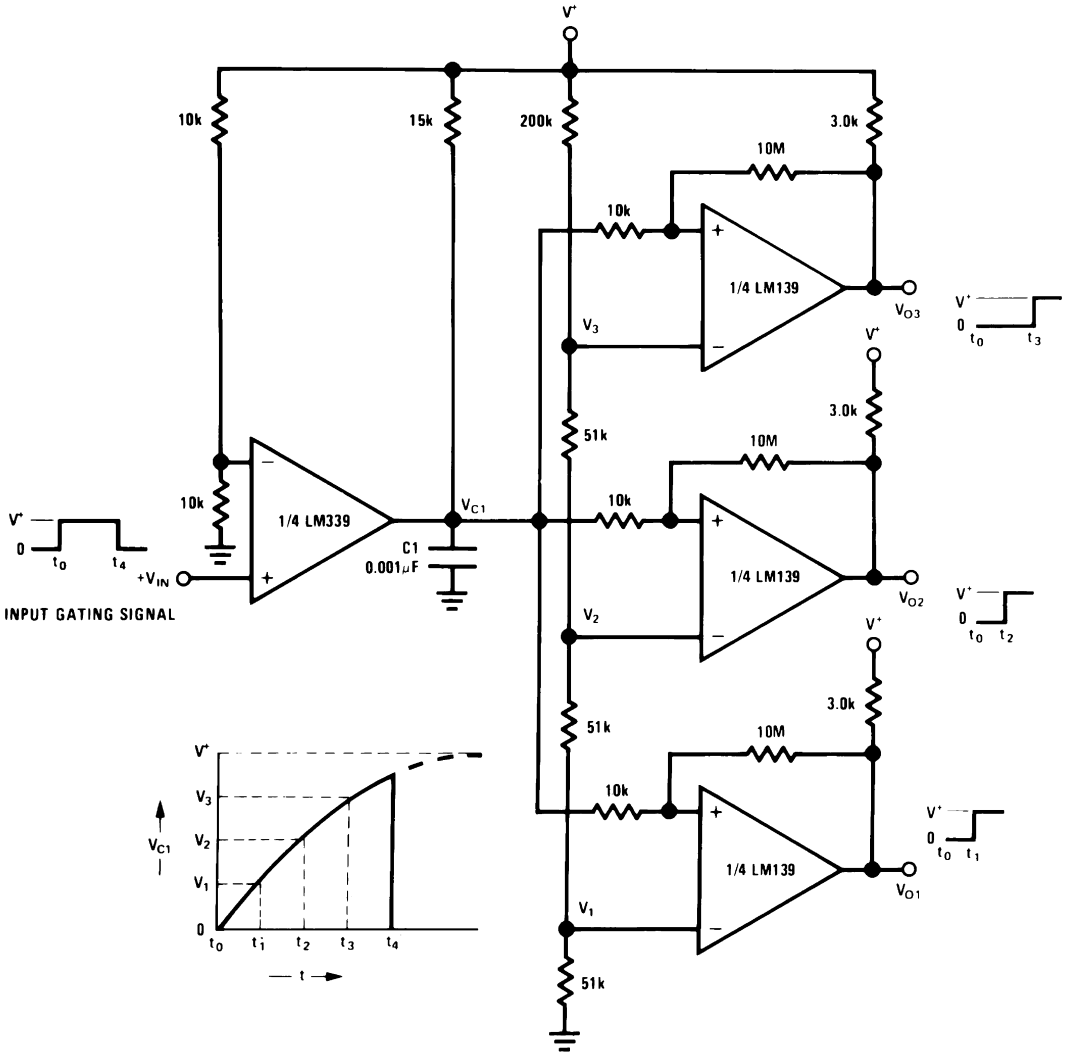


Figure 17. Time Delay Generator

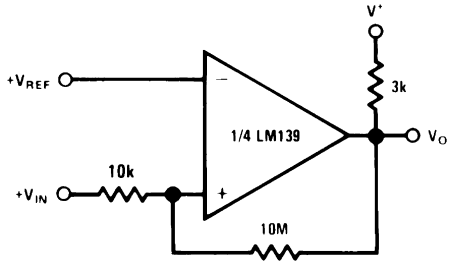


Figure 18. Non-Inverting Comparator with Hysteresis

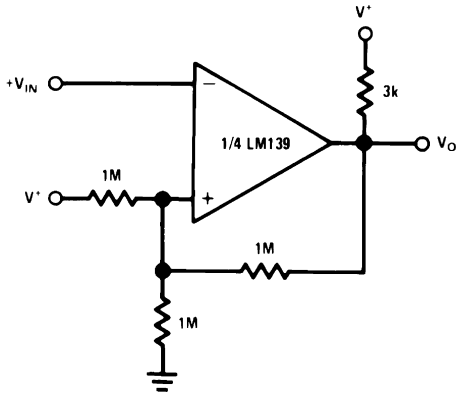


Figure 19. Inverting Comparator with Hysteresis

(V^+= 15 V_{DC})

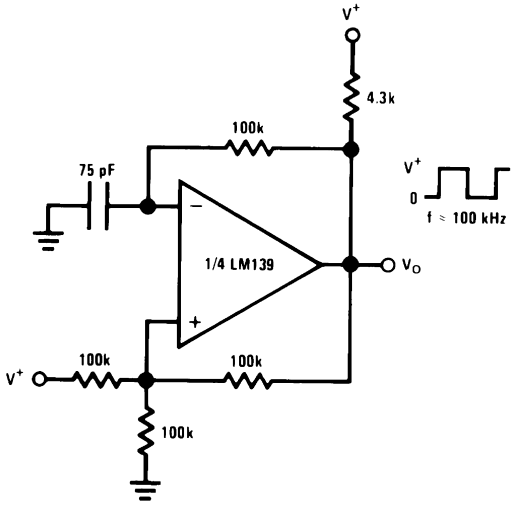


Figure 20. Squarewave Oscillator

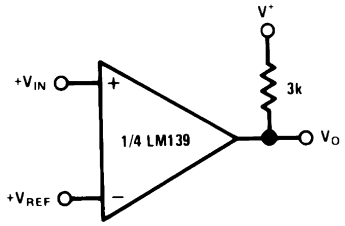


Figure 21. Basic Comparator

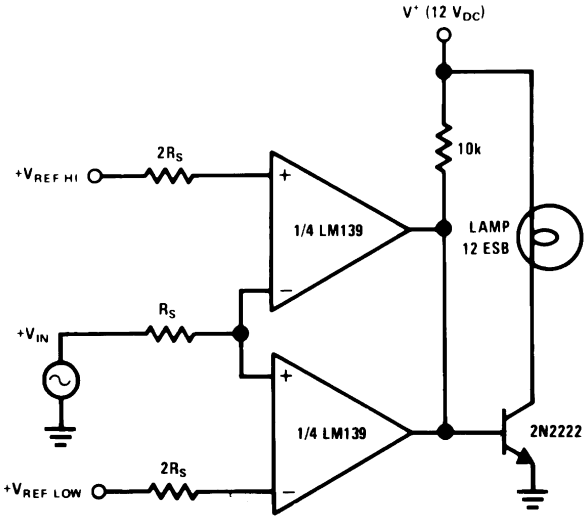


Figure 22. Limit Comparator

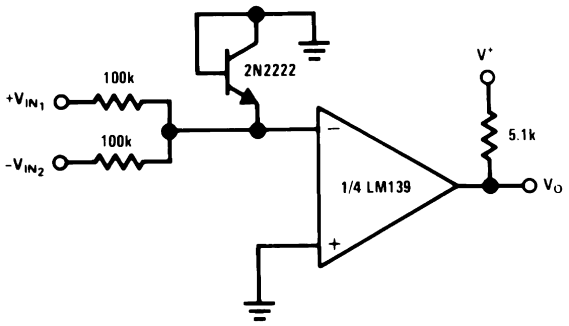
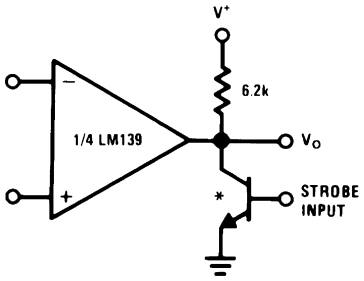


Figure 23. Comparing Input Voltages of Opposite Polarity



* Or open-collector logic gate without pull-up resistor

Figure 24. Output Strobing

(V^+= 15 V_{DC})

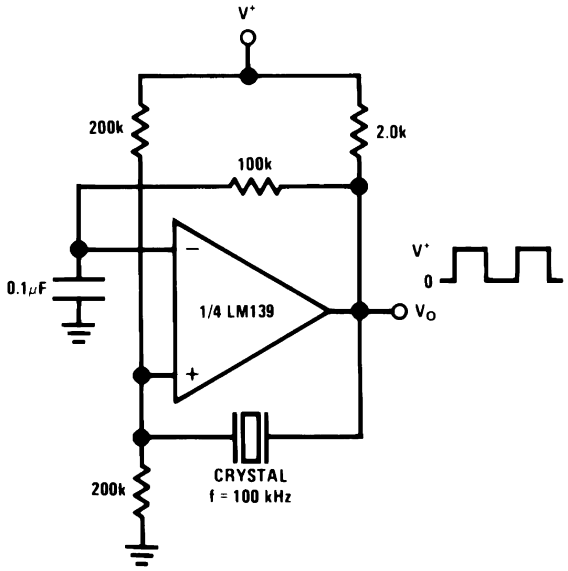
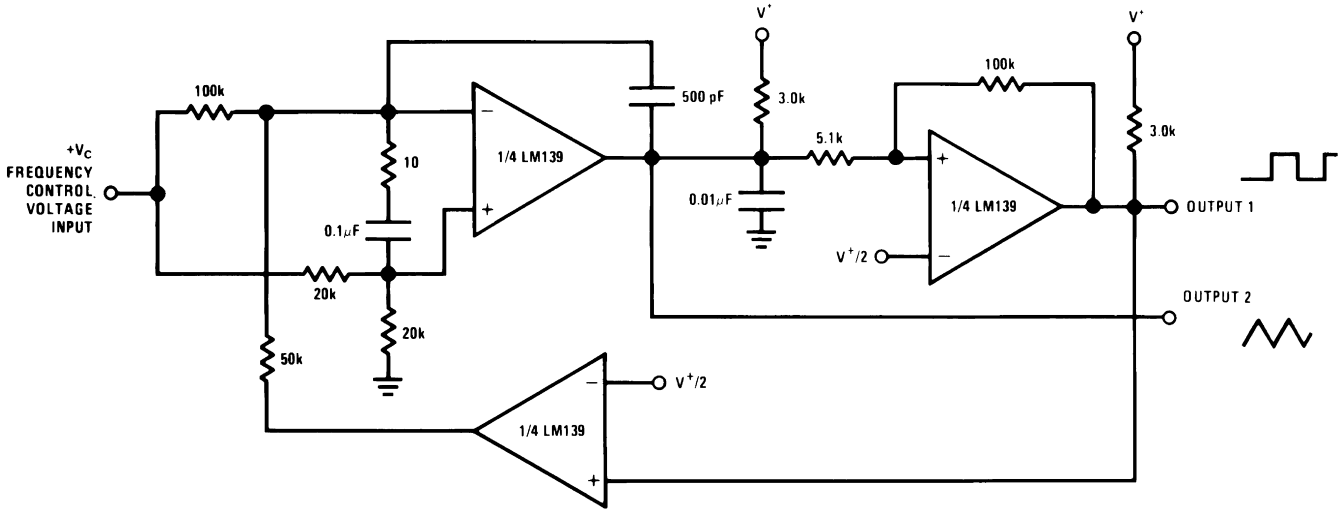


Figure 25. Crystal Controlled Oscillator



V^+ = +30 V_{DC}
250 mV_{DC} ≤ V_C ≤ +50 V_{DC}
700 Hz ≤ f_O ≤ 100 kHz

Figure 26. Two-Decade High-Frequency VCO

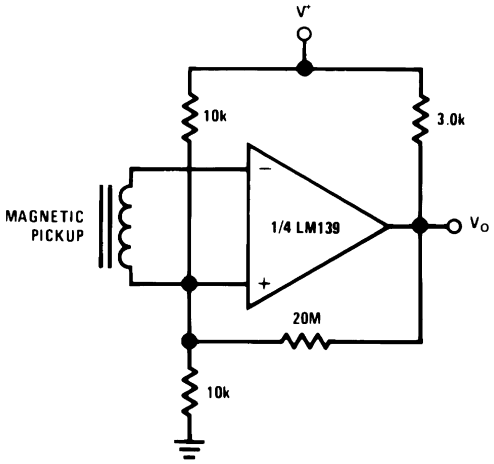


Figure 27. Transducer Amplifier

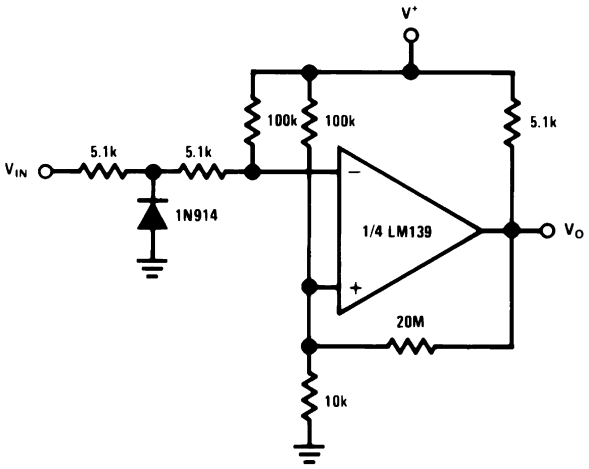


Figure 28. Zero Crossing Detector (Single Power Supply)

Split-Supply Applications

(V^+ = +15 V_{DC} and V^- = −15 V_{DC})

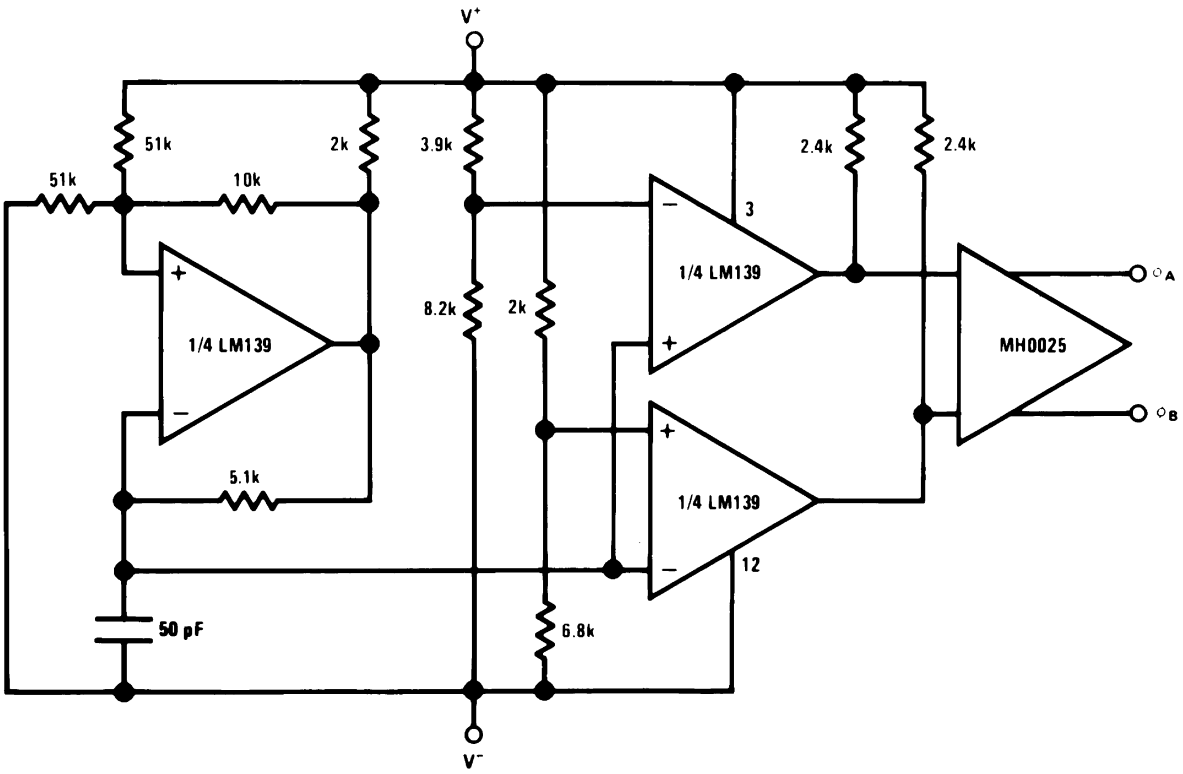


Figure 29. MOS Clock Driver

(V^+ = +15 V_{DC} and V^- = −15 V_{DC})

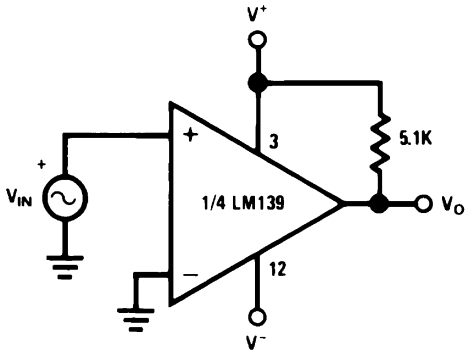


Figure 30. Zero Crossing Detector

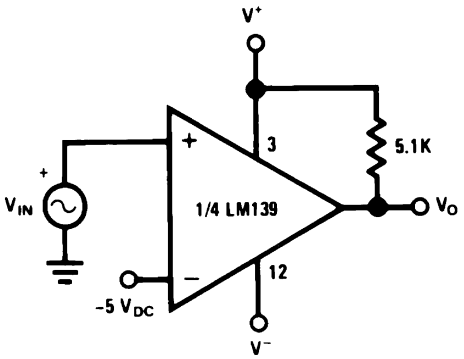
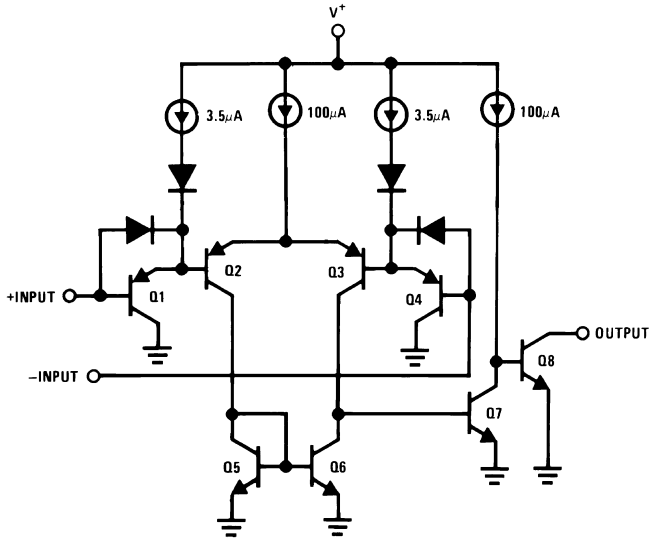


Figure 31. Comparator With a Negative Reference

Schematic Diagram



Revision History

Date Released	Revision	Section	Changes
02/08/05	A	New Release to corporate format	3 MDS datasheets converted into one Corp. datasheet format. MNLM139A-X-RH rev 4B0, MDLM139A-X rev 0C1, MNLM139–X rev 1A1. MDS datasheets will be archived.
06/28/06	B	Features, Rad Hard Electrical Section and Notes	Added Available with Radiation Ensured, Low Dose NSID's to table 5962R9673802VCA LM139AJRLQMLV, 5962R9673802VDA LM139AWRLQMLV, 5962R9673802VXA LM139AWGRLQMLV, and reference to Note. Archive Revision A.
02/13/08	C	Features, LM139A 883, QMLV & RH, SMD 5962–9673801 Electrical Characteristics, Notes	Added TID & Eldrs reference, Note - Condition A. Changed VCM parameter - pg 8, Title from Drift Values to Delta Values. Revision B will be Archived.
10/15/2010	D	Data Sheet Title	Changed the data sheet title from LM139A/LM139QML to LM139AQML/LM139QML, removed EOL NSID's. Added Bare Die NSID's. Revision C will be Archived
03/26/2013	G	All Sections	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8773901XA	ACTIVE	CFP	NAC	14	42	TBD	Call TI	Call TI	-55 to 125	LM139AWG -SMD Q 5962-87739 01XA ACO 01XA >T	Samples
5962-9673801VDA	ACTIVE	CFP	NAD	14	19	TBD	Call TI	Call TI	-55 to 125	LM139AW- QMLV Q 5962-96738 01VDA ACO 01VDA >T	Samples
5962-9673801VXA	ACTIVE	CFP	NAC	14	42	TBD	Call TI	Call TI	-55 to 125	LM139AWG- QMLV Q 5962-96738 01VXA ACO 01VXA >T	Samples
5962R9673801V9A	ACTIVE	DIESALE	Y	0	40	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
5962R9673801VCA	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	LM139AJRQMLV 5962R9673801VCA Q	Samples
5962R9673801VDA	ACTIVE	CFP	NAD	14	19	TBD	Call TI	Call TI	-55 to 125	LM139AWR QMLV Q 5962R96738 (01VDA ACO ~ 02VDA ACO) (01VDA >T ~ 02VDA >T)	Samples
5962R9673801VXA	ACTIVE	CFP	NAC	14	42	TBD	Call TI	Call TI	-55 to 125	LM139AWGR QMLV Q 5962R96738 01VXA ACO 01VXA >T	Samples
5962R9673802V9A	ACTIVE	DIESALE	Y	0	40	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
5962R9673802VCA	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	LM139AJRLQMLV 5962R9673802VCA Q	Samples
5962R9673802VDA	ACTIVE	CFP	NAD	14	19	TBD	Call TI	Call TI	-55 to 125	LM139AWRL QMLV Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										5962R96738 02VDA ACO 02VDA >T	
5962R9673802VXA	ACTIVE	CFP	NAC	14	42	TBD	Call TI	Call TI	-55 to 125	LM139AWGRL QMLV Q 5962R96738 02VXA ACO 02VXA >T	Samples
LM139 MD8	ACTIVE	DIESALE	Y	0	400	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM139 MDE	ACTIVE	DIESALE	Y	0	40	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM139 MDR	ACTIVE	DIESALE	Y	0	40	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM139AE/883	ACTIVE	LCCC	NAJ	20	50	TBD	Call TI	Call TI	-55 to 125	LM139AE /883 Q ACO 5962-90765 /883 Q >T	Samples
LM139AJ/883	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	LM139AJ/883 Q	Samples
LM139AJRLQMLV	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	LM139AJRLQMLV 5962R9673802VCA Q	Samples
LM139AJRQMLV	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	LM139AJRQMLV 5962R9673801VCA Q	Samples
LM139AW-QMLV	ACTIVE	CFP	NAD	14	19	TBD	Call TI	Call TI	-55 to 125	LM139AW- QMLV Q 5962-96738 01VDA ACO 01VDA >T	Samples
LM139AW-SMD	ACTIVE	CFP	NAD	14	19	TBD	Call TI	Call TI	-55 to 125	LM139AW -SMD Q 5962-87739 01DA ACO 01DA >T	Samples
LM139AW/883	ACTIVE	CFP	NAD	14	19	TBD	Call TI	Call TI	-55 to 125	LM139AW /883 Q ACO /883 Q >T	Samples
LM139AWG-QMLV	ACTIVE	CFP	NAC	14	42	TBD	Call TI	Call TI	-55 to 125	LM139AWG- QMLV Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										5962-96738 01VXA ACO 01VXA >T	
LM139AWG-SMD	ACTIVE	CFP	NAC	14	42	TBD	Call TI	Call TI	-55 to 125	LM139AWG -SMD Q 5962-87739 01XA ACO 01XA >T	Samples
LM139AWG/883	ACTIVE	CFP	NAC	14	42	TBD	Call TI	Call TI	-55 to 125	LM139AWG /883 Q ACO 5962-87739 /883 Q >T	Samples
LM139AWGRLQMLV	ACTIVE	CFP	NAC	14	42	TBD	Call TI	Call TI	-55 to 125	LM139AWGRL QMLV Q 5962R96738 02VXA ACO 02VXA >T	Samples
LM139AWGRQMLV	ACTIVE	CFP	NAC	14	42	TBD	Call TI	Call TI	-55 to 125	LM139AWGR QMLV Q 5962R96738 01VXA ACO 01VXA >T	Samples
LM139AWRLQMLV	ACTIVE	CFP	NAD	14	19	TBD	Call TI	Call TI	-55 to 125	LM139AWRL QMLV Q 5962R96738 02VDA ACO 02VDA >T	Samples
LM139AWRQMLV	ACTIVE	CFP	NAD	14	19	TBD	Call TI	Call TI	-55 to 125	LM139AWR QMLV Q 5962R96738 (01VDA ACO ~ 02VDA ACO) (01VDA >T ~ 02VDA >T)	Samples
LM139E/883	ACTIVE	LCCC	NAJ	20	50	TBD	Call TI	Call TI	-55 to 125	LM139E /883 Q ACO /883 Q >T	Samples
LM139J/883	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	LM139J/883 Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

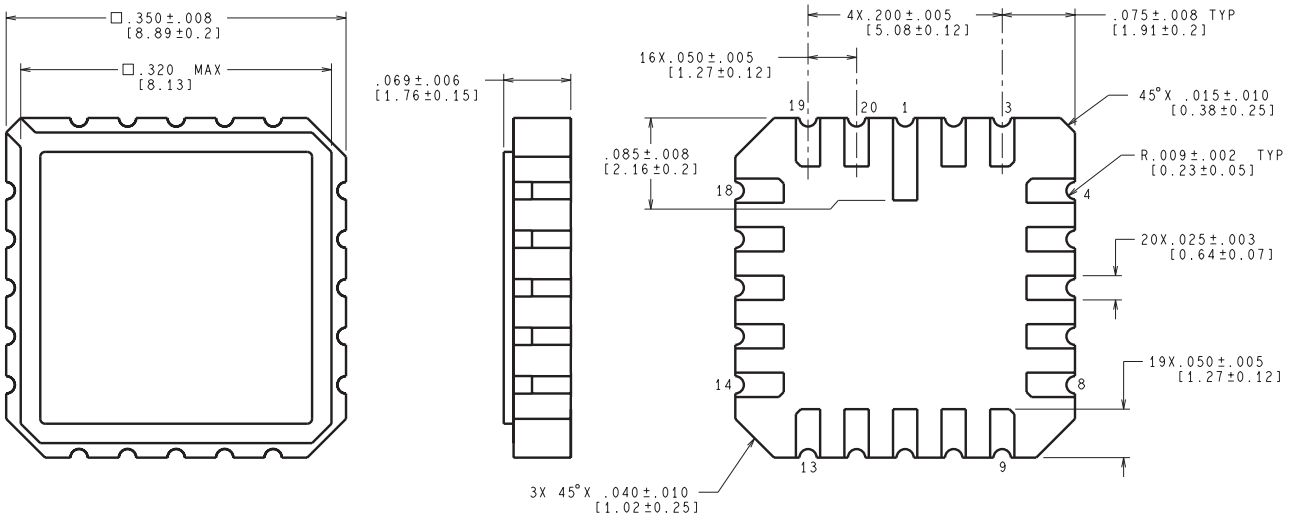
OTHER QUALIFIED VERSIONS OF LM139AQML, LM139AQML-SP :

- Military: LM139AQML
- Space: LM139AQML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

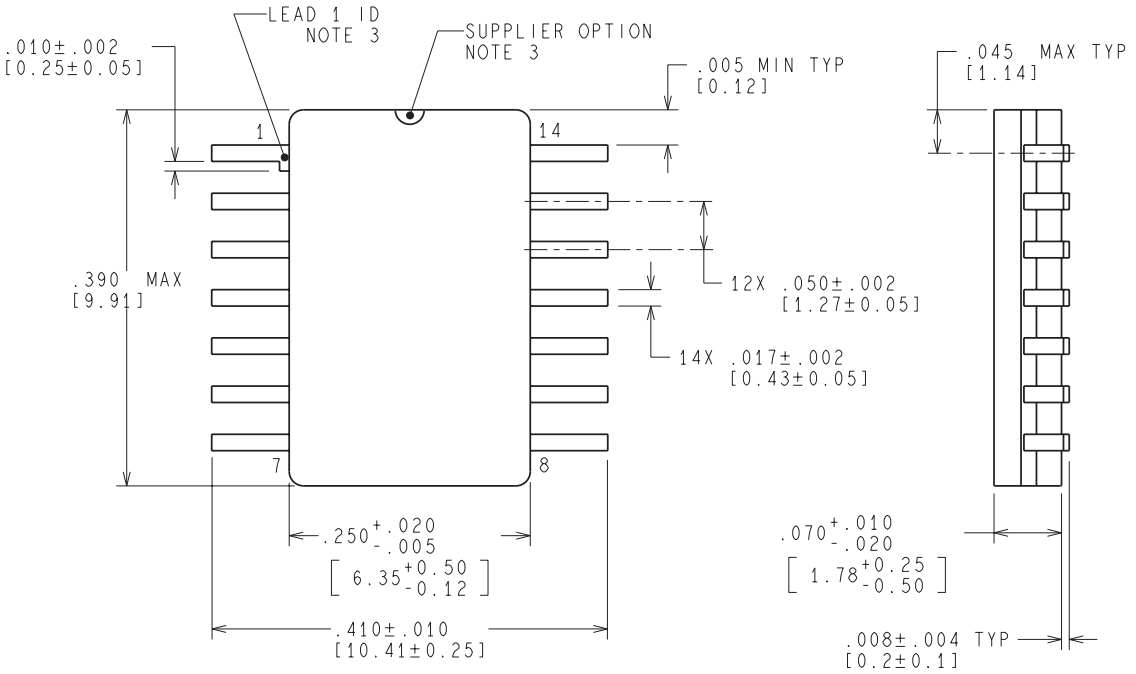
NAJ0020A

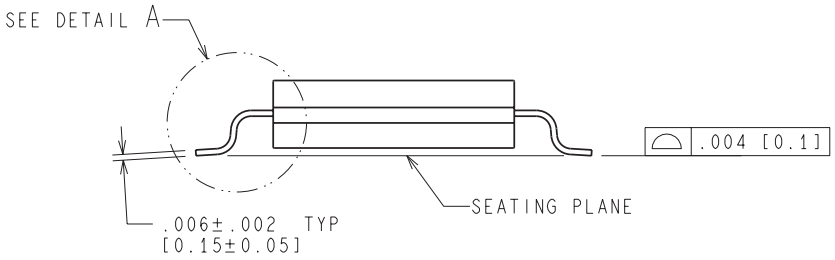


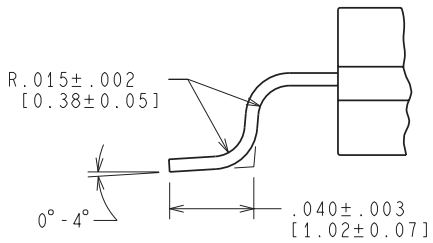
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

NAC0014A





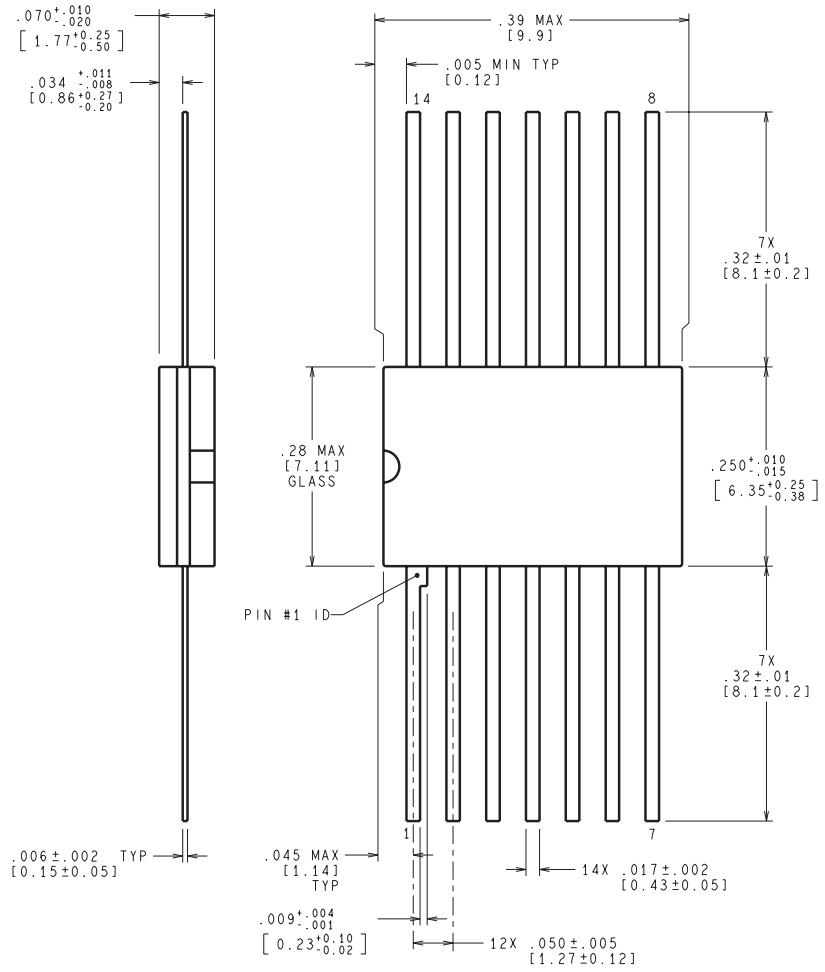


DETAIL A
TYPICAL

MIL-PRF-38535
CONFIGURATION CONTROL

WG14A (RevF)

NAD0014B



W14B (Rev P)

MIL-PRF-38535 CONFIGURATION CONTROL

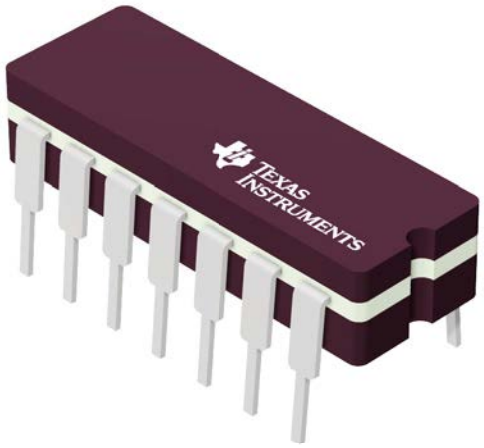
MIL-STD-1835B CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

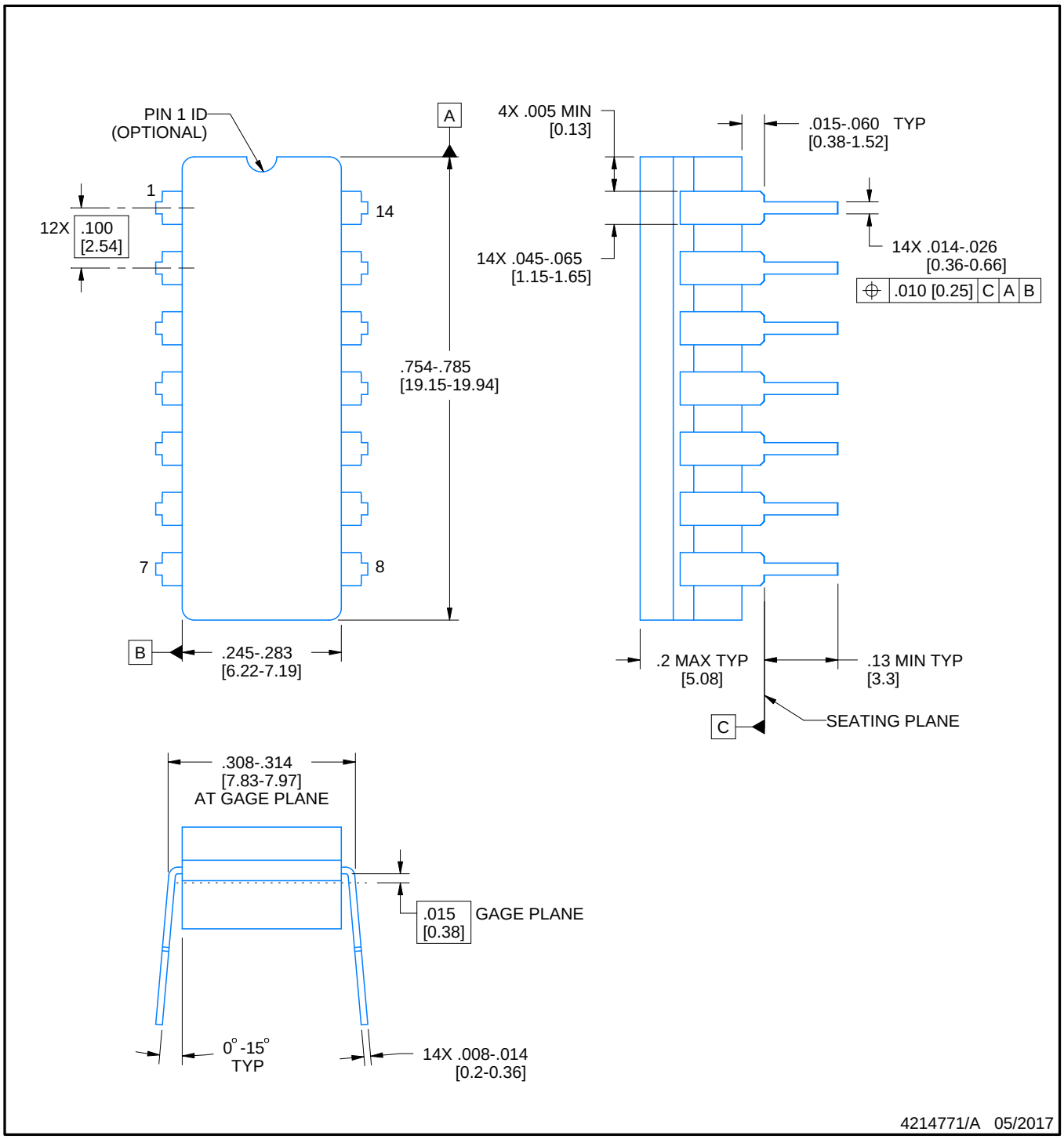
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

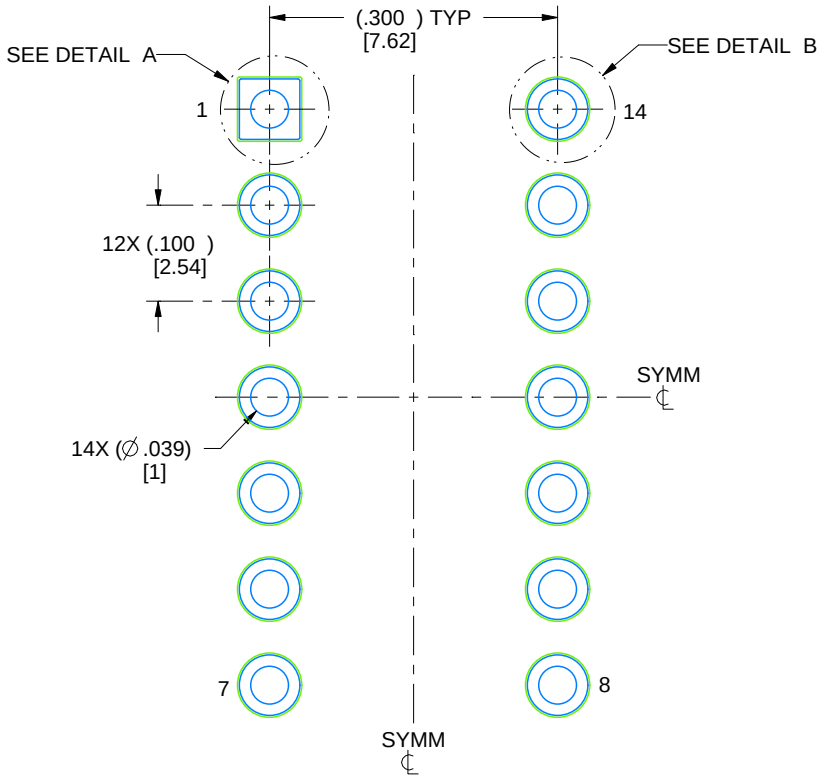
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

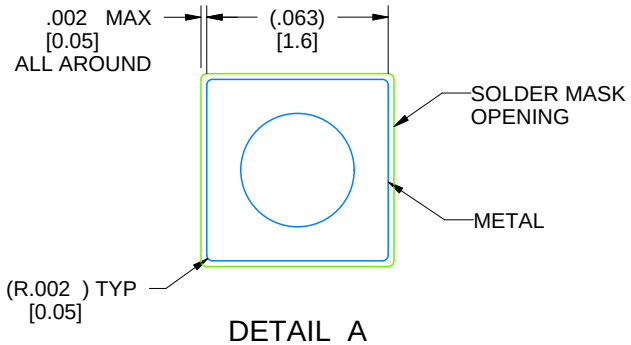
J0014A

CDIP - 5.08 mm max height

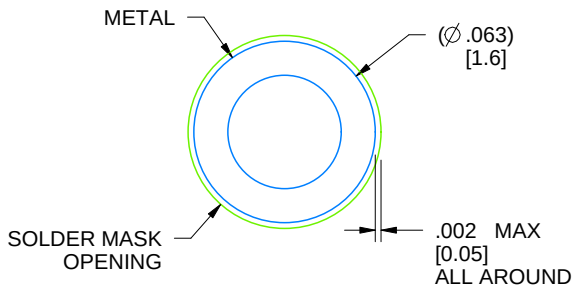
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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