National Semiconductor Corporation

PRELIMINARY

LM1578/LM2578/LM3578 Switching Regulator

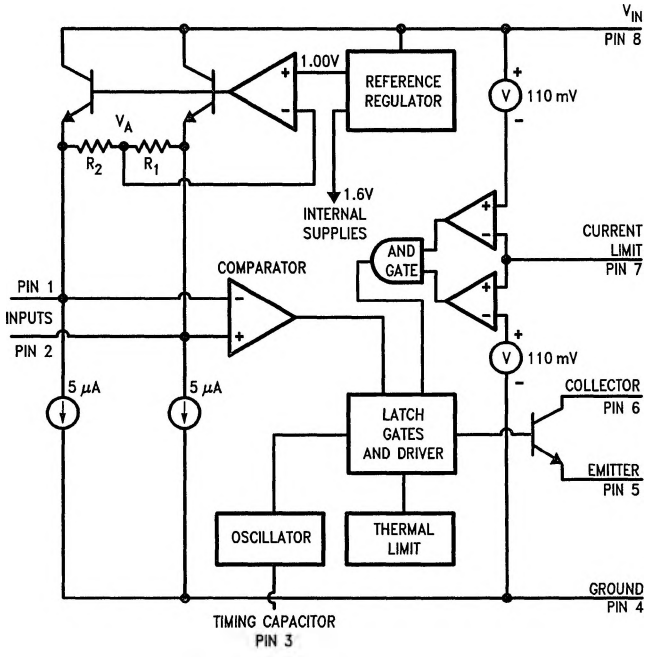
General Description

The LM1578 is a flexible 8-pin switching regulator which can easily be set up for such dc-to-dc voltage conversion circuits as the buck, boost, and inverting configurations. The LM1578 features a unique comparator input stage which not only has separate pin-outs for both the inverting and non-inverting inputs, but also provides an internal 1.0V reference to each input, thereby simplifying circuit design and p.c. board layout. The output can switch up to 750 mA and has output pins for its collector and emitter to promote design flexibility. The current limit terminal may be referenced to either the ground or the V_{in} terminal, depending upon the application. In addition, the LM1578 has an on-board oscillator, which is set by a single external capacitor.

Features

- Inverting and non-inverting inputs
- 1.0V reference at inputs
- Operates from supply voltages of 2V to 40V
- Output current up to 750 mA, saturation less than 1V
- Oscillator frequency adjustable to 100 kHz
- Current limit and thermal shut down
- Duty cycle up to 90%
- Design flexibility including buck, boost, inverting, and transformer configurations

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage	40V
Collector Output to Ground	−0.3V to +40V
Emitter Output to Ground	−1V to +40V
Power Dissipation (Note 2)	internally limited
Output Current	750 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C
Operating Temperature Range	
LM1578	−55°C to +125°C
LM2578	−40°C to +85°C
LM3578	0°C to +70°C
Maximum Junction Temperature	150°C

ESD rating is to be determined.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM1578			LM2578/LM3578			Units/ Limit
		Typ	Tested (Note 5)	Design (Note 6)	Typ	Tested (Note 5)	Design (Note 6)	
OSCILLATOR								
Frequency	C_T = 4000 pF	20			20			kHz
			22.4			25		kHz max
			17.6			15		kHz min
Frequency Drift with Temperature	C_T = 4000 pF	−0.13		**−0.25**	−0.13		**−0.30**	%/°C
								%/°C max
Amplitude	C_T = 4000 pF	550			550			mVpk-pk
REFERENCE/COMPARATOR (Note 8)								
Input Reference Voltage	$I_1 = I_2$ = 0 mA	1.0			1.0			V
	and		1.035			1.050		V max
	$I_1 = I_2$ = 1 mA ±1%		0.965			0.950		V min
	(Note 4)		**1.050**				**1.070**	V max
			0.950				**0.930**	V min
Input Reference Voltage Line Regulation	$1_1 = 1_2$ = 0 mA	0.003			0.003			%/V
	and		0.01			0.01		%/V max
	$I_1 = I_2$ = 1 mA ±1%		**0.02**				**0.02**	%/V max
	(Note 4)							
Inverting Input Current	$1_1 = 1_2$ = 0 mA, duty cycle = 75%	0.5			0.5			μA
Level Shift Accuracy	Level Shift Current = 1 mA	1.0			1.0			%
			5			10		% max
			8				**13**	% max
Input Reference Voltage Long Term Stability		100			100			ppm/kHr

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM1578			LM2578/LM3578			Units/ Limit
		Typ	Tested (Note 5)	Design (Note 6)	Typ	Tested (Note 5)	Design (Note 6)	
OUTPUT								
Collector Saturation Voltage	I_C = 750 mA, Emitter Grounded	0.7	0.85 **1.2**		0.7	0.90	**1.2**	V V max V max
Emitter Saturation Voltage	I_e = 80 mA, Collector at V_{in} = 40V	1.4	1.6 **2.1**		1.4	1.7	**2.0**	V V max V max
Collector Leakage Current	Collector to Emitter = 40V, Emitter Grounded, Output off	0.1	50 **100**		0.1	200	**250**	μA μA max μA max
Collector-Emitter Sustaining Voltage		40		34	40		34	V V min
CURRENT LIMIT								
Sense Voltage for Shutdown	Referred to V_{in} or Ground (Note 7)	110	95 **140**		110	80 160		mV mV min mV max
Sense Voltage Temperature Drift		0.3			0.3			%/°C
Sense Current	Referred to V_{in} Referred to Ground	40 0.4			40 0.4			μA μA
DEVICE POWER CONSUMPTION								
Supply Current	Output Off	2.0	3.0 **3.3**		2.0	3.5	**4.0**	mA mA max mA max
	Output On, I_C = 750 mA	14			14			mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its Rated Operating Conditions.

Note 2: At elevated temperatures, devices must be derated based on package thermal resistance. The device in a TO-5 package must be derated at 150°C/W, junction to ambient or 45°C/W, junction to case. The thermal resistance for the 8-pin N package is 130°C/W, junction to ambient.

Note 3: Unless otherwise specified, these specifications apply for V_{in} = 2V (2.2V, < −25°C) and V_{in} = 40V. Timing Capacitor = 4000 pF with 25% and 75% duty cycle. Normal typeface indicates T_j = 25°C limits. **Boldface type indicates limits for full temperature range.** This is T_j = −55°C to +150°C for the LM1578, T_j = −40°C to +125°C for the LM2578, and T_j = 0°C to +125°C for the LM3578.

Note 4: I_1 and I_2 are the external sink currents at the inputs.

Note 5: Guaranteed and 100% production tested.

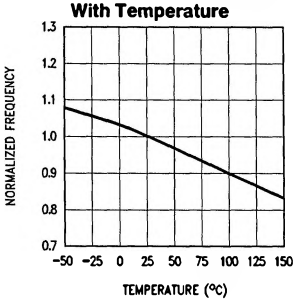
Note 6: Guaranteed (but not 100% production tested) over the operating temperature ranges. These limits are not to be used to calculate outgoing quality levels.

Note 7: Connection of a 10 kΩ resistor from pin 1 to pin 4 establishes the duty cycle at its maximum of 90% with a maximum voltage swing on the output collector of 40V. Applying the minimum current sense voltage will not reduce the duty cycle to less than 50%. Applying the maximum current limit sense voltage is certain to reduce the duty cycle below 50%. An additional 15 mV above the sense voltage may be required to reduce the duty cycle to 0% (see current limit of the typical performance characteristics).

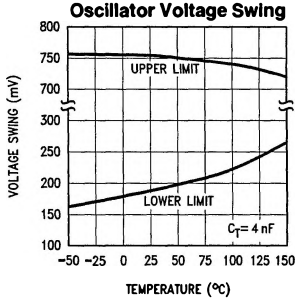
Note 8: Input terminals are protected from accidental shorts to ground but if external voltages higher than the reference voltage is applied, excessive current will flow and should be limited to less than 5 mA.

Typical Performance Characteristics

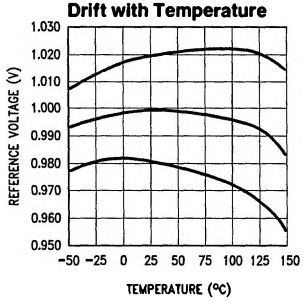
Oscillator Frequency Change With Temperature



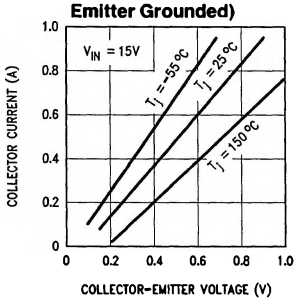
Oscillator Voltage Swing



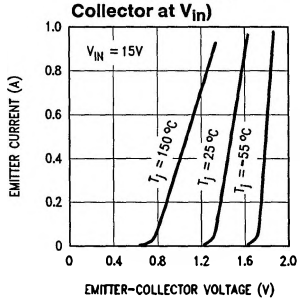
Input Reference Votlage Drift with Temperature



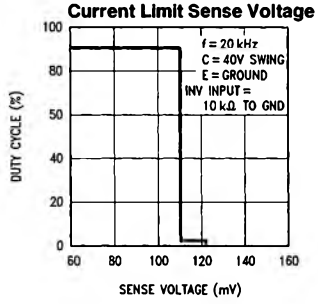
Collector Saturation Voltage (Sinking Current, Emitter Grounded)



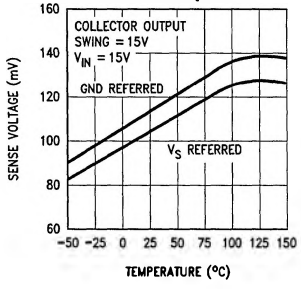
Emitter Saturation Voltage (Sourcing Current, Collector at V_{IN})



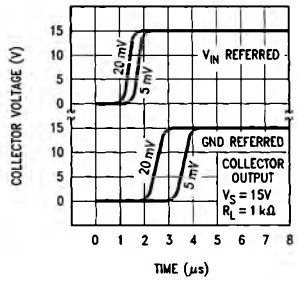
Ground Referred Current Limit Sense Voltage



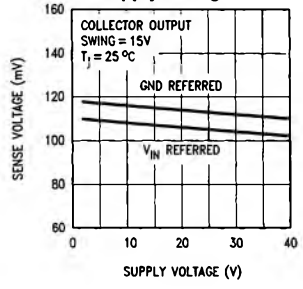
Current Limit Sense Voltage Drift with Temperature



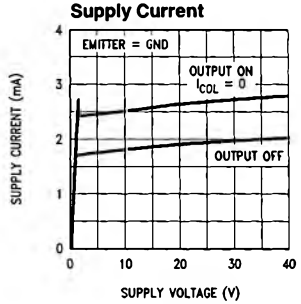
Current Limit Response Time For Various Over Drives



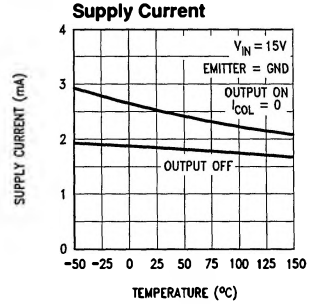
Current Limit Sense Voltage vs. Supply Voltage



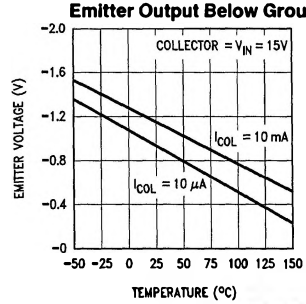
Supply Current



Supply Current



Collector Current With Emitter Output Below Ground



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Test Circuit*

Parameter tests can be made using the test circuit shown. Select the desired V_{in}, collector voltage and duty cycle with adjustable power supplies. A digital volt meter with an input resistance greater than 100 MΩ should be used to measure the following:

Input Reference Voltage to Ground; S1 in either position.

Level Shift Accuracy (%) = $(T_{P3}(V)/1V) \times 100\%$; S1 at $I_1 = I_2 = 1$ mA

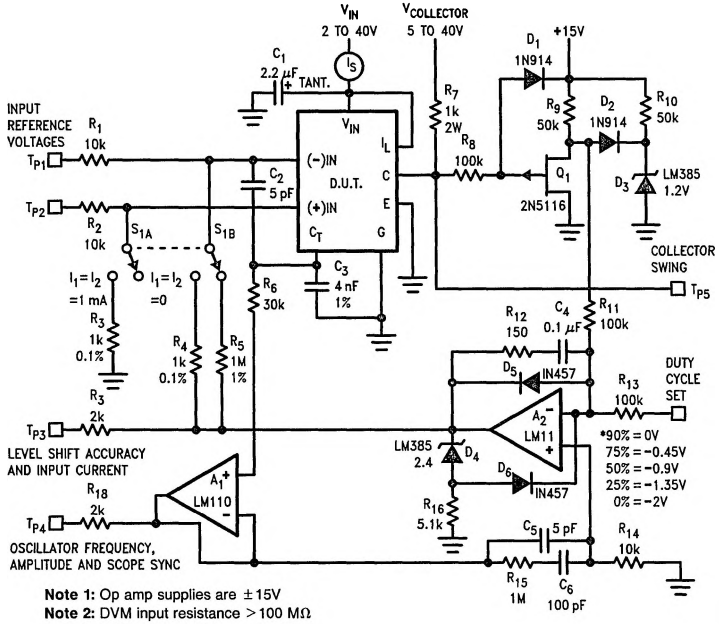
Input Current (mA) = $(1V - T_{p3}(V))/1$ MΩ: S1 at $I_1 = I_2 = 0$ mA.

Oscillator T_{P4} can be measured using a frequency counter or an oscilloscope.

The current limit sense voltage is measured by connecting an adjustable 0 to 1V floating power supply in series with the current limit terminal and referring it to either the ground or the V_{in} terminal. Set the duty cycle to 90% and monitor test point T_{P5} while adjusting the floating power supply voltage until the LM1578's duty cycle just reaches 0%. This voltage is the current limit sense voltage.

The supply current should be measured with the duty cycle at 0% and S1 in the $I_1 = I_2 = 0$ mA position.

*LM1578 specifications are measured using automated test equipment. This circuit is provided for the customer's convenience when checking parameters. Due to possible variations in testing conditions, the measured values from these testing procedures may not match those of the factory.



Note 1: Op amp supplies are ±15V
Note 2: DVM input resistance >100 MΩ
Note 3: *LM1578 max duty cycle is 90%

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Definition of Terms

Input Reference Voltage: The reference voltage referred to ground, applied to either the inverting or non-inverting inputs, which will cause the output to switch on or off.

Input Reference Current: The current applied to either the inverting or the non-inverting input which will cause the output to switch on or off.

Input Level Shift Accuracy: For two equal resistors sinking current from the inverting and non-inverting input terminals, the input level shift accuracy is the ratio of the voltage across the resistors to produce a given duty cycle at the output.

Collector Saturation Voltage: With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's emitter connected to ground, the collector saturation voltage is the collector-to-emitter voltage for a given collector current.

Emitter Saturation Voltage: With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's collector connected to V_{in}, the emitter saturation voltage is the collector-to-emitter voltage for a given emitter current.

Current Limit Sense Voltage: The voltage referred to either the supply or the ground terminal which will cause the output transistor to turn off and resets cycle-by-cycle at the oscillator frequency.

Current Limit Sense Current: The bias current for the current limit terminal at sense voltage.

Supply Current: The IC power supply current, excluding the output transistor's collector current, with the oscillator operating.

Functional Description

The LM1578 is a very simple device. A control signal is fedback to the LM1578's comparator section for output error detection. The comparator and oscillator feed their respective signals to a logic network for determining when the output transistor is to be turned on and off. The following is a brief description of the various stages of the LM1578.

COMPARATOR INPUT STAGE

The LM1578 has a unique comparator input stage-not only are both the inverting and non-inverting inputs available to the user, but both are referenced to a 1.0V reference This is accomplished as follows: A 1.0V reference is fed into a modified voltage follower circuit (see FUNCTIONAL DIAGRAM). When both inputs are floating, no current flows through either R_1 or R_2, and thus, both inputs to the comparator are at the same potential as V_a, i.e. 1.0V. When one input, say the non-inverting input, is moved ΔV away from V_a, a current of $\Delta V/R_1$ flows through R_1. This same current flows through R_2 and thus the comparator sees a total voltage difference of 2 ΔV between its inputs. The high gain of the system immediately corrects for this imbalance and returns both inputs to the 1.0V level

The LM1578's unique comparator input stage increases circuit flexibility, while minimizing the total number of parts. The inverting switching regulator configuration, for example, can be set-up without having to use an external op amp for feedback polarity reversal (See TYPICAL APPLICATIONS).

OSCILLATOR

The LM1578 provides an on-board oscillator which can be adjusted up to 100 kHz. It's frequency is set by a single external capacitor, C_1. A graph displaying C_1 versus frequency is shown in *Figure 1*. The oscillator provides a blanking pulse to turn off the output transistor for at least 10% of each oscillator cycle to help protect the device.

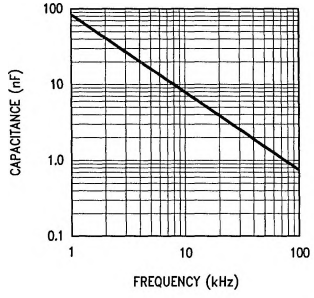

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FIGURE 1

OUTPUT TRANSISTOR

The output transistor is capable of delivering up to 750 mA of current with a saturation voltage of less than 1.2V. The collector and emitter are both available as shown in the functional diagram.

CURRENT LIMIT

The LM1578's current limit is novel in that it may be referenced to either the ground or the V_{in} terminal, and operates on a cycle-by-cycle basis.

The current limit section consists of two comparators: one with its non-inverting input referenced to a voltage, V, 110 mV below V_{in}, the other with its inverting input referenced 110 mV above ground (see FUNCTIONAL DIAGRAM). The current limit is activated whenever the current limit terminal is pulled 110 mV away from either V_{in} or ground.

Typical Applications

The LM1578 may be operated in either the continuous or the discontinuous conduction mode. The following applications (except for the Buck-Boost Regulator) are designed for continous conduction operation. That is, the inductor current is not allowed to fall to zero. This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

BUCK REGULATOR

The buck configuration is used to step an input voltage down to a lower level. Transistor Q1 in *Figure 2* chops the input D.C. voltage into a squarewave. This squarewave is then converted back into a D.C. voltage of lower magnitude by the low pass filter consisting of L1 and C1. The duty cycle, D, of the squarewave relates the output voltage to the input voltage by the following relation:

$V_{out} = D \times V_{in} = V_{in} \times (t_{on})/(t_{on} + t_{off})$.

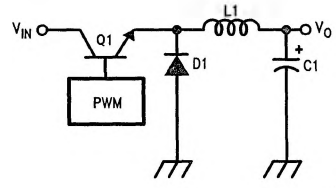

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FIGURE 2

Figure 3 is a 15V to 5V buck regulator with an output current, I_o, of 350 mA. The circuit becomes discontinuous at 20% of $I_{o(max)}$, has 10 mV of output voltage ripple, an efficiency of 75%, a load regulation of 30 mV (70 mA to 350 mA) and a line regulation of 10 mV ($12 \leq V_{in} \leq 18V$).

Component values are selected as follows:

$R1 = (V_o - 1) \times R2$ where $R2 = 10\,k\Omega$

$R3 = V/I_{sw(max)}$

$R3 = 0.15\Omega$

where:

V is the current limit sense voltage, 0.11V

$I_{sw(max)}$ is the maximum allowable current thru the output transistor.

L1 is the inductor and may be found from the inductance calculation chart, as follows.

Given $V_{in} = 15V$ $V_o = 5V$
$I_{o(max)} = 350\,mA$ $f_{osc} = 50\,kHz$
Discontinuous at 20% of $I_{o(max)}$.

Note that since the circuit will become discontinuous at 20% of $I_{o(max)}$, the load current must not be allowed to fall below 70 mA.

Step 1: Calculate the maximum D.C. current through the inductor, $I_{IND(max)}$. The necessary equations are indicated at the top of the chart and show that $I_{IND(max)} = I_{o(max)}$ for the buck configuration. Thus, $I_{IND(max)} = 350\,mA$.

Typical Applications (Continued)

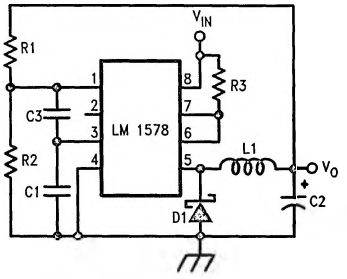
Step 2: Calculate the inductor Volts-sec product, E-T_{op}, according to the equations given from the chart. For the Buck;

$E\text{-}T_{op} = (V_{in} - V_o)(V_o/V_{in})(1000/f_{osc})$

$= (15 - 5)(5/15)(1000/50)$

$= 100V - \mu s.$

with the oscillator frequency, f_{osc}, expressed in kHz.



V_{in} = 15V
V_o = 5V
V_{ripple} = 50 mV
I_o = 350 mA
f_{osc} = 50 kHz
R1 = 40 kΩ
R2 = 10 kΩ
R3 = 0.15Ω
C1 = 1820 pF
C2 = 220 μF
C3 = 20 pF
L1 = 470 μH
D1 = 1N5818

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FIGURE 3. Buck or Step-Down Regulator

Step 3: Using the graph with axis labeled "Discontinuous At % I_o" and "$I_{IND(max, DC)}$" find the point where the desired maximum inductor current, $I_{IND(max, DC)}$ intercepts the desired discontinuity percentage.

In this example, the point of interest is where the 0.35A line intersects with the 20% line. This is nearly the midpoint of the horizontal axis.

Step 4: This last step is merely the translation of the point found in Step 3 to the graph directly below it. This is accomplished by moving straight down the page to the point which intercepts the desired E-T_{op}. For this example, E-T_{op} is 66V-μs and the desired inductor value is 470 μH. Since this example was for 20% discontinuity, the bottom chart could have been used directly, as noted in step 3 of the chart instructions.

For a full line of standard inductor values, contact Pulse Engineering (San Diego, Calif.) regarding their PE526XX series, or A. I. E. Magnetics (Nashville, Tenn.).

A more precise inductance value may be calculated for the Buck, Boost and Inverting Regulators as follows:

BUCK

$L = V_o(V_{in} - V_o)/(\Delta I_o V_{in} f_{osc})$

BOOST

$L = V_{in}^2(V_o - V_{in})/(\Delta I_o f_{osc} V_o^2)$

INVERT

$L = V_{in}^2 |V_o|/[\Delta I_o(V_{in} + |V_o|)^2 f_{osc}]$

where:

$\Delta I_o = 2I_o \times$ (Discontinuity Factor). The Discontinuity Factor is the percent discontinuity of I_o expressed as a decimal (i.e.; for 10% discontinuity, the discontinuity factor is 0.1).

C1 is the frequency selection capacitor found in *Figure 1*.

$C2 \geq V_o(V_{in} - V_o)/(8f_{osc}{}^2 V_{in} V_{ripple} L1)$

where V_{ripple} is the peak-to-peak output voltage ripple.

C3 is necessary for continuous operation and is generally in the 10 to 30 pF range.

D1 should be a Schottky type diode, such as the 1N5818 or 1N5819.

BUCK WITH BOOSTED OUTPUT CURRENT

For applications requiring a large output current, an external transistor may be used as shown in *Figure 4*. This circuit steps a 15V supply down to 5V with 1.5A of output current. The output ripple is 50 mV, with an efficiency of 80%, a load regulation of 40 mV (150 mA to 1.5A), and a line regulation of 20 mV (12V ≤ V_{in} ≤ 18V).

Component values are selected as outlined for the buck regulator with a discontinuity factor of 10%, with the addition of R4 and R5:

$R4 = 10V_{BE1}B_f/I_p$

$R5 = (V_{in} - V - V_{BE1} - V_{sat})B_f/(I_{IND(max, DC)} + I_{R4})$

where:

V_{BE1} is the V_{BE} of transistor Q1.

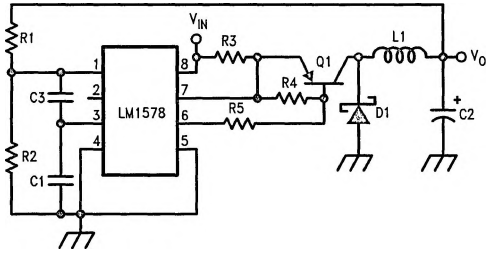
V_{sat} is the saturation voltage of the LM1578 output transistor.

V is the current limit sense voltage.

B_f is the forced current gain of transistor Q1 (B_f = 30 for *Figure 4*).

$I_{R4} = V_{BE1}/R4$

$I_p = I_{IND(max, DC)} + 0.5\Delta I_o$



V_{in} = 15V
V_o = 5V
V_{ripple} = 50 mV
I_o = 1.5A
f_{osc} = 50 kHz
R1 = 40 kΩ
R2 = 10 kΩ
R3 = 0.05Ω
R4 = 200Ω
R5 = 330Ω
C1 = 1820 pF
C2 = 330 μF
C3 = 20 pF
L1 = 220 μH
D1 = 1N5819
Q1 = D45

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FIGURE 4. Buck Converter with Boosted Output Current

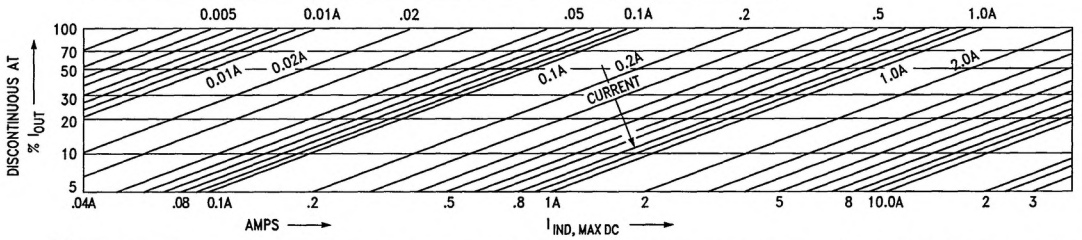
Typical Applications (Continued)

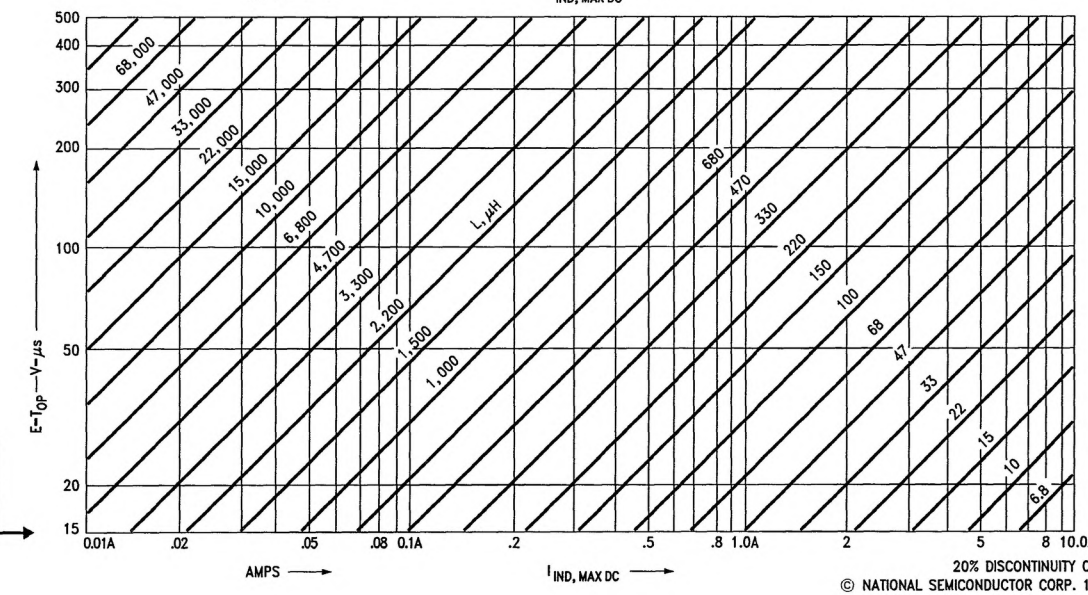
DC/DC CONVERTER
INDUCTANCE CALCULATOR

HOW TO USE THIS CHART

1. CALCULATE $I_{IND, MAX\ DC}$ HERE →
2. CALCULATE $E\text{-}T_{OP}$ HERE →
3. ENTER REQUIRED % DISCONTINUITY HERE → IF "20%" PROCEED TO (7)
4. PROCEED → HORIZONTALLY TO $I_{IND, MAX\ DC}$ FROM (1)
5. FROM $I_{IND, MAX\ DC}$ PROCEED VERTICALLY TO ↓ $E\text{-}T_{OP}$ FROM (2)
6. READ INDUCTANCE VALUE AT $E\text{-}T_{OP}$ FOR $I_{IND, MAX\ DC}$
7. READ $I_{IND, MAX\ DC}$ FROM (1) HERE
8. READ INDUCTANCE VALUE AT $E\text{-}T_{OP}$ FOR $I_{IND, MAX\ DC}$

BUCK	BOOST	INVERT	
$I_{IND} = I_{LOAD}$	$I_{IND} = I_{LOAD} \frac{V_O}{V_{IN}}$	$I_{IND} = I_{LOAD} \cdot \frac{V_{IN} + \lvert V_O \rvert}{V_{IN}}$	I_{IND}
$(V_{IN} - V_O) \cdot \frac{V_O}{V_{IN}} \cdot \frac{1000}{F, kHz}$	$(V_O - V_{IN}) \cdot \frac{V_{IN}}{V_O} \cdot \frac{1000}{F, kHz}$	$V_{IN} \cdot \frac{\lvert V_O \rvert}{V_{IN} + \lvert V_O \rvert} \cdot \frac{1000}{F, kHz}$	$E\text{-}T_{OP}$





20% DISCONTINUITY ONLY

TL/H/8711–7

Typical Applications (Continued)

BOOST REGULATOR

The boost regulator converts a low input voltage into a higher output voltage. The basic configuration is shown in *Figure 5*. Energy is stored in the inductor while the transistor is on and then transferred with the input voltage to the output capacitor for filtering when the transistor is off. Thus,

$V_o = V_{in} + V_{in}(t_{on}/t_{off})$.

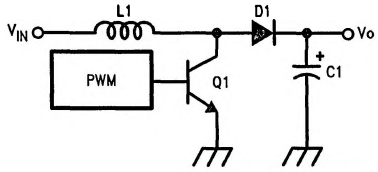


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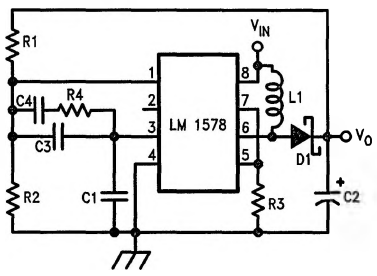
FIGURE 5

The circuit of *Figure 6* converts a 5V supply into a 15V supply with 150 mA of output current, a load regulation of 14 mV (30 mA to 150 mA), and a line regulation of 35 mV ($4.5V \le V_{in} \le 8.5V$).



V_{in} = 5V
V_o = 15V
V_{ripple} = 10 mV
I_o = 150 mA
f_{osc} = 50 kHz
R1 = 140 kΩ
R2 = 10 kΩ
R3 = 0.1 Ω
R4 = 220 kΩ
C1 = 1820 pF
C2 = 470 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 330 μH
D1 = 1N5818

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FIGURE 6. Boost or Step-Up Regulator

$R1 = (V_o - 1)\,R2$ where $R2 = 10\,k\Omega$.

$R3 = V/(I_{IND(max,\,DC)} + 0.5\,\Delta I_o)$

where:

ΔI_o is defined in the "Buck Regulator" section.

R4, C3 and C4 are necessary for continuous operation and are typically 220 kΩ, 20 pF, and 0.0022 μF respectively.

C1 is the oscillator frequency selection capacitor found in *Figure 1*.

$C2 \ge I_o\,(V_o - V_{in})/(f_{osc}\,V_o\,V_{ripple})$.

D1 is a Schottky type diode such as a IN5818 or IN5819.

L1 is found as described in the buck converter section.

INVERTING REGULATOR

Figure 7 shows the basic configuration for an inverting regulator. The input voltage is of a positive polarity, but the output is negative. The output may be less than, equal to, or greater in magnitude than the input. The relationship between the magnitude of the input voltage and the output voltage is $V_o = V_{in} \times (t_{on}/t_{off})$.

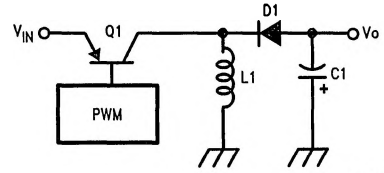

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FIGURE 7.

Figure 8 shows an LM1578 configured as a 5V to −15V polarity inverter with an output current of 300 mA, a load regulation of 44 mV (60 mA to 300 mA) and a line regulation of 50 mV ($4.5V \le V_{in} \le 8.5V$).

$R1 = (|V_o| + 1)\,R2$ where $R2 = 10\,k\Omega$.

$R3 = V/(I_{IND(max,\,DC)} + 0.5\,\Delta I_o)$.

$R4 = 10V_{BE1}Bf/(I_{IND\,(max,\,DC)} + 0.5\,\Delta I_o)$

where:

V, V_{BE1}, V_{sat}, and B_f are defined in the "Buck Converter with Boosted Output Current" section.

ΔI_o is defined in the "Buck Regulator" section.

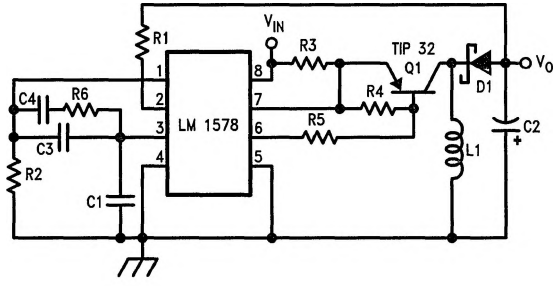
R5 is defined in the "Buck with Boosted Output Current" section.

R6 serves the same purpose as R4 in the Boost Regulator circuit and is typically 220 kΩ.

C1, C3 and C4 are defined in the "Boost Regulator" section.

$C2 \ge I_o\,|V_o|/[f_{osc}(|V_o| + V_{in})\,V_{ripple}]$

L1 is found as outlined in the section on buck converters, using the inductance chart for the invert configuration and 20% discontinuity.



V_{in} = 5V
V_o = −15V
V_{ripple} = 5 mV
I_o = 300 mA, I_{min} = 60 mA
f_{osc} = 50 kHz
R1 = 160 kΩ R2 = 10 kΩ
R3 = 0.01 Ω R4 = 190Ω
R5 = 82Ω R6 = 220 kΩ
C1 = 1820 pF
C2 = 1000 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 150 μH
D1 = 1N5818

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FIGURE 8. Inverting Regulator

Typical Applications (Continued)

BUCK-BOOST REGULATOR

The Buck-Boost Regulator, shown in *Figure 9*, may step a voltage up or down, depending upon whether or not the desired output voltage is greater or less than the input voltage. In this case, the output voltage is 12V with an input voltage from 9V to 15V. The circuit exhibits an efficiency of 75%, with a load regulation of 60 mV (10 mA to 100 mA) and a line regulation of 52 mV.

$R1 = (V_o - 1)\,R2$ where $R2 = 10\,k\Omega$

$R3 = V/0.75A$

R4, C1, C3 and C4 are defined in the "Boost Regulator" section.

D1 and D2 are Schottky type diodes such as the 1N5818 or 1N5819.

$$C2 \geq \frac{(I_o/V_{ripple})\,(V_o + 2V_d)}{[f_{osc}\,(V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})]}$$

where:

V_d is the forward voltage drop of the diodes.

V_{sat} is the saturation voltage of the LM1578 output transistor.

V_{sat1} is the saturation voltage of transistor Q1.

$$L1 \geq (V_{in} - V_{sat} - V_{sat1})\,(t_{on}/I_p)$$

where:

$$t_{on} = \frac{(1/f_{osc})\,(V_o + 2V_d)}{(V_o + V_{in} + 2V_d - V_{sat} - V_{sat1})}$$

$$I_P = \frac{2I_o\,(V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})}{(V_{in} - V_{sat} - V_{sat1})}$$

RS-232 LINE DRIVER POWER SUPPLY

The power supply, shown in *Figure 10*, operates from an input voltage as low as 4.2V (5V nominal), and delivers an output of ±12V at ±40 mA with better than 70% efficiency. The circuit provides a load regulation of ±150 mV (from 10% to 100% of full load) and a line regulation of ±10 mV. Other notable features include a cycle-by-cycle current limit and an output voltage ripple of less than 40 mVp-p.

A unique feature of this circuit is it's use of feedback from both outputs. This dual feedback configuration results in a sharing of the output voltage regulation by each output so that neither side becomes unbalanced as in single feedback systems. In addition, since both sides are regulated, it is not necessary to use a linear regulator for output regulation.

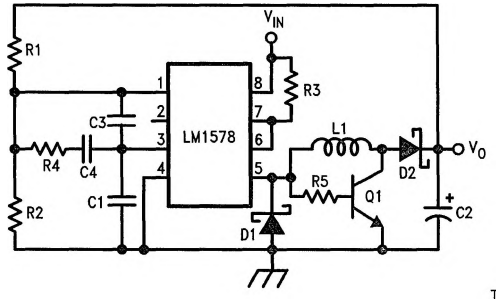
The feedback resistors, R2 and R3, may be selected as follows by assuming a value of 10 kΩ for R1;

$R2 = (V_o - 1V)/45.8\,\mu A = 240\,k\Omega$

$R3 = (|V_o| + 1V)/54.2\,\mu A = 240\,k\Omega$

Actually, the currents used to program the values for the feedback resistors may vary from 40 μA to 60 μA, as long as their sum is equal to the 100 μA necessary to establish the 1V threshold across R1. Ideally, these currents should be equal (50 μA each) for optimal control. However, as was done here, they may be mismatched in order to use standard resistor values. This results in a slight mismatch of regulation between the two outputs.

The current limit resistor, R4, is selected by dividing the current limit threshold voltage by the maximum peak current level in the output switch. For our purposes R4 = 90 mV/750 mA = 0.12Ω. A value of 0.1Ω was used.



$9V \leq V_{in} \leq 15V$
$V_o = 12V$
$I_o = 100\,mA$
$V_{ripple} = 50\,mV$
$f_{osc} = 50\,kHz$
R1 = 110 k
R2 = 10 k
R3 = 0.1
R4 = 220 k
R5 = 270
C1 = 1820 pF
C2 = 220 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 220 μH
D1, D2 = 1N5819
Q1 = D44

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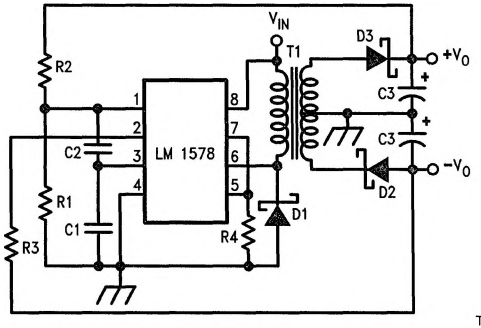
FIGURE 9. Buck-Boost Regulator



$V_{in} = 5V$
$V_o = \pm 12V$
$I_o = \pm 40\,mA$
$f_{osc} = 80\,kHz$
R1 = 10 kΩ
R2 = 240 kΩ
R3 = 240 kΩ
R4 = 0.1 Ω
C1 = 820 pF
C2 = 10 pF
C3 = 220 μF
D1, D2, D3 = 1N5819
T1 = PE-64287

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FIGURE 10. RS-232 Line Driver Power Supply

Typical Applications (Continued)

Capacitor C1 sets the oscillator frequency and is selected from *Figure 1*.

Capacitor C2 serves as a compensation capacitor for synchronous operation and a value of 10 to 50 pF should be sufficient for most applications.

A minimum value for an ideal output capacitor C3, could be calculated as $C = I \times t/\Delta V$ where I is the load current, t is the transistor on time (typically $0.4/f_{osc}$), and ΔV is the peak-to-peak output voltage ripple. A larger output capacitor than this theoretical value should be used since electrolytics have poor high frequency performance. Experience has shown that a value from 5 to 10 times the calculated value should be used.

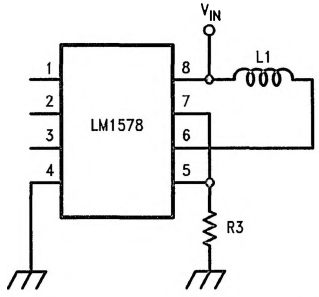
For good efficiency, the diodes must have a low forward voltage drop and be fast switching. 1N5819 Schottky diodes work well.

Transformer selection should be picked for an output transistor "on" time of $0.4/f_{osc}$, and a primary inductance high enough to prevent the output transistor switch from ramping higher than the transistor's rating of 750 mA. Pulse Engineering (San Diego, Calif.) and Renco Electronics, Inc. (Deer Park, N.Y.) can provide further assistance in selecting the proper transformer for a specific application need. The transformer used in *Figure 10* was a Pulse Engineering PE-64287.

CURRENT LIMIT

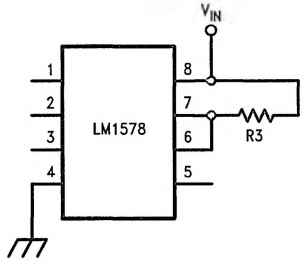
As mentioned in the functional description, the current limit terminal may be referenced to either the V_{in} or the ground terminal. Resistor, R3 converts the current to be sensed into a voltage for current limit detection.

Current Limit Ground Referred



TL/H/8711–15

Current Limit V_{in} Referred



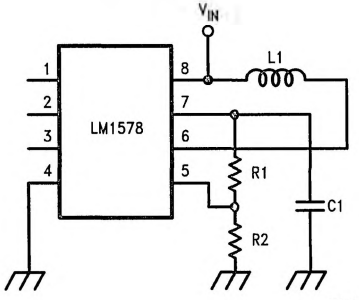
TL/H/8711–16

CURRENT LIMIT TRANSIENT SUPPRESSION

When noise spikes and switching transients interfere with proper current limit operation, R1 and C1 act together as a low pass filter to control the current limit circuitry's response time.

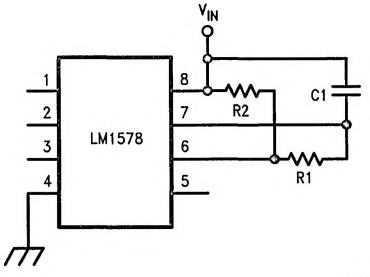
Because the sense current of the current limit terminal varies according to where it is referenced, R1 should be less than 2 kΩ when referenced to ground, and less than 100 Ω when referenced to V_{in}.

Current Limit Transient Suppressor Ground Referred



TL/H/8711–17

Current Limit Transient Suppressor V_{in} Referred

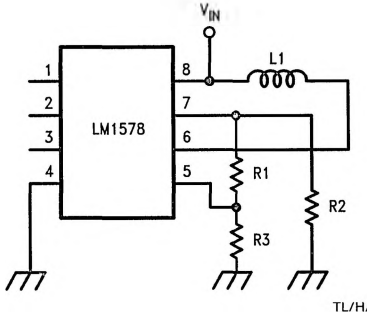


TL/H/8711–18

C. L. SENSE VOLTAGE MULTIPLICATION

When a larger sense resistor value is desired, the voltage divider network, consisting of R1 and R2, may be used. This effectively multiplies the sense voltage by (1 + R1/R2). Also, R_1 can be replaced by a diode to increase current limit sense voltage to about 800 mV (diode V_f + 110 mV).

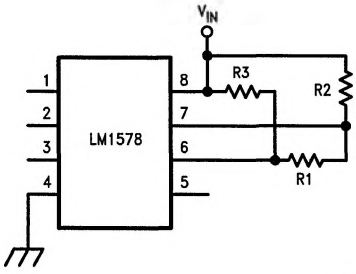
Current Limit Sense Voltage Multiplication Ground Referred



TL/H/8711–19

Typical Applications (Continued)

Current Limit Sense Voltage Multiplication V_{in} Referred



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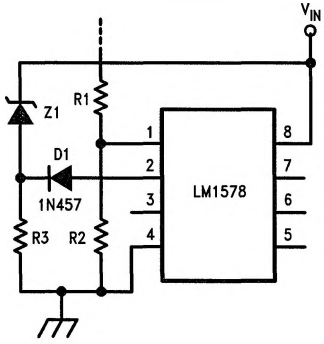
UNDER-VOLTAGE LOCKOUT

Under-voltage lockout is accomplished with few external components. When V_{in} becomes lower than the zener breakdown voltage, the output transistor is turned off. This occurs because diode D1 will then become forward biased, allowing resistor R3 to sink a greater current from the non-inverting input than is sunk by the parallel combination of R1 and R2 at the inverting terminal. R3 should be one-fifth of the value of R1 and R2 in parallel.

Under Voltage Lockout



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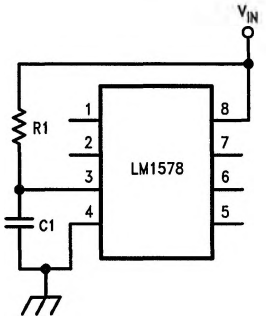
MAXIMUM DUTY CYCLE LIMITING

The maximum duty cycle can be externally limited by adjusting the charge to discharge ratio of the oscillator capacitor with a single external resistor. Typical values are 50 μA for the charge current, 450 μA for the discharge current, and a voltage swing from 200 mV to 750 mV. Therefore, R1 is selected for the desired charging and discharging slopes and C1 is readjusted to set the oscillator frequency.

Maximum Duty Cycle Limiting



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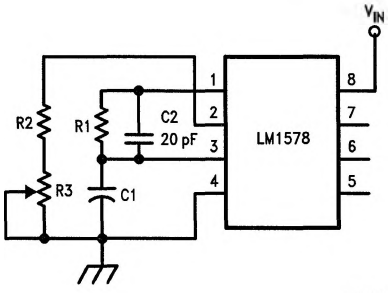
DUTY CYCLE ADJUSTMENT

When manual or mechanical selection of the output transistor's duty cycle is needed, the circuit shown below may be used. The output will turn on with the beginning of each oscillator cycle and turn off when the current sunk by R2 and R3 from the non-inverting terminal becomes greater than the current sunk from the inverting terminal.

R1 should be less than 500 kΩ but greater than 100 kΩ to prevent loading of the oscillator. R2 should be approximately 100 kΩ. R3 is used to adjust the duty cycle.

When the sum of R2 and R3 is twice the value of R1, the duty cycle will be about 50%. Capacitor C1 may be electrolytic to lower the oscillator frequency below 1 Hz.

Duty Cycle Adjustment



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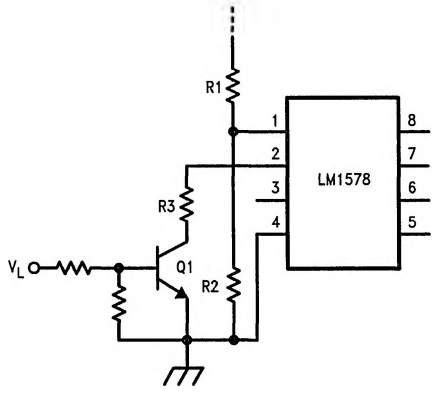
REMOTE SHUTDOWN

The LM1578 may be remotely shutdown by sinking a greater current from the non-inverting input than from the inverting input. This may be accomplished by selecting resistor R3 to be approximately one-half the value of R1 and R2 in parallel.

Typical Applications (Continued)

Remote Shutdown—Shutdown Occurs When V_L is High



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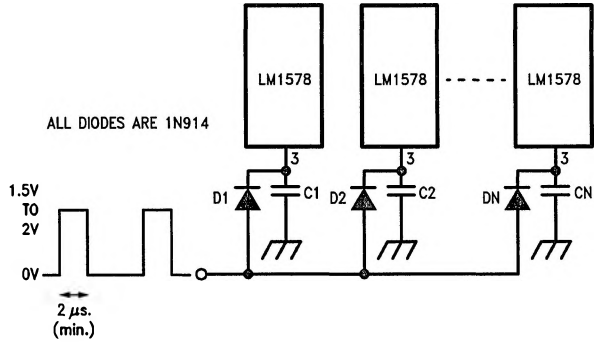
SYNCHRONIZING DEVICES

When several devices are to be operated at once, their oscillators may be synchronized by the application of an external signal. This drive signal should be a pulse waveform with a minimum pulse width of 2 μsec. and an amplitude from 1.5V to 2.0V. The signal source must be capable of 1.) driving capacitive loads and 2.) delivering up to 500 μA for each LM1578.

Capacitors C1 thru CN are to be selected for a 20% slower frequency than the synchronization frequency.

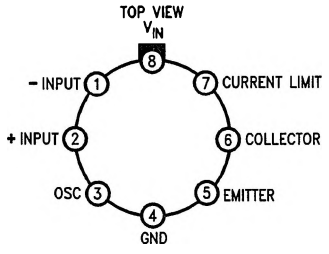
Synchronizing Devices



TL/H/8711–25

Connection Diagram

Metal Can



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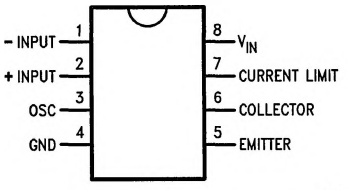
Order Number LM1578H, LM2578H, or LM3578H
See NS Package Number H08C

Dual-In-Line Package



TL/H/8711–27

Order Number LM2578N, LM3578N
See NS Package Number N08E