# QUAD DIFFERENTIAL COMPARATOR
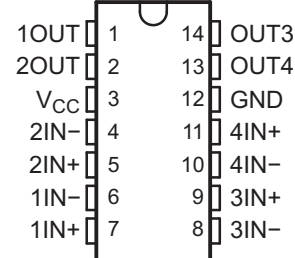
**Check for Samples: LM239A-EP**

## FEATURES

- **Wide Supply Ranges**
  - **Single Supply: 2 V to 36 V (Tested to 30 V for Non-V Devices and 32 V for V-Suffix Devices)**
  - **Dual Supplies: ±1 V to ±18 V (Tested to ±15 V for Non-V Devices and ±16 V for V-Suffix Devices)**
- **Low Supply-Current Drain Independent of Supply Voltage: 0.8 mA (Typ)**
- **Low Input Bias Current: 25 nA (Typ)**
- **Low Input Offset Current: 5 nA (Typ)**
- **Low Input Offset Voltage: 2 mV (Typ)**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: ±36 V**
- **Low Output Saturation Voltage**
- **Output Compatible With TTL, MOS, and CMOS**

## SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**[1]
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

D OR PW PACKAGE
(TOP VIEW)

| | | |
|---|---|---|
| 1OUT | 1 | 14 OUT3 |
| 2OUT | 2 | 13 OUT4 |
| $V_{CC}$ | 3 | 12 GND |
| 2IN− | 4 | 11 4IN+ |
| 2IN+ | 5 | 10 4IN− |
| 1IN− | 6 | 9 3IN+ |
| 1IN+ | 7 | 8 3IN− |

(1) Custom temperature ranges available

## DESCRIPTION/ORDERING INFORMATION

These devices consist of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible, as long as the difference between the two supplies is 2 V to 36 V, and $V_{CC}$ is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## Table 1. ORDERING INFORMATION[1]

| $T_A$ | PACKAGE[2] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 125°C | SOP - D | Tape and reel | LM239AQDREP | LM239AEP |
| −55°C to 125°C | SOP - D | Tape and reel | LM239AMDREP | LM239AME |
| | TSSOP - PW | Tape and reel | LM239AMPWREP | LM239AE |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## SYMBOL (EACH COMPARATOR)
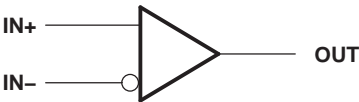


## SCHEMATIC (EACH COMPARATOR)
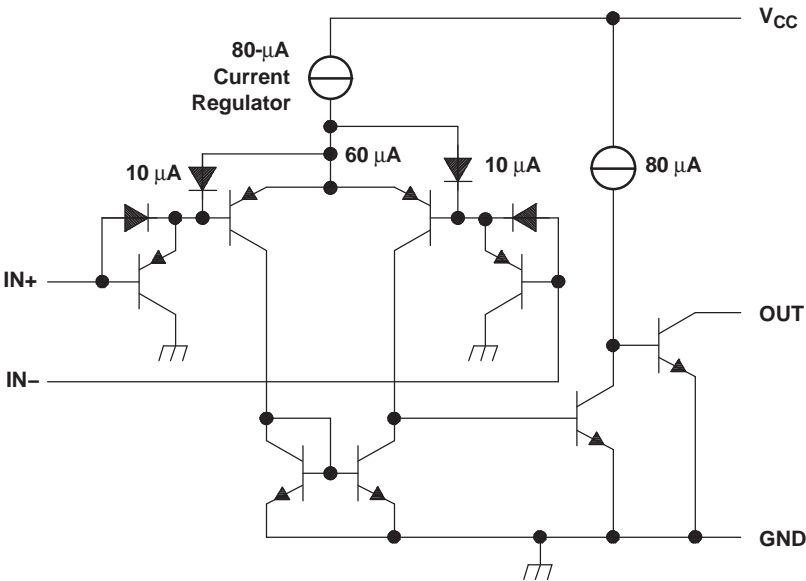


All current values shown are nominal.

Product Folder Link(s): *LM239A-EP*

## ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage[2] | | 36 | V |
| $V_{ID}$ | Differential input voltage[3] | | ±36 | V |
| $V_I$ | Input voltage range (either input) | −0.3 | 36 | V |
| $V_O$ | Output voltage | | 36 | V |
| $I_O$ | Output current | | 20 | mA |
| | Duration of output short circuit to ground[4] | | Unlimited | |
| $\theta_{JA}$ | Package thermal impedance, junction to free air[5] [6] | | 86 | °C/W |
| $T_J$ | Operating virtual-junction temperature | | 136 | °C |
| | Lead temperature 1,6 mm (1/16 in) from case for 10 s | | 260 | °C |
| $T_{stg}$ | Storage temperature range[7] | −65 | 150 | °C |

(1)   Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2)   All voltage values, except differential voltages, are with respect to network ground.

(3)   Differential voltages are at IN+ with respect to IN−.

(4)   Short circuits from outputs to $V_{CC}$ can cause excessive heating and eventual destruction.

(5)   Maximum power dissipation is a function of $T_J$ (max), $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J$ (max) $- T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.

(6)   The package thermal impedance is calculated in accordance with JESD 51-7.

(7)   Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

# LM239A-EP

## ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{CC}$ = 5 V (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS[1] | | $T_A$ [2] | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{CC}$ = 5 V to 30 V, $V_{IC}$ = $V_{ICR}$ min, $V_O$ = 1.4 V | | 25°C | | 1 | 2.5 | mV |
| | | | | Full range | | | 5.5 | |
| $I_{IO}$ | Input offset current | $V_O$ = 1.4 V | | 25°C | | 5 | 50 | nA |
| | | | | Full range | | | 150 | |
| $I_{IB}$ | Input bias current | $V_O$ = 1.4 V | | 25°C | | −25 | −250 | nA |
| | | | | Full range | | | −400 | |
| $V_{ICR}$ | Common-mode input-voltage range[3] | | | 25°C | | 0 to $V_{CC}$ − 1.5 | | V |
| | | | | Full range | | 0 to $V_{CC}$ − 2 | | |
| $A_{VD}$ | Large-signal differential-voltage amplification | $V_{CC}$ = 15 V, $V_O$ = 1.4 V to 11.4 V, $R_L$ ≥ 15 kΩ to $V_{CC}$ | | 25°C | 50 | 200 | | V/mV |
| $I_{OH}$ | High-level output current | $V_{ID}$ = 1 V | $V_{OH}$ = 5 V | 25°C | | 0.1 | 50 | nA |
| | | | $V_{OH}$ = 30 V | Full range | | | 1 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = −1 V, | $I_{OL}$ = 4 mA | 25°C | | 150 | 400 | mV |
| | | | | Full range | | | 700 | |
| $I_{OL}$ | Low-level output current | $V_{ID}$ = −1 V, | $V_{OL}$ = 1.5 V | 25°C | 6 | 16 | | mA |
| $I_{CC}$ | Supply current (four comparators) | $V_O$ = 2.5 V, | No load | 25°C | | 0.8 | 2 | mA |

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) Full range (MIN to MAX) for LM139 and LM139A is −55°C to 125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(3) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+}$ − 1.5 V; however, one input can exceed $V_{CC}$, and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30 V without damage.

## SWITCHING CHARACTERISTICS

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|
| Response time | $R_L$ connected to 5 V through 5.1 kΩ, $C_L$ = 15 pF[1] [2] | 100-mV input step with 5-mV overdrive | 1.3 | μs |
| | | TTL-level input step | 0.3 | |

(1) $C_L$ includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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Product Folder Link(s): *LM239A-EP*

## TYPICAL CHARACTERISTICS

### SUPPLY CURRENT
### vs
### SUPPLY VOLTAGE
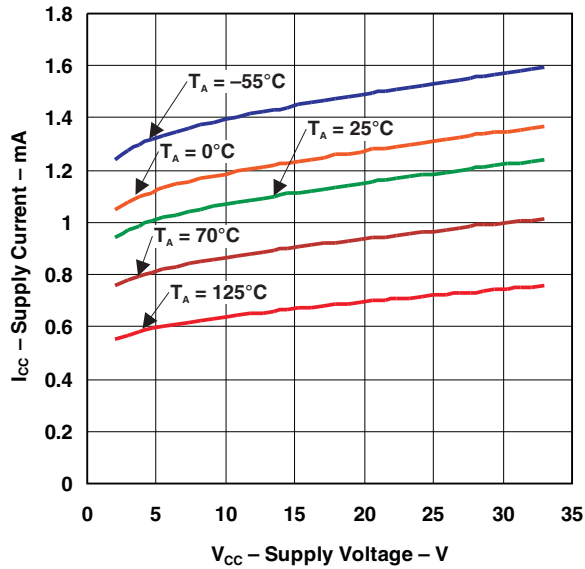


### INPUT BIAS CURRENT
### vs
### SUPPLY VOLTAGE



### OUTPUT SATURATION VOLTAGE

Product Folder Link(s): *LM239A-EP*
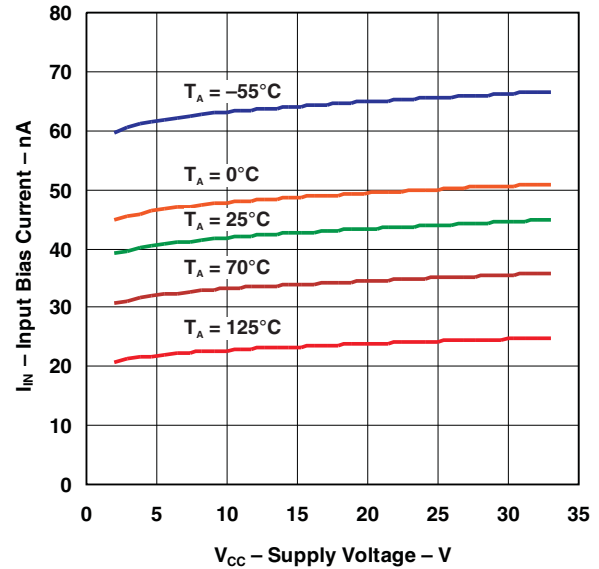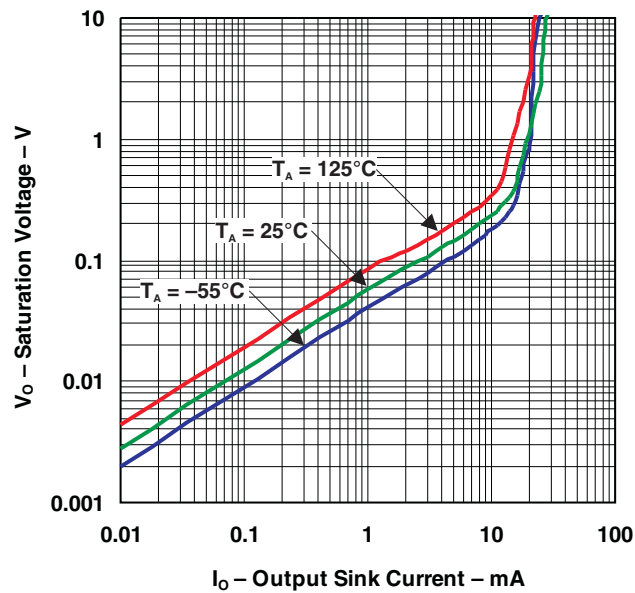
# TYPICAL CHARACTERISTICS (continued)

**RESPONSE TIME FOR VARIOUS OVERDRIVES**
**NEGATIVE TRANSITION**
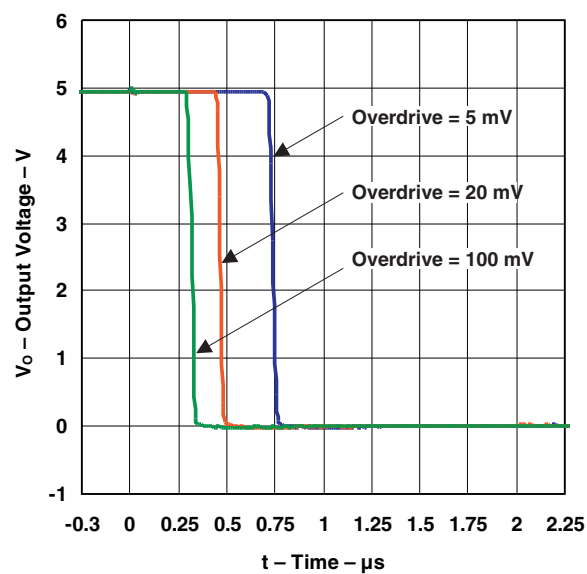
**RESPONSE TIME FOR VARIOUS OVERDRIVES**
**POSITIVE TRANSITION**
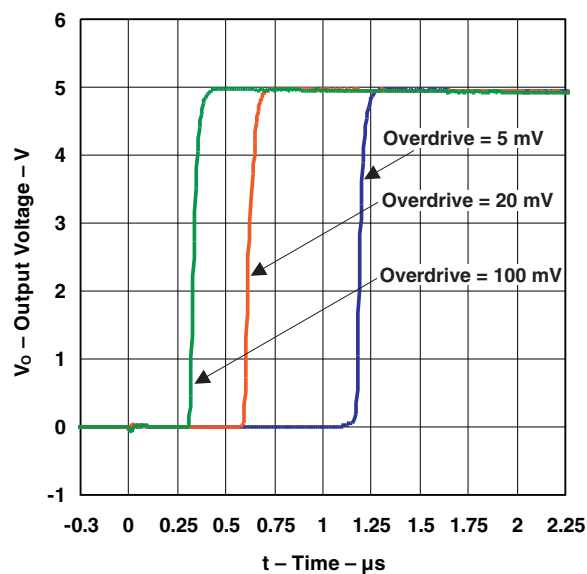
## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| LM239AMDREP | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| LM239AMPWREP | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| LM239AQDREP | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| V62/03672-01XE | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| V62/03672-02XE | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |
| V62/03672-02YE | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Contact TI Distributor or Sales Office |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF LM239A-EP :**

- Catalog: LM239A

- Automotive: LM239A-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

![Texas Instruments logo]

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

## TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM239AMDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LM239AMPWREP | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LM239AQDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| LM239AMDREP | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| LM239AMPWREP | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| LM239AQDREP | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |

D (R−PDSO−G14)                                           PLASTIC SMALL OUTLINE



0.344 (8,75)
0.337 (8,55)
C

14                                    8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)  D

1                                     7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)          0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AB.

**TEXAS INSTRUMENTS**
www.ti.com

D (R−PDSO−G14)                                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x1,27

5,40

Stencil Openings
(Note D)

14x0,55

14x1,50

12x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

0.07
All Around

Example
Solder Mask Opening
(See Note E)

4211283−3/E  08/12
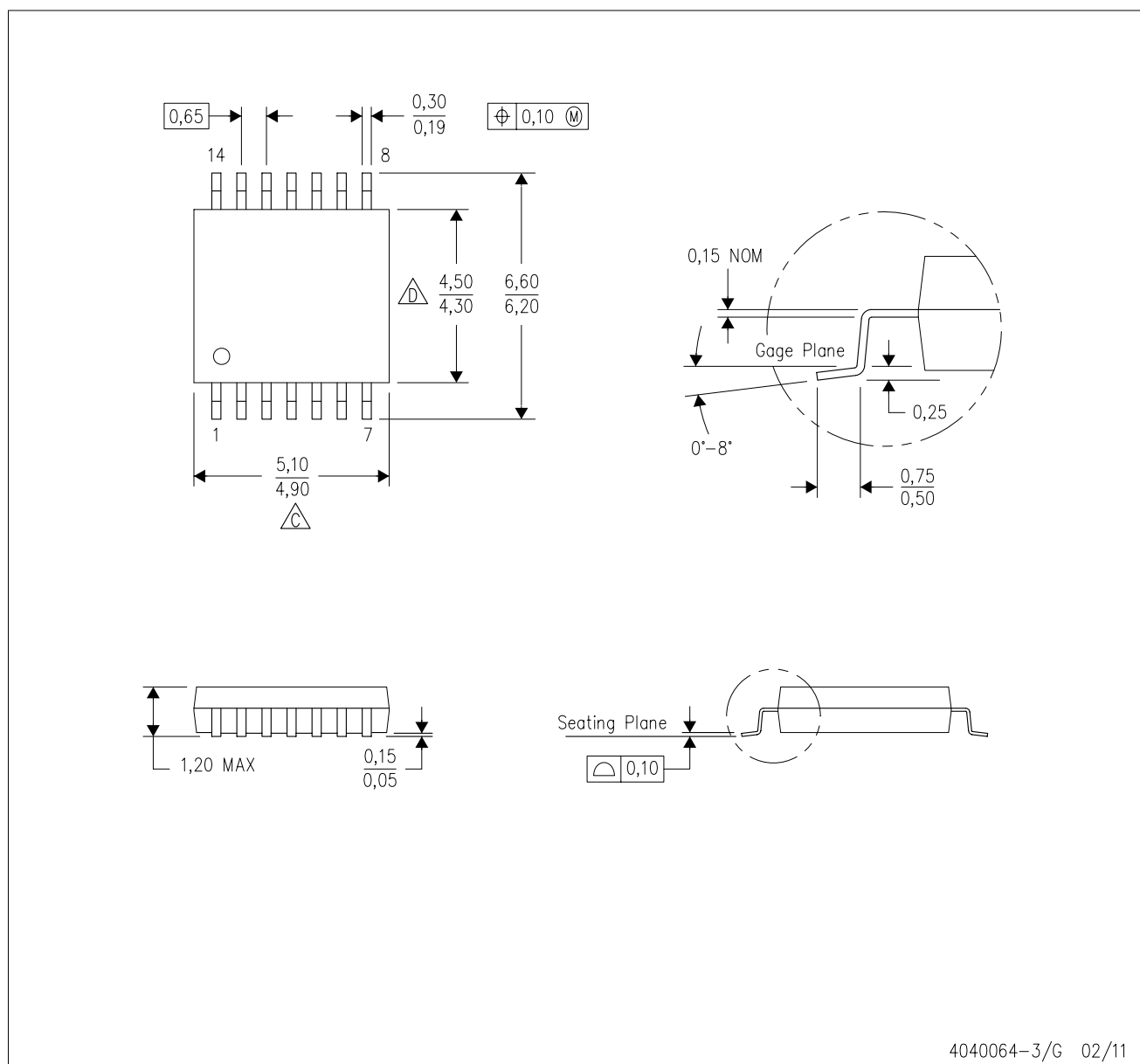
NOTES:    A.  All linear dimensions are in millimeters.
          B.  This drawing is subject to change without notice.
          C.  Publication IPC−7351 is recommended for alternate designs.
          D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
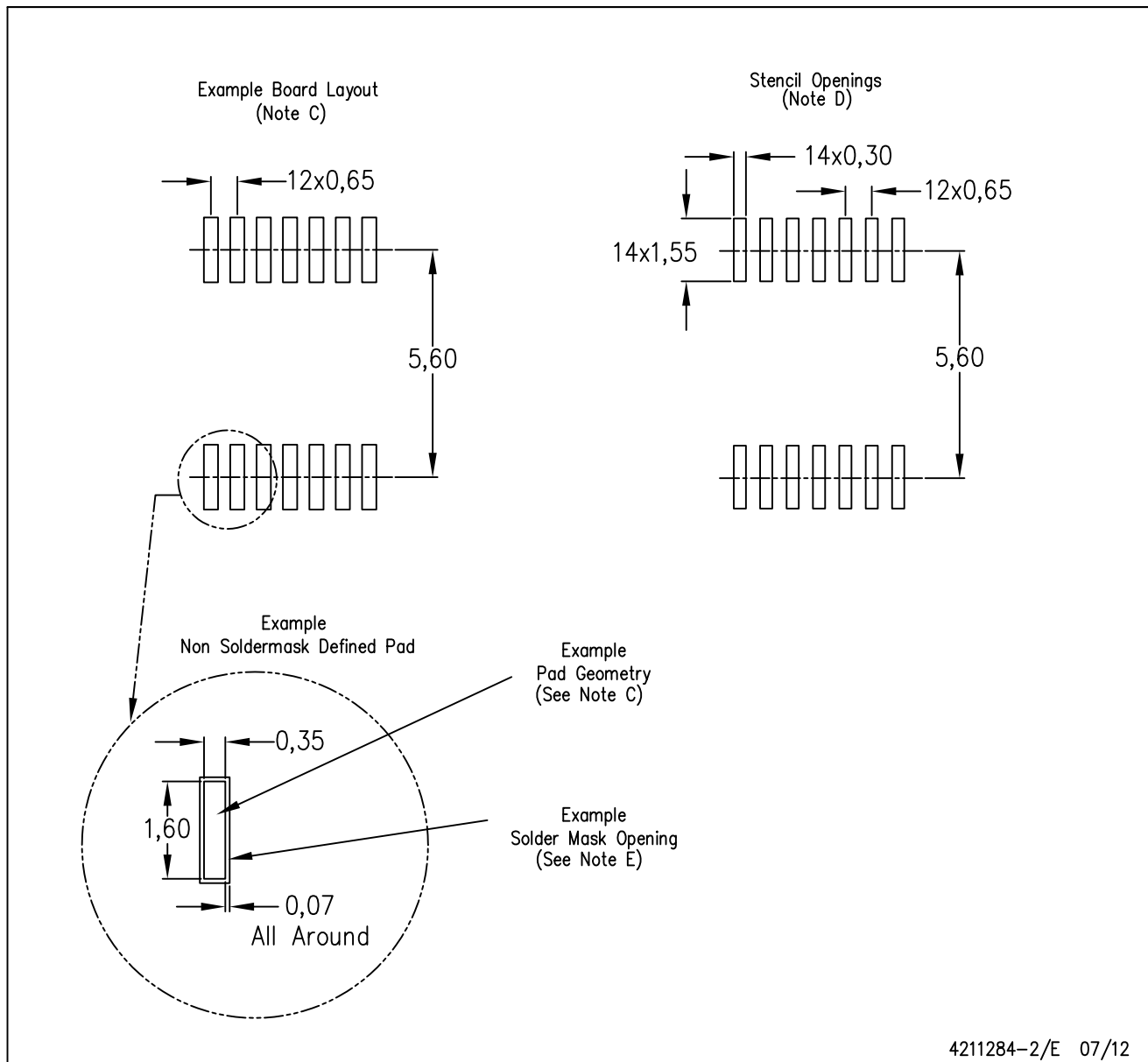
PW (R−PDSO−G14)                    PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14

8

D  4,50
   4,30

6,60
6,20

1        7

5,10
4,90

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌀ 0,10

4040064−3/G  02/11

NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
        Ⓒ   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
        Ⓓ   Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

PW (R–PDSO–G14)                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

←12x0,65

5,60

Stencil Openings
(Note D)

←14x0,30

←12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

←0,35

1,60

Example
Solder Mask Opening
(See Note E)

←0,07
All Around

4211284–2/E  07/12

NOTES:    A.  All linear dimensions are in millimeters.
          B.  This drawing is subject to change without notice.
          C.  Publication IPC–7351 is recommended for alternate designs.
          D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
          E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
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| Logic | logic.ti.com | Security | www.ti.com/security |
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| RFID | www.ti-rfid.com | | |
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