LM2524D/LM3524D Regulating Pulse Width Modulator

Check for Samples: LM2524D, LM3524D

FEATURES

- **Fully interchangeable with standard LM3524 family**
- **±1% precision 5V reference with thermal shut-down**
- **Output current to 200 mA DC**
- **60V output capability**
- **Wide common mode input range for error-amp**
- **One pulse per period (noise suppression)**
- **Improved max. duty cycle at high frequencies**
- **Double pulse suppression**
- **Synchronize through pin 3**

DESCRIPTION

The LM3524D family is an improved version of the industry standard LM3524. It has improved specifications and additional features yet is pin for pin compatible with existing 3524 families. New features reduce the need for additional external circuitry often required in the original version.

The LM3524D has a ±1% precision 5V reference. The current carrying capability of the output drive transistors has been raised to 200 mA while reducing V_{CEsat} and increasing V_{CE} breakdown to 60V. The common mode voltage range of the error-amp has been raised to 5.5V to eliminate the need for a resistive divider from the 5V reference.

In the LM3524D the circuit bias line has been isolated from the shut-down pin. This prevents the oscillator pulse amplitude and frequency from being disturbed by shut-down. Also at high frequencies (≈300 kHz) the max. duty cycle per output has been improved to 44% compared to 35% max. duty cycle in other 3524s.

In addition, the LM3524D can now be synchronized externally, through pin 3. Also a latch has been added to insure one pulse per period even in noisy environments. The LM3524D includes double pulse suppression logic that insures when a shut-down condition is removed the state of the T-flip-flop will change only after the first clock pulse has arrived. This feature prevents the same output from being pulsed twice in a row, thus reducing the possibility of core saturation in push-pull designs.

Connection Diagram

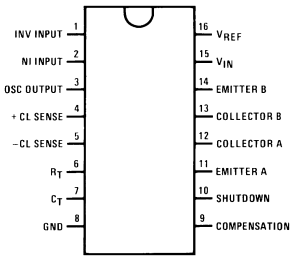
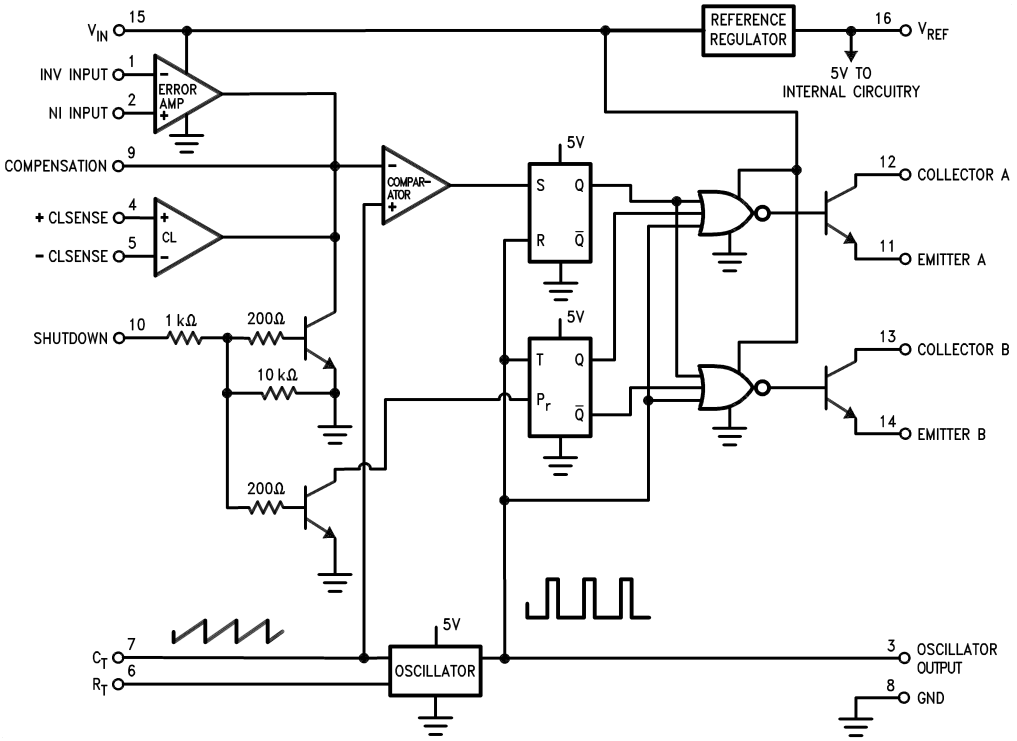


Figure 1. Top View
Order Number LM2524DN or LM3524DN
See NS Package Number N16E
Order Number LM3524DM
See NS Package Number M16A

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage	40V
Collector Supply Voltage	
(LM2524D)	55V
(LM3524D)	40V
Output Current DC (each)	200 mA
Oscillator Charging Current (Pin 7)	5 mA
Internal Power Dissipation	1W
Operating Junction Temperature	
Range (2)	
LM2524D	−40°C to +125°C
LM3524D	0°C to +125°C
Maximum Junction Temperature	150°
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	
M, N Pkg.	260°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) For operation at elevated temperatures, devices in the N package must be derated based on a thermal resistance of 86°C/W, junction to ambient. Devices in the M package must be derated at 125°C/W, junction to ambient.

Electrical Characteristics

			LM2524D			LM3524D			
Symbol	**Parameter**	**Conditions**		**Tested**	**Design**		**Tested**	**Design**	**Units**
			Typ	**Limit**	**Limit**	**Typ**	**Limit**	**Limit**	
				(2)	(3)		(2)	(3)	
REFERENCE SECTION									
V_{REF}	Output Voltage		5	4.85	**4.80**	5	4.75		V_{Min}
				5.15	**5.20**		5.25		V_{Max}
V_{RLine}	Line Regulation	V_{IN} = 8V to 40V	10	15	**30**	10	25	50	mV_{Max}
V_{RLoad}	Load Regulation	I_L = 0 mA to 20 mA	10	15	**25**	10	25	50	mV_{Max}
$\frac{\Delta V_{IN}}{\Delta V_{REF}}$ (1)	Ripple Rejection	f = 120 Hz	66			66			dB
I_{OS}	Short Circuit	V_{REF} = 0		25			25		mA Min
	Current		50			50			
				180			200		mA Max
N_O	Output Noise	10 Hz ≤ f ≤ 10 kHz	40		100	40		100	$\mu V_{rms\ Max}$
	Long Term	T_A = 125°C	20			20			mV/kHr
	Stability								
OSCILLATOR SECTION									
f_{OSC}	Max. Freq.	R_T = 1k, C_T = 0.001 µF	550		500	350			kHz_{Min}
		(4)							
f_{OSC}	Initial	R_T = 5.6k, C_T = 0.01 µF		17.5			17.5		kHz_{Min}
	Accuracy	(4)	20			20			
				22.5			22.5		kHz_{Max}
		R_T = 2.7k, C_T = 0.01 µF		34			30		kHz_{Min}
		(4)	38			38			
				42			46		kHz_{Max}
Δf_{OSC}	Freq. Change	V_{IN} = 8 to 40V	0.5	1		0.5	1.0		$\%_{Max}$
	with V_{IN}								
Δf_{OSC}	Freq. Change	T_A = −55°C to +125°C							
	with Temp.	at 20 kHz R_T = 5.6k,	5			5			%
		C_T = 0.01 µF							
V_{OSC}	Output Amplitude	R_T = 5.6k, C_T = 0.01 µF	3	2.4		3	2.4		V_{Min}
	(Pin 3) (5)								
t_{PW}	Output Pulse	R_T = 5.6k, C_T = 0.01 µF	0.5	1.5		0.5	1.5		μs_{Max}
	Width (Pin 3)								
	Sawtooth Peak	R_T = 5.6k, C_T = 0.01 µF	3.4	3.6	**3.8**		3.8		V_{Max}
	Voltage								
	Sawtooth Valley	R_T = 5.6k, C_T = 0.01 µF	1.1	0.8	**0.6**		0.6		V_{Min}
	Voltage								
ERROR-AMP SECTION									
V_{IO}	Input Offset	V_{CM} = 2.5V	2	8	**10**	2	10		mV_{Max}

(1) Unless otherwise stated, these specifications apply for $T_A = T_J$ = 25°C. Boldface numbers apply over the rated temperature range: LM2524D is −40° to 85°C and LM3524D is 0°C to 70°C. V_{IN} = 20V and f_{OSC} = 20 kHz.
(2) Tested limits are guaranteed and 100% tested in production.
(3) Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage range. These limits are not used to calculate outgoing quality level.
(4) The value of a C_t capacitor can vary with frequency. Careful selection of this capacitor must be made for high frequency operation. Polystyrene was used in this test. NPO ceramic or polypropylene can also be used.
(5) OSC amplitude is measured open circuit. Available current is limited to 1 mA so care must be exercised to limit capacitive loading of fast pulses.

Electrical Characteristics (continued)

(1)

			LM2524D			LM3524D			
Symbol	Parameter	Conditions		Tested	Design		Tested	Design	Units
			Typ	Limit	Limit	Typ	Limit	Limit	
				(2)	(3)		(2)	(3)	
	Voltage								
I_{IB}	Input Bias	V_{CM} = 2.5V	1	8	**10**	1	10		μA_{Max}
	Current								
I_{IO}	Input Offset	V_{CM} = 2.5V	0.5	1.0	**1**	0.5	1		μA_{Max}
	Current								
I_{COSI}	Compensation	$V_{IN(I)} - V_{IN(NI)}$ = 150 mV		65			65		μA_{Min}
	Current (Sink)		95			95			
				125			125		μA_{Max}
I_{COSO}	Compensation	$V_{IN(NI)} - V_{IN(I)}$ = 150 mV		−125			−125		μA_{Min}
	Current (Source)		−95			−95			
				−65			−65		μA_{Max}
A_{VOL}	Open Loop Gain	$R_L = \infty$, V_{CM} = 2.5 V	80	74	**60**	80	70	60	dB_{Min}
VCMR	Common Mode			1.5	**1.4**		1.5		V_{Min}
	Input Voltage Range			5.5	**5.4**		5.5		V_{Max}
CMRR	Common Mode		90	80		90	80		dB_{Min}
	Rejection Ratio								
G_{BW}	Unity Gain	A_{VOL} = 0 dB, V_{CM} = 2.5V	3			2			MHz
	Bandwidth								
V_O	Output Voltage	$R_L = \infty$		0.5			0.5		V_{Min}
	Swing			5.5			5.5		V_{Max}
PSRR	Power Supply	V_{IN} = 8 to 40V	80		70	80	65		db_{Min}
	Rejection Ratio								
COMPARATOR SECTION									
$\frac{t_{ON}}{t_{OSC}}$ (2)	Minimum Duty Cycle	Pin 9 = 0.8V, [R_T = 5.6k, C_T = 0.01 µF]	0	0		0	0		$\%_{Max}$
$\frac{t_{ON}}{t_{OSC}}$ (3)	Maximum Duty Cycle	Pin 9 = 3.9V, [R_T = 5.6k, C_T = 0.01 µF]	49	45		49	45		$\%_{Min}$
$\frac{t_{ON}}{t_{OSC}}$ (4)	Maximum Duty Cycle	Pin 9 = 3.9V, [R_T = 1k, C_T = 0.001 µF]	44	35		44	35		$\%_{Min}$
V_{COMPZ}	Input Threshold	Zero Duty Cycle	1			1			V
	(Pin 9)								
V_{COMPM}	Input Threshold	Maximum Duty Cycle	3.5			3.5			V
	(Pin 9)								
I_{IB}	Input Bias		−1			−1			µA
	Current								
CURRENT LIMIT SECTION									
V_{SEN}	Sense Voltage	$V_{(Pin\ 2)} - V_{(Pin\ 1)} \geq$		180			180		mV_{Min}
		150 mV	200			200			
				220			220		mV_{Max}
TC-V_{sense}	Sense Voltage T.C.		0.2			0.2			mV/°C

Electrical Characteristics (continued)

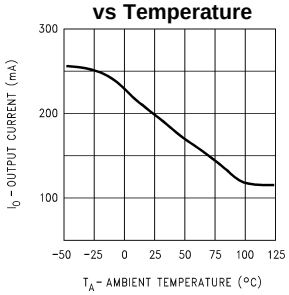
(1)

			LM2524D			LM3524D			
Symbol	**Parameter**	**Conditions**		**Tested**	**Design**		**Tested**	**Design**	**Units**
			Typ	**Limit**	**Limit**	**Typ**	**Limit**	**Limit**	
				(2)	**(3)**		**(2)**	**(3)**	
	Common Mode		−0.7			−0.7			V_{Min}
	Voltage Range	$V_5 - V_4$ = 300 mV	1			1			V_{Max}
SHUT DOWN SECTION									
V_{SD}	High Input	$V_{(Pin\ 2)} - V_{(Pin\ 1)} \geq$	1	0.5		1	0.5		V_{Min}
	Voltage	150 mV		1.5			1.5		V_{Max}
I_{SD}	High Input	$I_{(pin\ 10)}$	1			1			mA
	Current								
OUTPUT SECTION (EACH OUTPUT)									
V_{CES}	Collector Emitter	$I_C \leq$ 100 µA		55			40		V_{Min}
	Voltage Breakdown								
I_{CES}	Collector Leakage	V_{CE} = 60V							
	Current	V_{CE} = 55V	0.1	50					μA_{Max}
		V_{CE} = 40V				0.1	50		
V_{CESAT}	Saturation	I_E = 20 mA	0.2	0.5		0.2	0.7		V_{Max}
	Voltage	I_E = 200 mA	1.5	2.2		1.5	2.5		
V_{EO}	Emitter Output	I_E = 50 mA	18	17		18	17		V_{Min}
	Voltage								
t_R	Rise Time	V_{IN} = 20V,							
		I_E = −250 µA	200			200			ns
		R_C = 2k							
t_F	Fall Time	R_C = 2k	100			100			ns
SUPPLY CHARACTERISTICS SECTION									
V_{IN}	Input Voltage	After Turn-on		8			8		V_{Min}
	Range			40			40		V_{Max}
T	Thermal Shutdown	(6)	160			160			°C
	Temp.								
I_{IN}	Stand By Current	V_{IN} = 40V (7)	5	10		5	10		mA

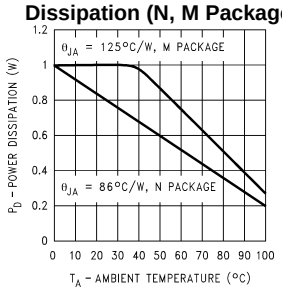
(6) For operation at elevated temperatures, devices in the N package must be derated based on a thermal resistance of 86°C/W, junction to ambient. Devices in the M package must be derated at 125°C/W, junction to ambient.
(7) Pins 1, 4, 7, 8, 11, and 14 are grounded; Pin 2 = 2V. All other inputs and outputs open.

Typical Performance Characteristics

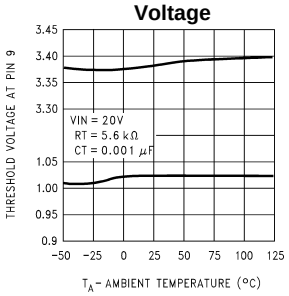
Switching Transistor Peak Output Current vs Temperature



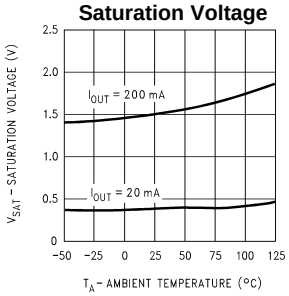
Maximum Average Power Dissipation (N, M Packages)



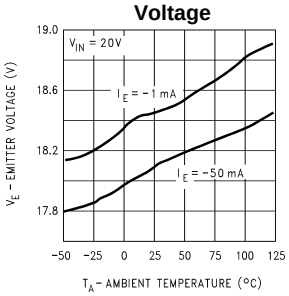
Maximum & Minimum Duty Cycle Threshold Voltage



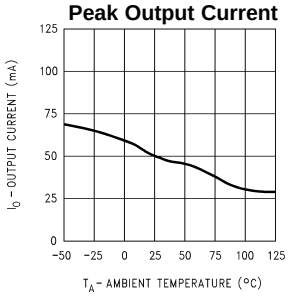
Output Transistor Saturation Voltage



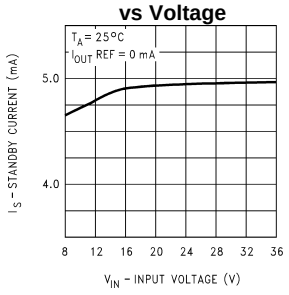
Output Transistor Emitter Voltage



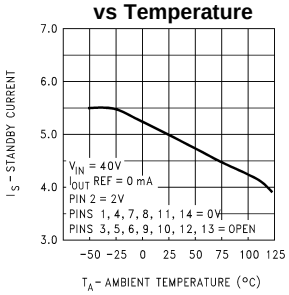
Reference Transistor Peak Output Current



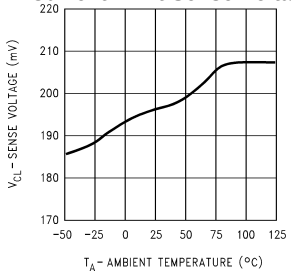
Standby Current vs Voltage



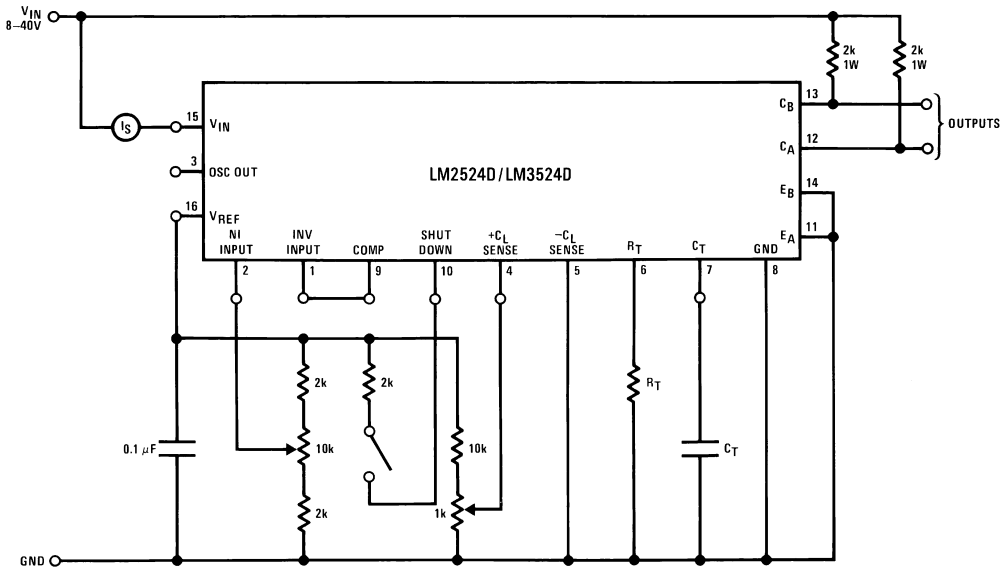
Standby Current vs Temperature



Current Limit Sense Voltage



Test Circuit

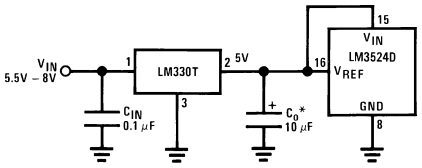


Functional Description

INTERNAL VOLTAGE REGULATOR

The LM3524D has an on-chip 5V, 50 mA, short circuit protected voltage regulator. This voltage regulator provides a supply for all internal circuitry of the device and can be used as an external reference.

For input voltages of less than 8V the 5V output should be shorted to pin 15, V_{IN}, which disables the 5V regulator. With these pins shorted the input voltage must be limited to a maximum of 6V. If input voltages of 6V–8V are to be used, a pre-regulator, as shown in Figure 2, must be added.



*Minimum C_O of 10 μF required for stability.

Figure 2.

OSCILLATOR

The LM3524D provides a stable on-board oscillator. Its frequency is set by an external resistor, R_T and capacitor, C_T. A graph of R_T, C_T vs oscillator frequency is shown is Figure 3. The oscillator's output provides the signals for triggering an internal flip-flop, which directs the PWM information to the outputs, and a blanking pulse to turn off both outputs during transitions to ensure that cross conduction does not occur. The width of the blanking pulse, or dead time, is controlled by the value of C_T, as shown in Figure 4. The recommended values of R_T are 1.8 kΩ to 100 kΩ, and for C_T, 0.001 μF to 0.1 μF.

If two or more LM3524D's must be synchronized together, the easiest method is to interconnect all pin 3 terminals, tie all pin 7's (together) to a single C_T, and leave all pin 6's open except one which is connected to a single R_T. This method works well unless the LM3524D's are more than 6″ apart.

A second synchronization method is appropriate for any circuit layout. One LM3524D, designated as master, must have its R_TC_T set for the correct period. The other slave LM3524D(s) should each have an R_TC_T set for a 10% longer period. All pin 3's must then be interconnected to allow the master to properly reset the slave units.

The oscillator may be synchronized to an external clock source by setting the internal free-running oscillator frequency 10% slower than the external clock and driving pin 3 with a pulse train (approx. 3V) from the clock. Pulse width should be greater than 50 ns to insure full synchronization.

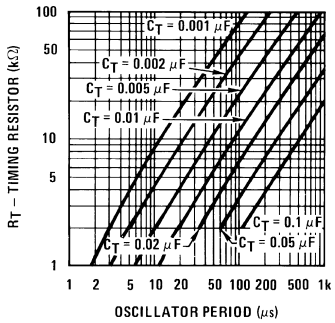


Figure 3.

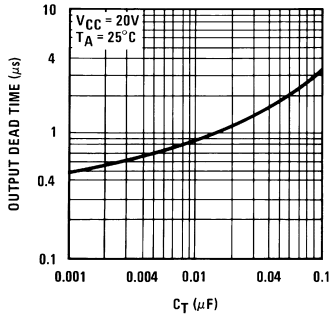


Figure 4.

ERROR AMPLIFIER

The error amplifier is a differential input, transconductance amplifier. Its gain, nominally 86 dB, is set by either feedback or output loading. This output loading can be done with either purely resistive or a combination of resistive and reactive components. A graph of the amplifier's gain vs output load resistance is shown in Figure 5.

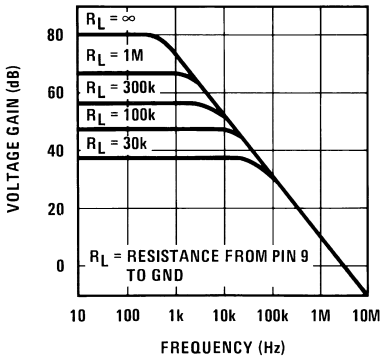


Figure 5.

The output of the amplifier, or input to the pulse width modulator, can be overridden easily as its output impedance is very high ($Z_O \cong 5$ MΩ). For this reason a DC voltage can be applied to pin 9 which will override the error amplifier and force a particular duty cycle to the outputs. An example of this could be a non-regulating motor speed control where a variable voltage was applied to pin 9 to control motor speed. A graph of the output duty cycle vs the voltage on pin 9 is shown in Figure 6.

The duty cycle is calculated as the percentage ratio of each output's ON-time to the oscillator period. Paralleling the outputs doubles the observed duty cycle.

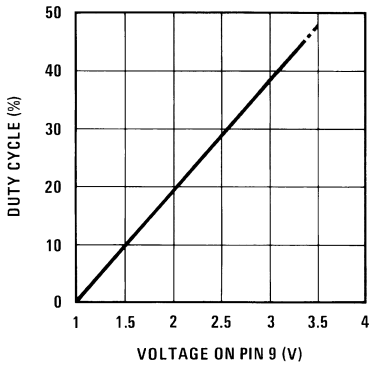


Figure 6.

The amplifier's inputs have a common-mode input range of 1.5V–5.5V. The on board regulator is useful for biasing the inputs to within this range.

CURRENT LIMITING

The function of the current limit amplifier is to override the error amplifier's output and take control of the pulse width. The output duty cycle drops to about 25% when a current limit sense voltage of 200 mV is applied between the $+C_L$ and $-C_L$sense terminals. Increasing the sense voltage approximately 5% results in a 0% output duty cycle. Care should be taken to ensure the −0.7V to +1.0V input common-mode range is not exceeded.

In most applications, the current limit sense voltage is produced by a current through a sense resistor. The accuracy of this measurement is limited by the accuracy of the sense resistor, and by a small offset current, typically 100 µA, flowing from +CL to −CL.

OUTPUT STAGES

The outputs of the LM3524D are NPN transistors, capable of a maximum current of 200 mA. These transistors are driven 180° out of phase and have non-committed open collectors and emitters as shown in Figure 7.

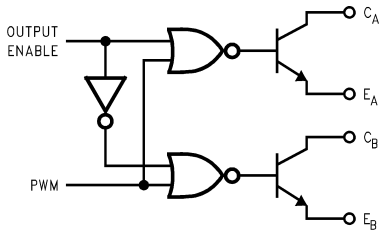


Figure 7.

Typical Applications

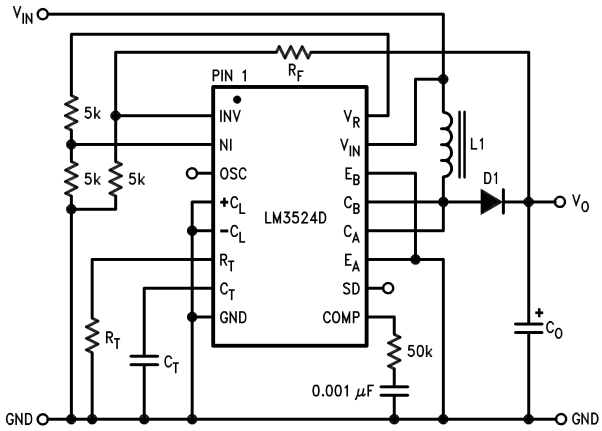


Figure 8. Positive Regulator, Step-Up Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

Design Equations

$$R_F = 5k\left(\frac{V_o}{2.5} - 1\right)$$

$$f_{OSC} \cong \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5 V_{IN}^2 (V_o - V_{IN})}{f_{OSC} I_o V_o^2}$$

$$C_o = \frac{I_o (V_o - V_{IN})}{f_{OSC} \Delta V_o V_o}$$

$$I_{o(MAX)} = I_{IN} \frac{V_{IN}}{V_o} \quad (5)$$

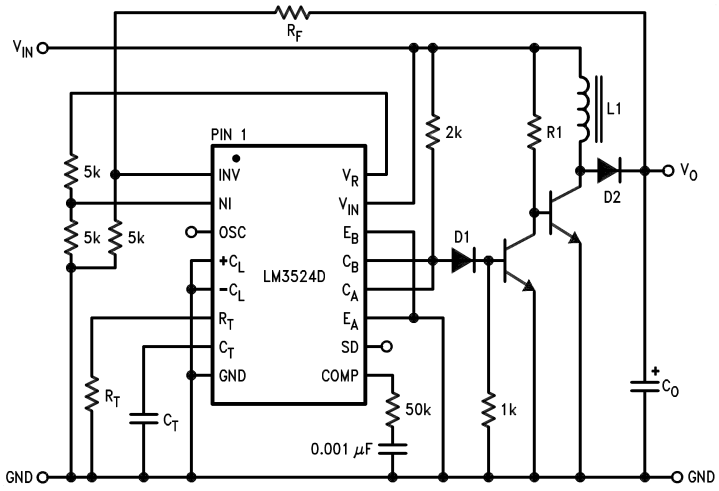


Figure 9. Positive Regulator, Step-Up Boosted Current Configuration

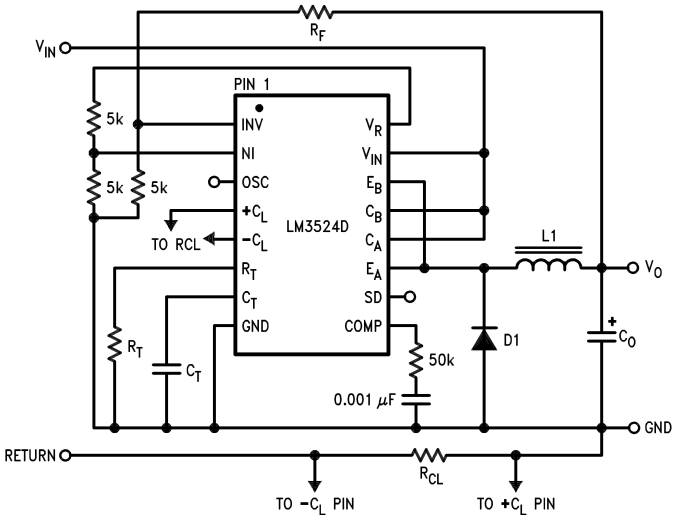


Figure 10. Positive Regulator, Step-Down Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

Design Equations

$$R_F = 5\ k\Omega \left(\frac{V_o}{2.5} - 1\right)$$

$$R_{CL} = \frac{\text{Current Limit Sense Volt}}{I_{o(MAX)}}$$

$$f_{OSC} \cong \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5 V_o (V_{IN} - V_o)}{I_o V_{IN} f_{OSC}}$$

$$C_o = \frac{(V_{IN} - V_o) V_o T^2}{8 \Delta V_o V_{IN} L1}$$

$$I_{o(MAX)} = I_{IN} \frac{V_{IN}}{V_o} \quad (6)$$

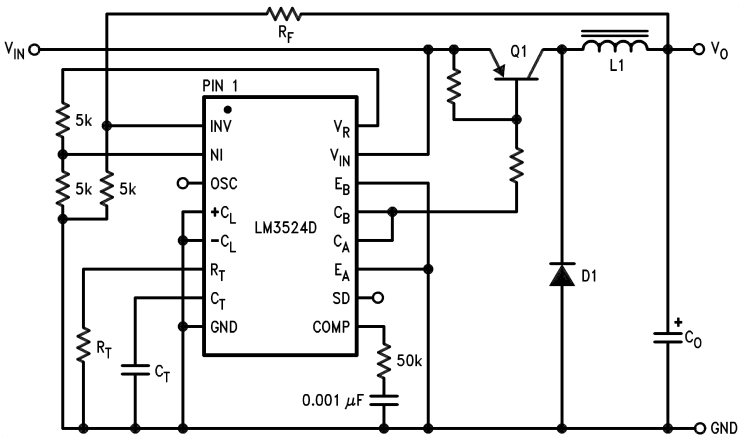


Figure 11. Positive Regulator, Step-Down Boosted Current Configuration

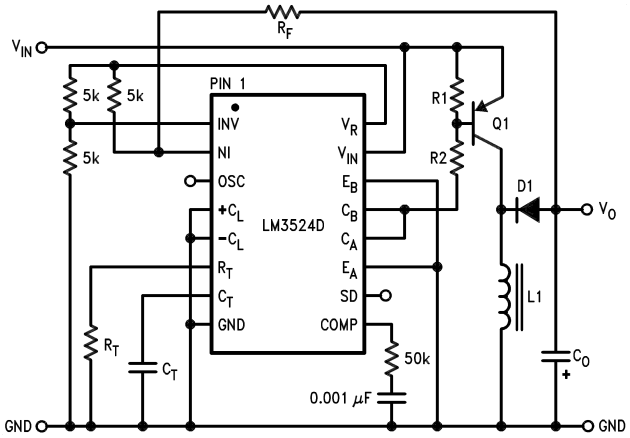


Figure 12. Boosted Current Polarity Inverter

Design Equations

$$R_F = 5k\left(1 - \frac{V_o}{2.5}\right)$$

$$f_{OSC} \cong \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5 V_{IN}\, V_o}{f_{OSC}\,(V_o + V_{IN})\, I_o}$$

$$C_o = \frac{I_o V_o}{\Delta V_o\, f_{OSC}\,(V_o + V_{IN})} \quad (7)$$

BASIC SWITCHING REGULATOR THEORY AND APPLICATIONS

The basic circuit of a step-down switching regulator circuit is shown in Figure 13, along with a practical circuit design using the LM3524D in Figure 16.

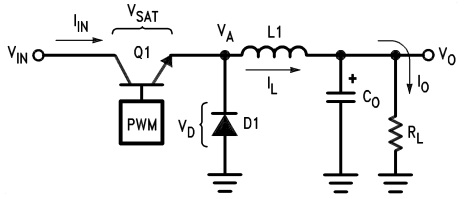


Figure 13. Basic Step-Down Switching Regulator

The circuit works as follows: Q1 is used as a switch, which has ON and OFF times controlled by the pulse width modulator. When Q1 is ON, power is drawn from V_{IN} and supplied to the load through L1; V_A is at approximately V_{IN}, D1 is reverse biased, and C_o is charging. When Q1 turns OFF the inductor L1 will force V_A negative to keep the current flowing in it, D1 will start conducting and the load current will flow through D1 and L1. The voltage at $V_A$is smoothed by the L1, C_o filter giving a clean DC output. The current flowing through L1 is equal to the nominal DC load current plus some ΔI_L which is due to the changing voltage across it. *A good rule of thumb is to set* $\Delta I_{LP\text{-}P} \cong 40\% \times I_o$.

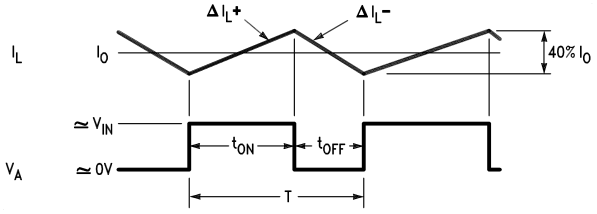


Figure 14. Relation of Switch Timing to Inductor Current in Step-Down Regulator

$$\text{From the relation } V_L = L\frac{d_i}{d_t},\ \Delta I_L \cong \frac{V_L T}{L1}$$

$$\Delta I_L{}^{+} = \frac{(V_{IN} - V_o)\, t_{ON}}{L1};\ \Delta I_L{}^{-} = \frac{V_o\, t_{OFF}}{L1} \tag{8}$$

Neglecting V_{SAT}, V_D, and settling $\Delta I_L{}^{+} = \Delta I_L{}^{-}$;

$$\boxed{V_o \cong V_{IN}\left(\frac{t_{ON}}{t_{OFF} + t_{ON}}\right)} = V_{IN}\left(\frac{t_{ON}}{T}\right); \tag{9}$$

where T = Total Period

The above shows the relation between V_{IN}, V_o and duty cycle.

$$I_{IN(DC)} = I_{OUT(DC)}\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right), \tag{10}$$

as Q1 only conducts during t_{ON}.

$$P_{IN} = I_{IN(DC)}\, V_{IN} = (I_{o(DC)})\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right) V_{IN}$$

$$P_o = I_o V_o \tag{11}$$

The efficiency, η, of the circuit is:

$$\eta MAX = \frac{P_o}{P_{IN}} = \frac{I_o V_o}{I_o \frac{(t_{ON})}{T} V_{IN} + \frac{(V_{SAT}\, t_{ON} + V_{D1} t_{OFF})}{T} I_o}$$

$$= \boxed{\frac{V_o}{V_o + 1}} \text{ for } V_{SAT} = V_{D1} = 1V. \tag{12}$$

ηMAX will be further decreased due to switching losses in Q1. For this reason Q1 should be selected to have the maximum possible f_T, which implies very fast rise and fall times.

CALCULATING INDUCTOR L1

$$t_{ON} \cong \frac{(\Delta I_L{}^{+}) \times L1}{(V_{IN} - V_o)},\ t_{OFF} = \frac{(\Delta I_L{}^{-}) \times L1}{V_o}$$

$$t_{ON} + t_{OFF} = T = \frac{(\Delta I_L{}^{+}) \times L1}{(V_{IN} - V_Q)} + \frac{(\Delta I_L{}^{-}) \times L1}{V_o}$$

$$= \frac{0.4 I_o L1}{(V_{IN} - V_o)} + \frac{0.4 I_o L1}{V_o} \tag{13}$$

Since $\Delta I_L{}^{+} = \Delta I_L{}^{-} = 0.4 I_o$

Solving the above for L1

$$\boxed{L1 = \frac{2.5\, V_o\, (V_{IN} - V_o)}{I_o\, V_{IN}\, f}} \tag{14}$$

where: L1 is in Henrys

f is switching frequency in Hz

Also, see LM1578 data sheet for graphical methods of inductor selection.

CALCULATING OUTPUT FILTER CAPACITOR C_o:

Figure 14 shows L1's current with respect to Q1's t_{ON} and t_{OFF} times (V_A is at the collector of Q1). This curent must flow to the load and C_o. C_o's current will then be the difference between I_L, and I_o.

$$Ic_o = I_L - I_o \tag{15}$$

From Figure 14 it can be seen that current will be flowing into C_o for the second half of t_{ON} through the first half of t_{OFF}, or a time, $t_{ON}/2 + t_{OFF}/2$. The current flowing for this time is $\Delta I_L/4$. The resulting ΔV_c or ΔV_o is described by:

$$\Delta V_{op\text{-}p} = \frac{1}{C} \times \frac{\Delta I_L}{4} \times \left(\frac{t_{ON}}{2} + \frac{t_{OFF}}{2}\right)$$

$$= \frac{\Delta I_L}{4C}\left(\frac{t_{ON} + t_{OFF}}{2}\right)$$

$$\text{Since } \Delta I_L = \frac{V_o(T - t_{ON})}{L1} \text{ and } t_{ON} = \frac{V_o T}{V_{IN}}$$

$$\Delta V_{op\text{-}p} = \frac{V_o\left(T - \frac{V_o T}{V_{IN}}\right)}{4C\,L1}\left(\frac{T}{2}\right) = \frac{(V_{IN} - V_o)\,V_o T^2}{8 V_{IN} C_o L1} \text{ or}$$

$$\boxed{C_o = \frac{(V_{IN} - V_o)\,V_o\,T^2}{8 \Delta V_o V_{IN} L1}}$$

where: C is in farads, T is $\frac{1}{\text{switching frequency}}$

ΔV_o is p-p output ripple (16)

For best regulation, the inductor's current cannot be allowed to fall to zero. Some minimum load current I_o, and thus inductor current, is required as shown below:

$$I_{o(MIN)} = \frac{(V_{IN} - V_o)\,t_{ON}}{2L1} = \boxed{\frac{(V_{IN} - V_o)\,V_o}{2 f V_{IN} L1}} \quad (17)$$

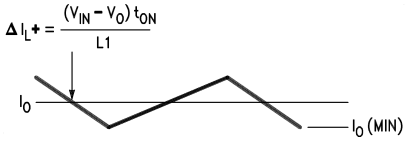


Figure 15. Inductor Current Slope in Step-Down Regulator

A complete step-down switching regulator schematic, using the LM3524D, is illustrated in Figure 16. Transistors Q1 and Q2 have been added to boost the output to 1A. The 5V regulator of the LM3524D has been divided in half to bias the error amplifier's non-inverting input to within its common-mode range. Since each output transistor is on for half the period, actually 45%, they have been paralleled to allow longer possible duty cycle, up to 90%. This makes a lower possible input voltage. The output voltage is set by:

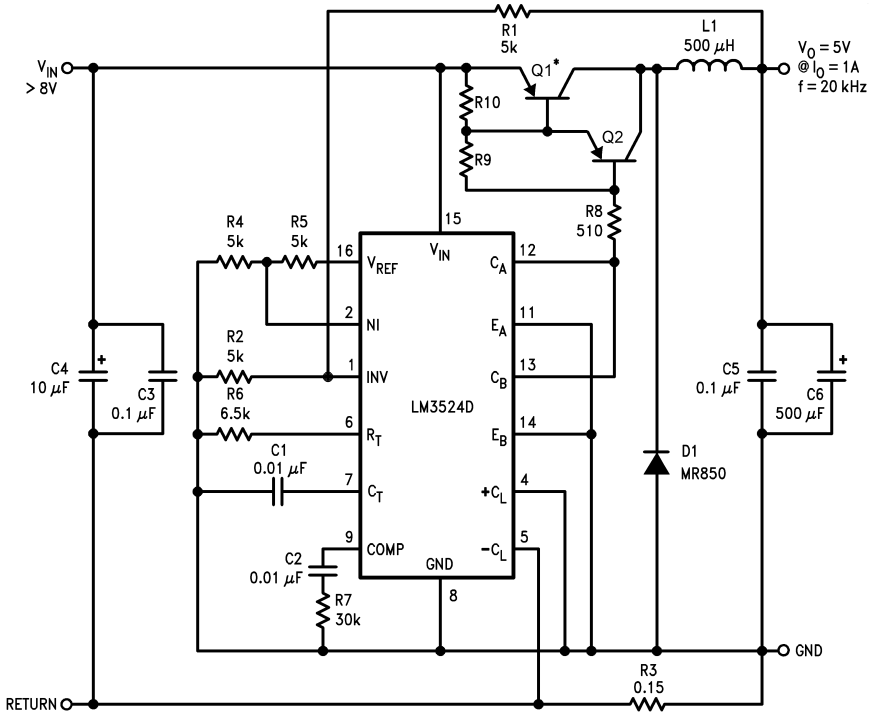
$$V_o = V_{NI}\left(1 + \frac{R1}{R2}\right), \quad (18)$$

where V_{NI} is the voltage at the error amplifier's non-inverting input.

Resistor R3 sets the current limit to:

$$\frac{200\text{ mV}}{R3} = \frac{200\text{ mV}}{0.15} = 1.3\text{A}. \quad (19)$$

Figure 17 and Figure 18 show a PC board layout and stuffing diagram for the 5V, 1A regulator of Figure 16. The regulator's performance is listed in Table 1.



*Mounted to Staver Heatsink No. V5-1.
Q1 = BD344
Q2 = 2N5023
L1 = >40 turns No. 22 wire on Ferroxcube No. K300502 Torroid core.

Figure 16. 5V, 1 Amp Step-Down Switching Regulator

Table 1.

Parameter	Conditions	Typical
		Characteristics
Output Voltage	V_{IN} = 10V, I_o = 1A	5V
Switching Frequency	V_{IN} = 10V, I_o = 1A	20 kHz
Short Circuit	V_{IN} = 10V	1.3A
Current Limit		
Load Regulation	V_{IN} = 10V	3 mV
	I_o = 0.2 − 1A	
Line Regulation	ΔV_{IN} = 10 − 20V,	6 mV
	I_o = 1A	
Efficiency	V_{IN} = 10V, I_o = 1A	80%
Output Ripple	V_{IN} = 10V, I_o = 1A	10 mVp-p

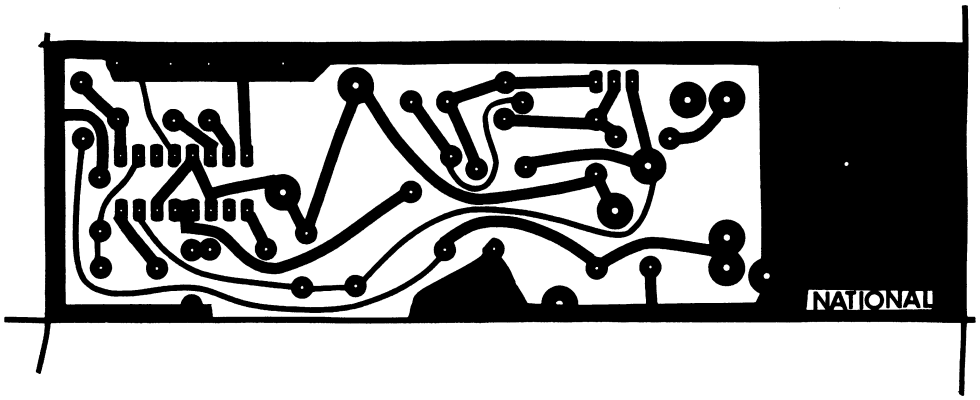


Figure 17. 5V, 1 Amp Switching Regulator, Foil Side

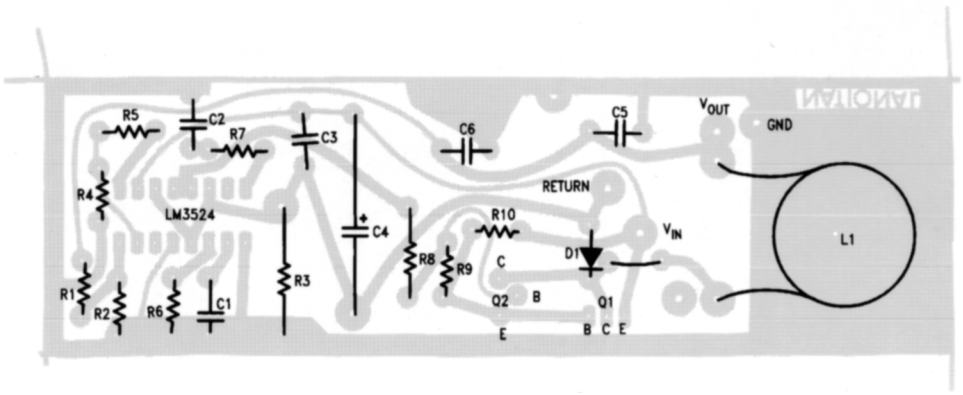


Figure 18. Stuffing Diagram, Component Side

THE STEP-UP SWITCHING REGULATOR

Figure 19 shows the basic circuit for a step-up switching regulator. In this circuit Q1 is used as a switch to alternately apply V_{IN} across inductor L1. During the time, t_{ON}, Q1 is ON and energy is drawn from V_{IN} and stored in L1; D1 is reverse biased and I_o is supplied from the charge stored in C_o. When Q1 opens, t_{OFF}, voltage V1 will rise positively to the point where D1 turns ON. The output current is now supplied through L1, D1 to the load and any charge lost from C_o during t_{ON} is replenished. Here also, as in the step-down regulator, the current through L1 has a DC component plus some ΔI_L. ΔI_L is again selected to be approximately 40% of I_L. Figure 20 shows the inductor's current in relation to Q1's ON and OFF times.

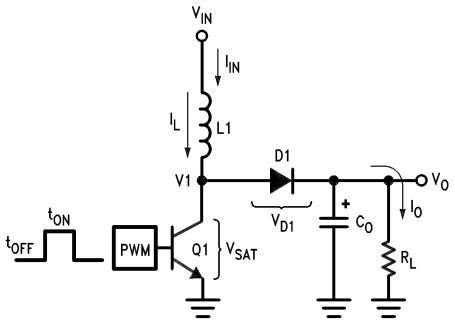


Figure 19. Basic Step-Up Switching Regulator

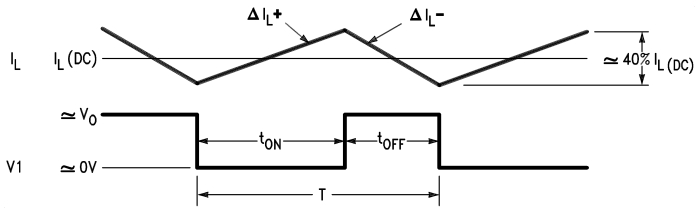


Figure 20. Relation of Switch Timing to Inductor Current in Step-Up Regulator

$$\text{From } \Delta I_L = \frac{V_L T}{L},\ \Delta I_L{}^{+} \cong \frac{V_{IN} t_{ON}}{L1}$$
$$\text{and } \Delta I_L{}^{-} \cong \frac{(V_o - V_{IN})\, t_{OFF}}{L1} \tag{20}$$

Since $\Delta I_L+ = \Delta I_L-$, $V_{IN}t_{ON} = V_o t_{OFF} - V_{IN}t_{OFF}$,

and neglecting V_{SAT} and V_{D1}

$$\boxed{V_o \cong V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)} \tag{21}$$

The above equation shows the relationship between V_{IN}, V_o and duty cycle.

In calculating input current $I_{IN(DC)}$, which equals the inductor's DC current, assume first 100% efficiency:

$$P_{IN} = I_{IN(DC)}\, V_{IN}$$
$$P_{OUT} = I_o V_o = I_o\, V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right) \tag{22}$$

for $\eta = 100\%$, $P_{OUT} = P_{IN}$

$$I_o\, V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right) = I_{IN(DC)}\, V_{IN}$$
$$I_{IN(DC)} = I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right) \tag{23}$$

This equation shows that the input, or inductor, current is larger than the output current by the factor ($1 + t_{ON}/t_{OFF}$). Since this factor is the same as the relation between V_o and V_{IN}, $I_{IN(DC)}$ can also be expressed as:

$$\boxed{I_{IN(DC)} = I_o\left(\frac{V_o}{V_{IN}}\right)} \tag{24}$$

So far it is assumed $\eta = 100\%$, where the actual efficiency or η_{MAX} will be somewhat less due to the saturation voltage of Q1 and forward on voltage of D1. The internal power loss due to these voltages is the average I_L current flowing, or I_{IN}, through either V_{SAT} or V_{D1}. For $V_{SAT} = V_{D1} = 1V$ this power loss becomes $I_{IN(DC)}$ (1V). η_{MAX} is then:

$$\eta_{MAX} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_{IN}\,(1V)} = \frac{V_O I_O}{V_O I_O + I_O\left(1 + \frac{t_{ON}}{t_{OFF}}\right)} \tag{25}$$

$$\text{From } V_o = V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$
$$\boxed{\eta_{max} = \frac{V_{IN}}{V_{IN} + 1}} \tag{26}$$

This equation assumes only DC losses, however η_{MAX} is further decreased because of the switching time of Q1 and D1.

In calculating the output capacitor C_o it can be seen that C_o supplies I_o during t_{ON}. The voltage change on C_o during this time will be some $\Delta V_c = \Delta V_o$ or the output ripple of the regulator. Calculation of C_o is:

$$\Delta V_o = \frac{I_o t_{ON}}{C_o} \text{ or } C_o = \frac{I_o t_{ON}}{\Delta V_o}$$

$$\text{From } V_o = V_{IN}\left(\frac{T}{t_{OFF}}\right); t_{OFF} = \frac{V_{IN}}{V_o} T$$

$$\text{where } T = t_{ON} + t_{OFF} = \frac{1}{f}$$

$$t_{ON} = T - \frac{V_{IN}}{V_o} T = T\left(\frac{V_o - V_{IN}}{V_o}\right) \text{ therefore:}$$

$$C_o = \frac{I_o T\left(\frac{V_o - V_{IN}}{V_o}\right)}{\Delta V_o} = \boxed{\frac{I_o (V_o - V_{IN})}{f \Delta V_o V_o}} \quad (27)$$

where: C_o is in farads, f is the switching frequency,

ΔV_o is the p-p output ripple

Calculation of inductor L1 is as follows:

$$L1 = \frac{V_{IN} t_{ON}}{\Delta I_L^+}, \text{ since during } t_{ON}, \quad (28)$$

V_{IN} is applied across L1

$$\Delta I_{Lp\text{-}p} = 0.4\, I_L = 0.41\, I_{IN} = 0.4\, I_o \left(\frac{V_o}{V_{IN}}\right), \text{ therefore:}$$

$$L1 = \frac{V_{IN} t_{ON}}{0.4\, I_o \left(\frac{V_o}{V_{IN}}\right)} \text{ and since } t_{ON} = \frac{T (V_o - V_{IN})}{V_o}$$

$$\boxed{L1 = \frac{2.5\, V_{IN}^2 (V_o - V_{IN})}{f\, I_o V_o^2}} \quad (29)$$

where: L1 is in henrys, f is the switching frequency in Hz

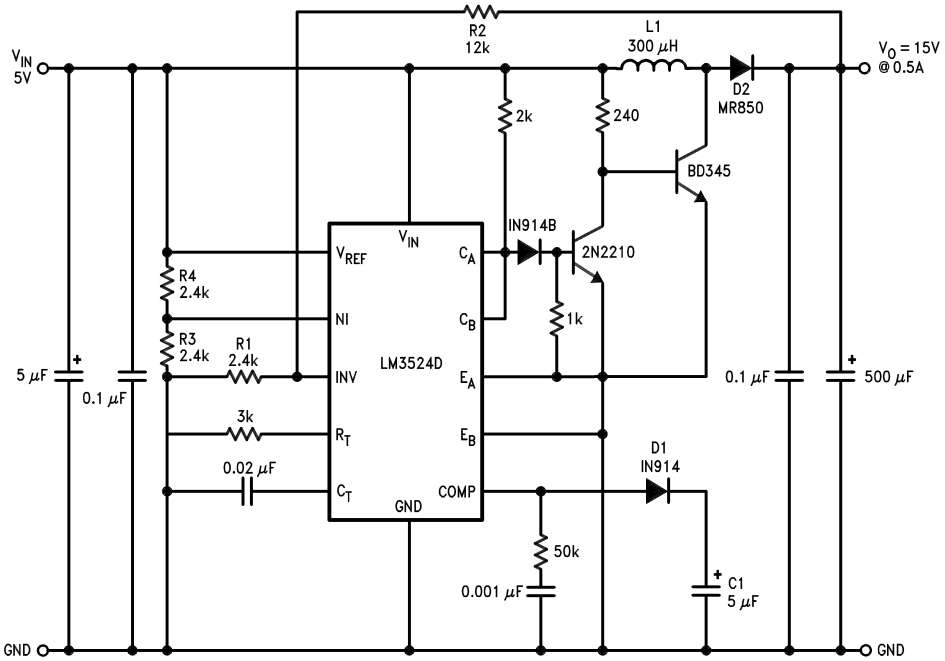
To apply the above theory, a complete step-up switching regulator is shown in Figure 21. Since V_{IN} is 5V, V_{REF} is tied to V_{IN}. The input voltage is divided by 2 to bias the error amplifier's inverting input. The output voltage is:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \times V_{INV} = 2.5 \times \left(1 + \frac{R2}{R1}\right) \quad (30)$$

The network D1, C1 forms a slow start circuit.

This holds the output of the error amplifier initially low thus reducing the duty-cycle to a minimum. Without the slow start circuit the inductor may saturate at turn-on because it has to supply high peak currents to charge the output capacitor from 0V. It should also be noted that this circuit has no supply rejection. By adding a reference voltage at the non-inverting input to the error amplifier, see Figure 22, the input voltage variations are rejected.

The LM3524D can also be used in inductorless switching regulators. Figure 23 shows a polarity inverter which if connected to Figure 21 provides a −15V unregulated output.



L1 = > 25 turns No. 24 wire on Ferroxcube No. K300502 Toroid core.

Figure 21. 15V, 0.5A Step-Up Switching Regulator

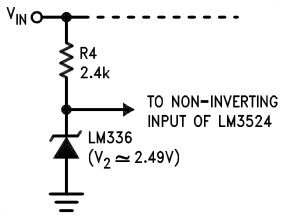


Figure 22. Replacing R3/R4 Divider in Figure 21 with Reference Circuit Improves Line Regulation

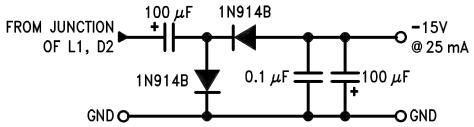


Figure 23. Polarity Inverter Provides Auxiliary −15V Unregulated Output from Circuit of Figure 21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2524DN/NOPB	ACTIVE	PDIP	NFG	16	25	Pb-Free (RoHS)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2524DN	Samples
LM3524DM	ACTIVE	SOIC	D	16	48	TBD	Call TI	Call TI	0 to 80	LM3524DM	Samples
LM3524DM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 80	LM3524DM	Samples
LM3524DMX	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 80	LM3524DM	Samples
LM3524DMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 80	LM3524DM	Samples
LM3524DN	ACTIVE	PDIP	NFG	16	25	TBD	Call TI	Call TI	0 to 80	LM3524DN	Samples
LM3524DN/NOPB	ACTIVE	PDIP	NFG	16	25	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	0 to 80	LM3524DN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

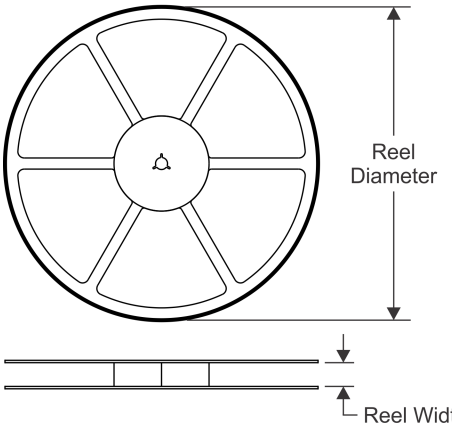
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

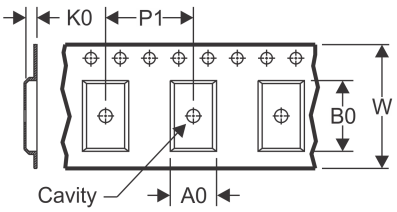
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

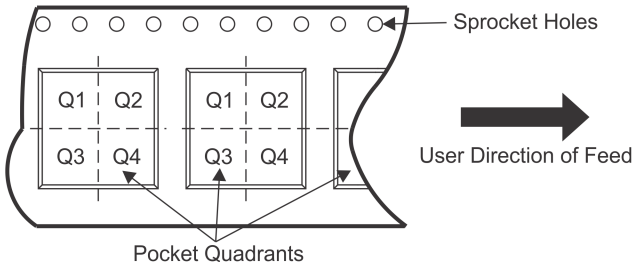


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

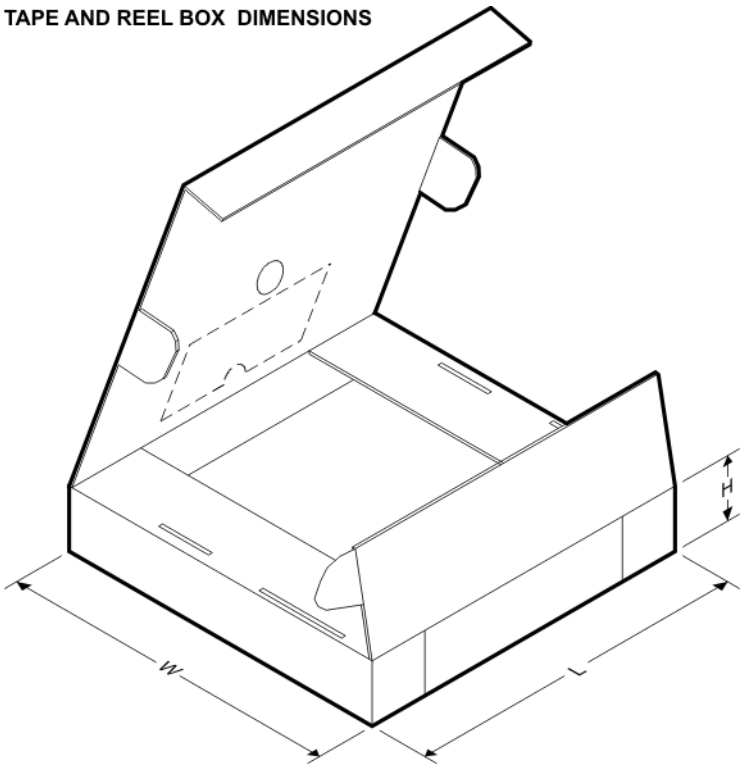
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3524DMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LM3524DMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

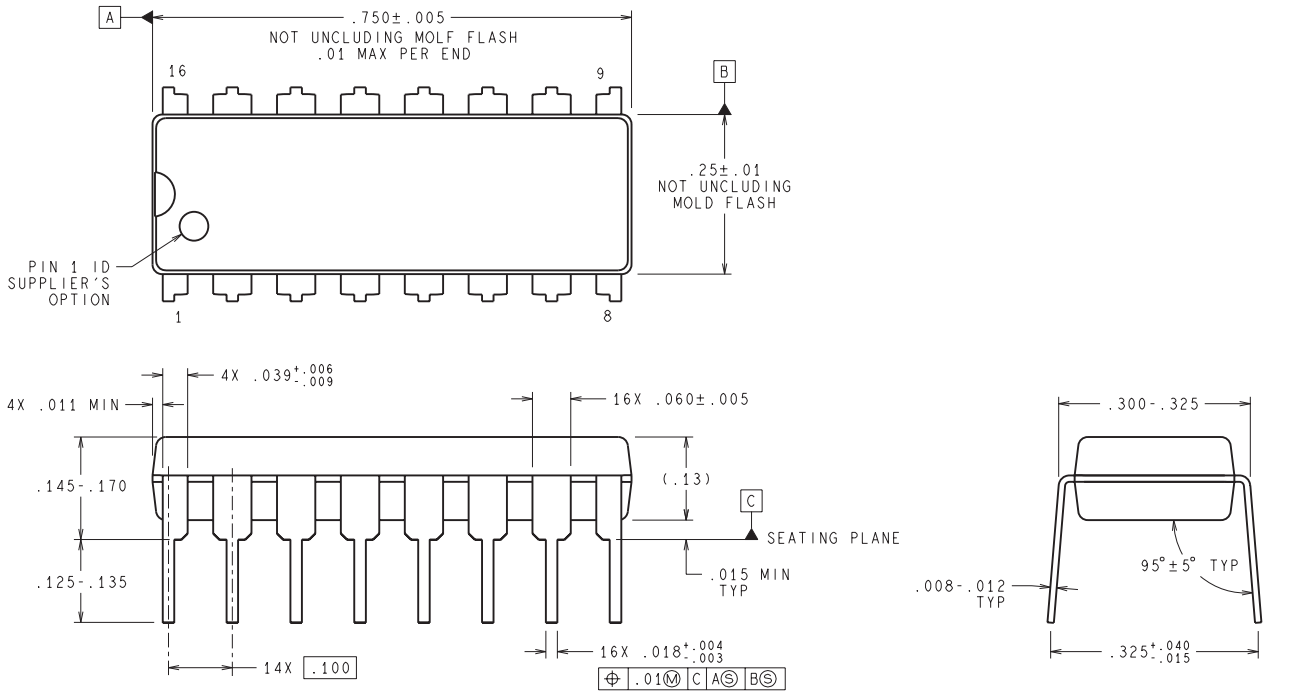
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3524DMX	SOIC	D	16	2500	349.0	337.0	45.0
LM3524DMX/NOPB	SOIC	D	16	2500	349.0	337.0	45.0

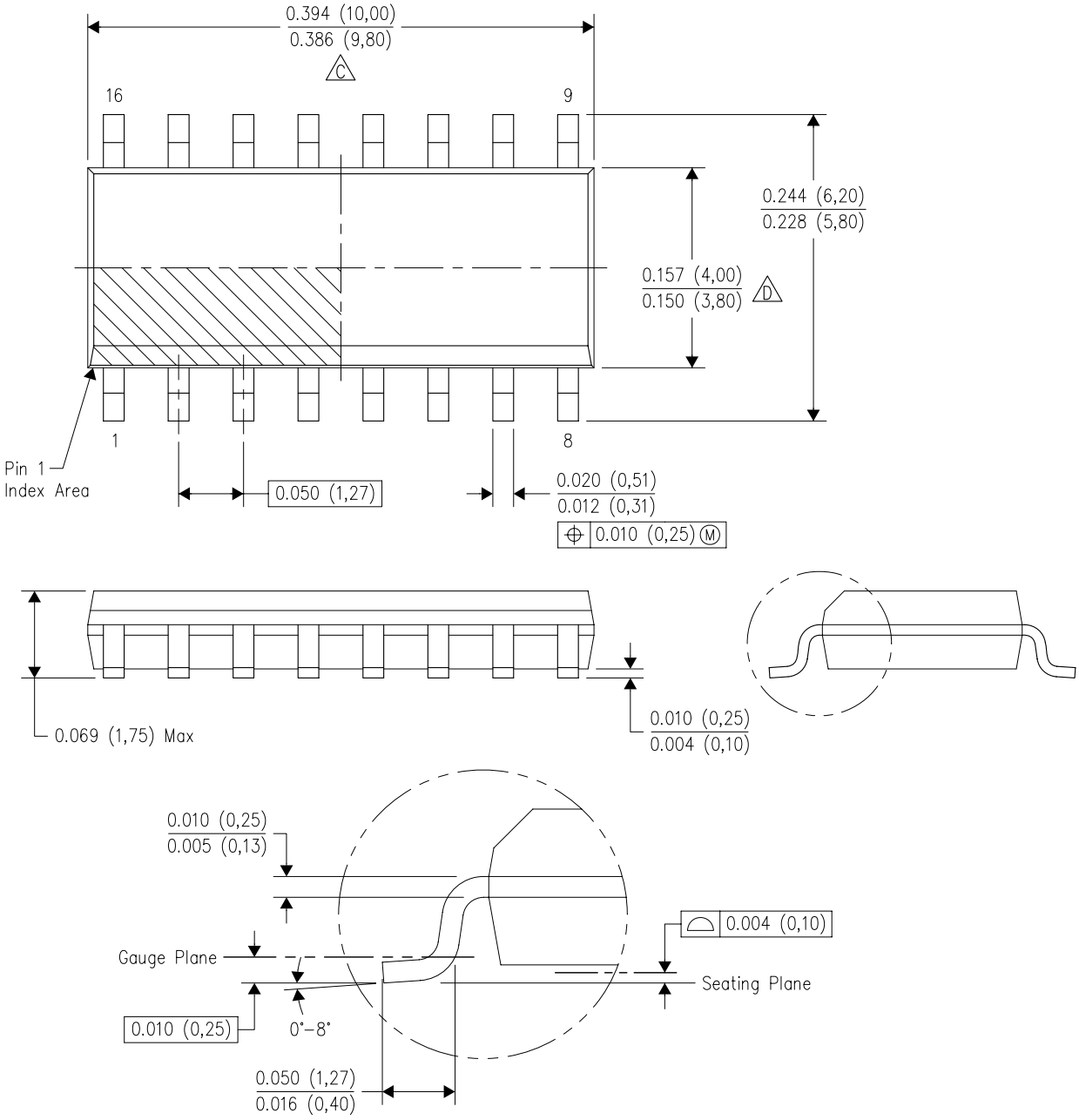
NFG0016E



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N16E (Rev G)

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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