LM2685 Dual Output Regulated Switched Capacitor Voltage Converter

Check for Samples: LM2685

FEATURES

- **+5V Regulated Output**
- **Inverts V_{05}(+5V) to V_{NEG}(−5V)**
- **Doubles Input Supply Voltage**
- **TSSOP-14 Package**
- **80% Typical Conversion Efficiency at 25mA**
- **Input Voltage Range of 2.85V to 6.5V**
- **Independent Shutdown Control Pins**

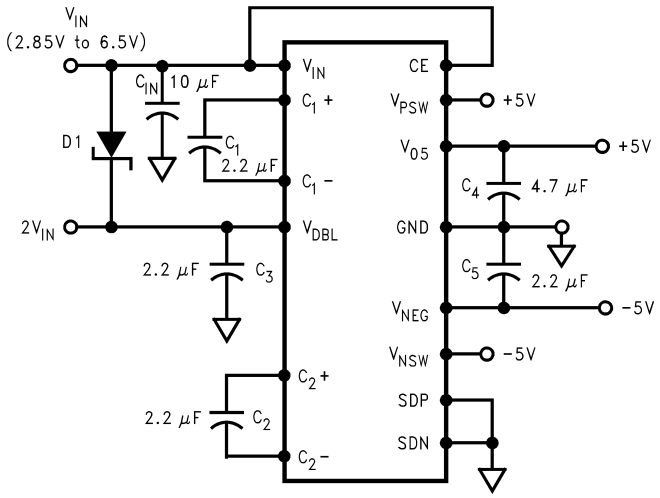
APPLICATIONS

- **Cellular Phones**
- **Pagers**
- **PDAs**
- **Handheld Instrumentation**
- **3.3V to 5V Voltage Conversion Applications**

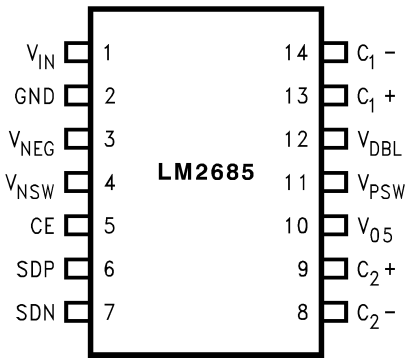
DESCRIPTION

The LM2685 CMOS charge-pump voltage converter operates as an input voltage doubler, +5V regulator and inverter for an input voltage in the range of +2.85V to +6.5V. Five low cost capacitors are used in this circuit to provide up to 50mA of output current at +5V (± 5%), and 15mA at −5V. The LM2685 operates at a 130 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 800µA (operating efficiency greater than 80% with most loads) and 6µA typical shutdown current, the LM2685 is ideal for use in battery powered systems. The device is in a small 14-pin TSSOP package.

Typical Application and Connection Diagram



14-Pin TSSOP



PIN DESCRIPTIONS

Pin No.	Name	Function
1	V_{IN}	Power supply input voltage.
2	GND	Power supply ground.
3	V_{NEG}	Negative output voltage created by inverting V_{05}.
4	V_{NSW}	V_{NEG} output connected through a series switch, NSW.
5	CE	Chip enable input. This pin is high for normal operation and low for shutdown. (See Shutdown and Load Disconnect section in the Detailed Device Description division.)
6	SDP	Positive side shutdown input. This pin is low for normal operation and high for positive side shutdown and V_{PSW} load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division.)
7	SDN	Negative side shutdown input. This pin is low for normal operation and high for negative side shutdown and V_{NSW} load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division.)
8	C_2^-	The negative terminal of inverting charge-pump capacitor, C2.
9	C_2^+	The positive terminal of inverting charge-pump capacitor, C2.
10	V_{05}	Regulated +5V output.
11	V_{PSW}	V_{05} output connected through a series switch, PSW.
12	V_{DBL}	Voltage Doubler Output. (2.85V ≤ V_{IN} ≤ 5.4V. See Voltage Doubler section).
13	C_1^+	The positive terminal of doubling charge-pump capacitor, C1.
14	C_1^-	The negative terminal of doubling charge-pump capacitor, C1.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{IN} to GND or GND to V_{NEG})	6.8V
SDN, SDP, CE	(GND − 0.3V) to (V_{IN} + 0.3V)
V_{05} Continuous Output Current	80mA
V_{05} Short-Circuit Duration to GND (3)	Indefinite
Continuous Power Dissipation (T_A = 25°C) (4)	600mW
T_{JMAX} (4)	150°C
θ_{JA} (4)	140°C/W
Operating Ambient Temp. Range	−40°C to 85°C
Operating Junction Temp. Range	−40°C to 125°C
Storage Temp. Range	−65°C to 150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD Rating (5)	2kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(3) V_{05} may be shorted to GND without damage. However, shorting V_{NEG} to V_{05} may damage the device and must be avoided. Also, for temperature above 85°C, V_{05} must not be shorted to GND or device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} — T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the specified package.
(5) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

ELECTRICAL CHARACTERISTICS

Limits with standard typeface apply for T_J = 25°C, and limits in **boldface type** apply over the full temperature range. Unless otherwise specified V_{IN} = 3.6V, $C_1 = C_2 = C_3 = C_5$ = 2.2µF. C_4 = 4.7µF (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V^+	Supply Voltage		**2.85**		**6.5**	V
I_Q	Supply Current	No Load		800	**1600**	µA
		No Load, V_{IN} = 6.5V		300	**600**	
I_{SD}	Shutdown Supply Current	V_{IN} = 6.5V		6	30	µA
V_{SD}	Shutdown Pin Input Voltage for CE, SDP, SDN	Logic Input High @ 6.5V	**2.4**			V
		Logic Input Low @ 6.5V			**0.8**	
I_L (+5V)	Output Current at V_{05}	2.85V < V_{IN} < 6.5V			**50**	mA
R_O (−5V)	Output Resistance at V_{NEG}	I_L = 15mA (2)		20	**40**	Ω
F_{SW}	Switch Frequency		**85**	130	**180**	kHz
P_{EFF}	Average Power Efficiency at V_{05}	2.85V ≤ V_{IN} ≤ 6.5V I_L = 25mA to GND		82		%
V_{05}	Output Regulation	1mA < I_L < 50mA, V_{IN} = 6.5V (3)	4.848	5.05	5.252	V
		1mA < I_L < 50mA, V_{IN} = 6.5V (3)	**4.797**	5.05	**5.303**	
G_{LINE}	Line Regulation	2.85V < V_{IN} < 3.6V		0.25		%/V
		3.6V < V_{IN} < 6.5V		0.05		
G_{LOAD}	Load Regulation	1mA < I_L < 50mA, V_{IN} = 6.5V		0.3	1.0	%
R_{SW}	Series Switch Resistance V_{NEG} to V_{NSW}	V_{IN} > 2.85V		1.5		Ω
	V_{05} to V_{PSW}			5.0		

(1) In the typical operating circuit, capacitors C_1 and C_2 are 2.2µF, 0.3Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.
(2) Specified output resistance includes internal switch resistance and ESR of capacitors. See the Detailed Device Description section.
(3) The 50 mA maximum current assumes no current is drawn from V_{DBL} pin. See Voltage Doubler section in the Detailed Device Description.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, T_A = 25°C, V_{IN} = 3.6V.

Supply Current vs Input Voltage

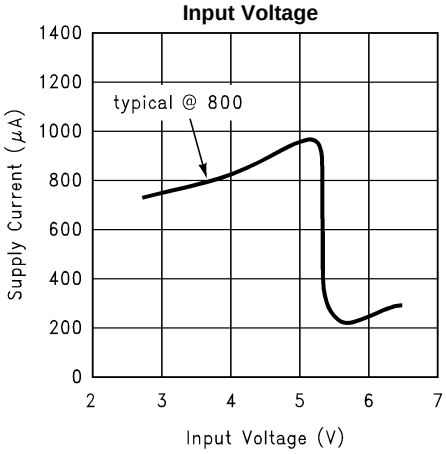


Figure 1.

Supply Current vs Temperature

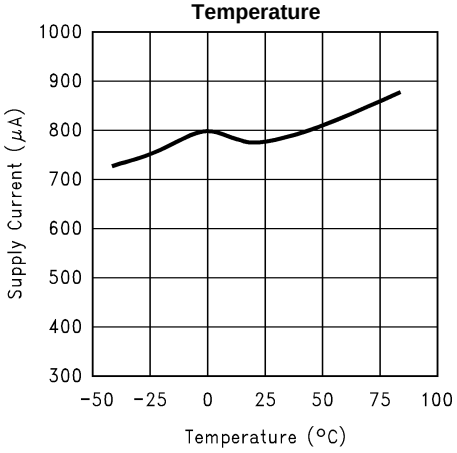


Figure 2.

Efficiency vs Load Current

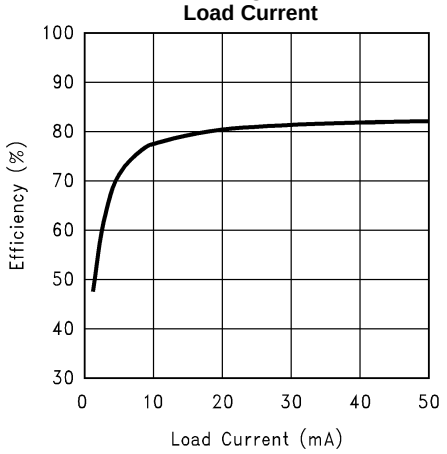


Figure 3.

Output Voltage (V_{05}) vs. Load Current

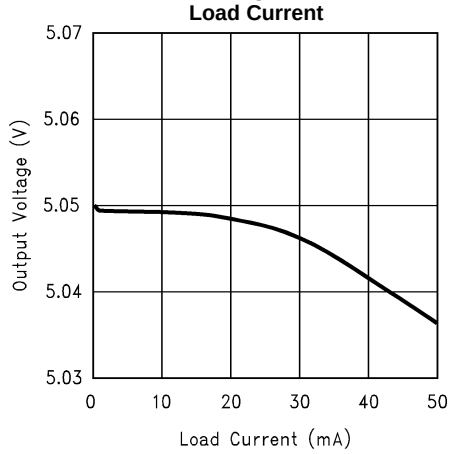


Figure 4.

V_{05} Voltage vs. Input Voltage

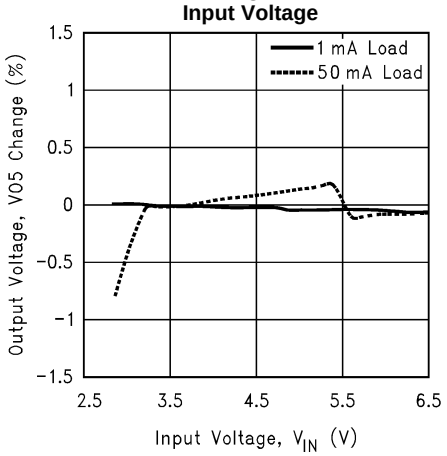


Figure 5.

Output Resistance (VNEG) vs. Temperature

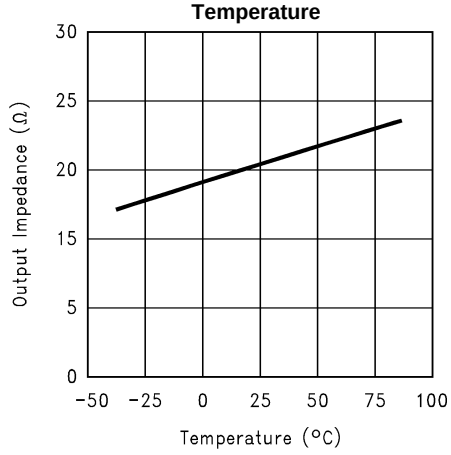


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V_{IN} = 3.6V.

Output Resistance (VDBL) vs. Input Voltage

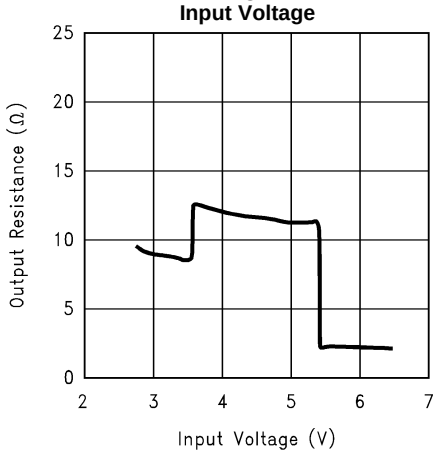


Figure 7.

Output Resistance (VDBL) vs. Temperature

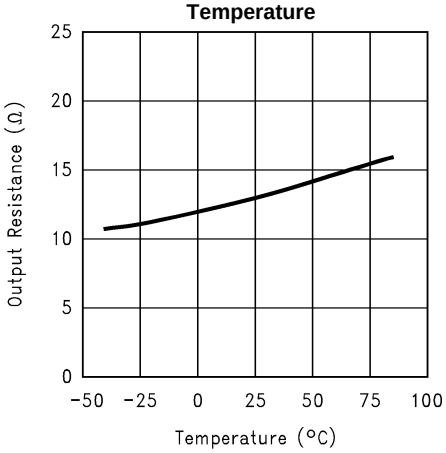


Figure 8.

Switch Frequency vs. Temperature

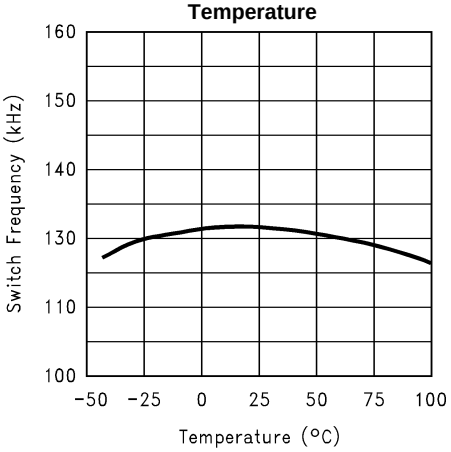
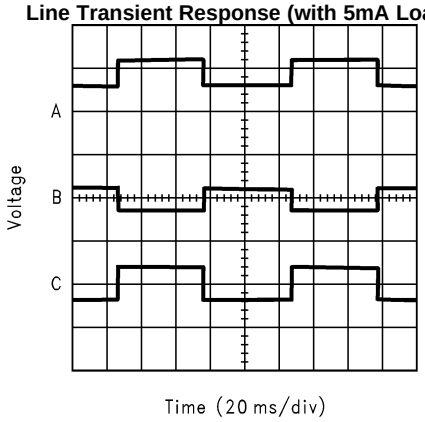


Figure 9.

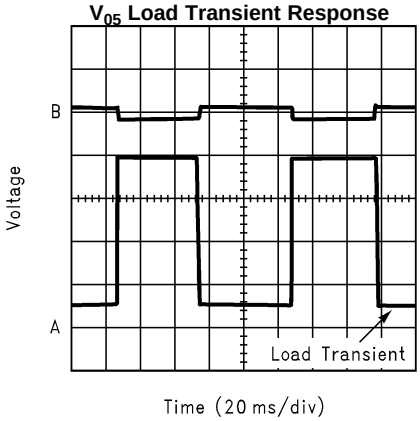
Line Transient Response (with 5mA Load)



A. INPUT VOLTAGE: V_{IN} = 3.2V to 6.0V, 5V/div
B. OUTPUT VOLTAGE: V_{PSW}: 100mV/div
C.OUTPUT VOLTAGE: V_{NSW}: 100mV/div

Figure 10.

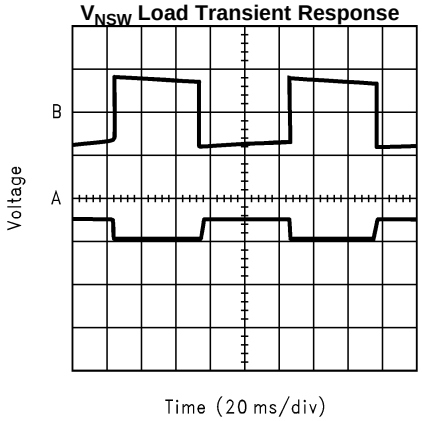
V_{05} Load Transient Response



A. LOAD CURRENT: I_{LOAD} = 5mA to 39.6mA, 10mA/div
B. OUTPUT VOLTAGE: V_{05}: 10mV/div

Figure 11.

V_{NSW} Load Transient Response



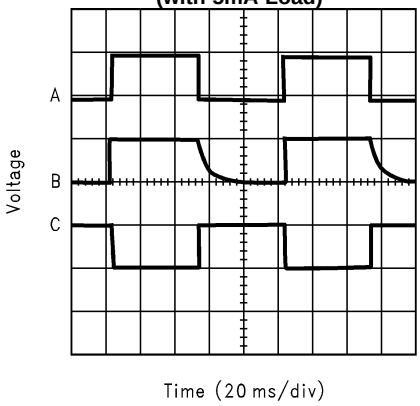
A. LOAD CURRENT: I_{LOAD} = 4.4mA to −9.4mA, 10mA/div
B. OUTPUT VOLTAGE: V_{NSW}: 50mV/div

Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V_{IN} = 3.6V.

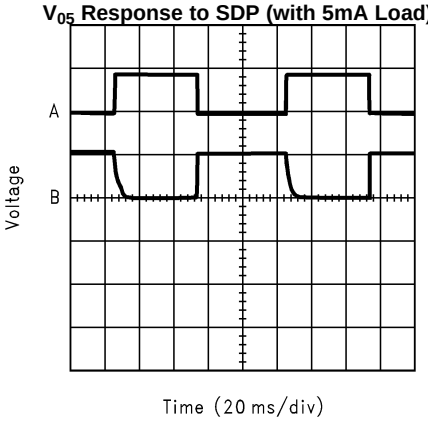
V_{PSW} and V_{NSW} Response to CE (with 5mA Load)



A. CE INPUT: 5V/div
B. OUTPUT VOLTAGE: V_{PSW}: 5V/div
C. OUTPUT VOLTAGE: V_{NSW}: 5V/div

Figure 13.

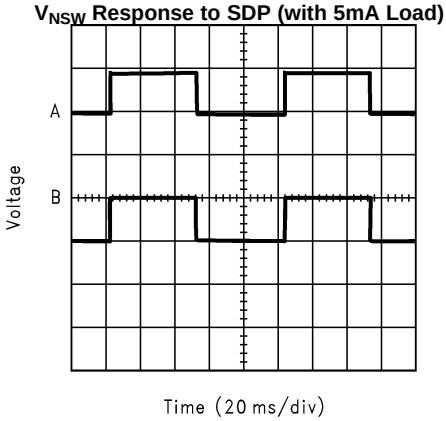
V_{05} Response to SDP (with 5mA Load)



A. SDP INPUT: 5V/div
B. OUTPUT VOLTAGE: 5V/div

Figure 14.

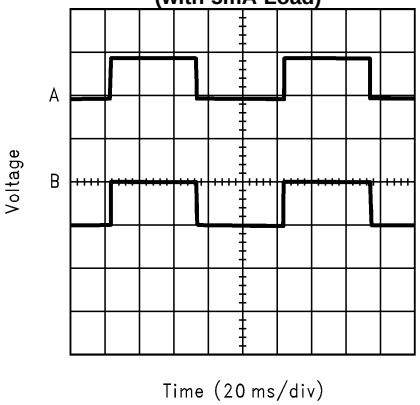
V_{NSW} Response to SDP (with 5mA Load)



A. SDP INPUT: 5V/div
B. OUTPUT VOLTAGE (V_{NSW}): 5V/div

Figure 15.

V_{NSW} Response to SDN (with 5mA Load)



A. SDN INPUT: 5V/div
B. OUTPUT VOLTAGE (V_{NSW}): 5V/div

Figure 16.

DETAILED DEVICE DESCRIPTION

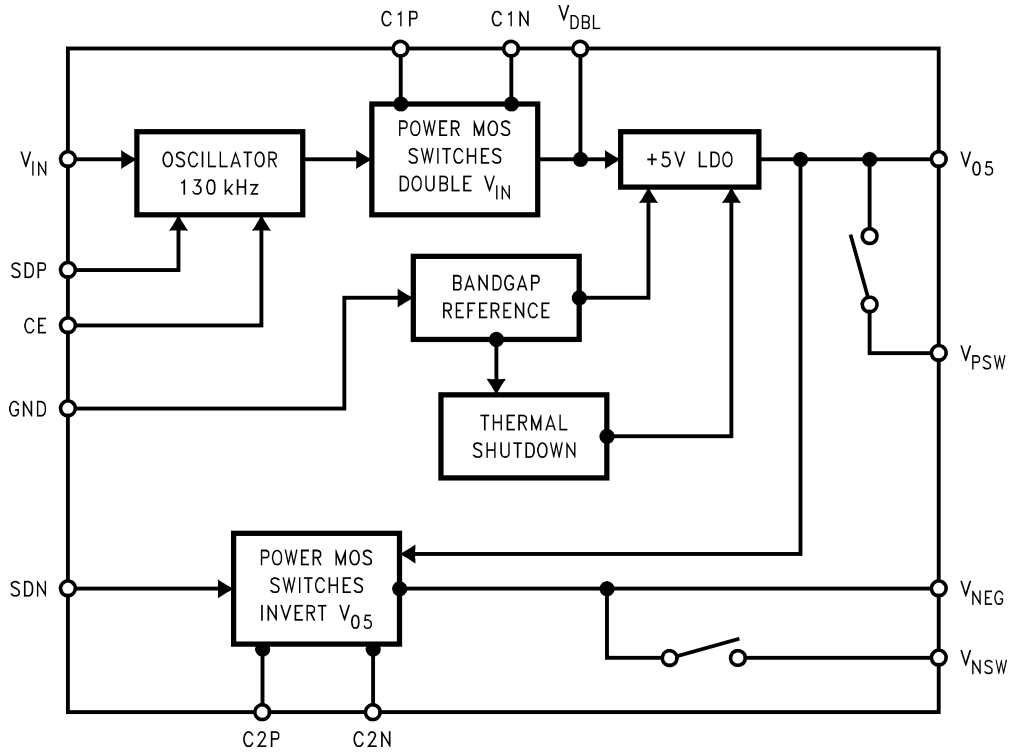


Figure 17. Functional Block Diagram

The LM2685 CMOS charge pump voltage converter operates as an input voltage doubler, +5V regulator and inverter for an input voltage in the range of +2.85V to +6.5V. It delivers maximum load currents of 50mA and 15mA for the regulated +5V and the inverted output voltages respectively, with an operating current of only 800µA. It also has a typical shutdown current of 6µA. All these performance qualities make the LM2685 an ideal device for battery powered systems.

The LM2685 has three main functional blocks: a voltage doubler, a low dropout (LDO) regulator, and a voltage inverter. Figure 17 shows the LM2685 functional block diagram.

VOLTAGE DOUBLER

The voltage doubler stage doubles the input voltage V_{IN}, within the range of +2.85V to +5.4V. For V_{IN} above 5.4V, the doubler shuts off and the input voltage is passed directly to V_{DBL} via an internal power switch.

The doubler contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Figure 18 illustrates the voltage conversion scheme. When S2 and S4 are closed, C1 charges to the supply voltage V_{IN}. During this time interval, switches S1 and S3 are open. In the next time interval, S2 and S4 are opened at the same time, S1 and S3 are closed, the sum of the input voltage V_{IN} and the voltage across C1 gives the $2V_{In}$ and the voltage across C2 gives the $2V_{IN}$ at V_{DBL} output. V_{DBL} supplies the LDO regulator. It is recommended not to load V_{DBL} when V_{05} has a load of 50mA. For proper operation, the sum of V_{DBL} and V_{05} loads must not be more than 50mA.

The Schottky diode D1 is only needed for start-up. The internal oscillator circuit uses the V_{DBL} and GND pins. The voltage across them must be larger than 1.8V to ensure the operation of the oscillator. During start-up, D1 is used to charge up the voltage at V_{DBL} pin to start the oscillator; it also protects the device from turning on its own parasitic diode and potentially latching up. The diode should have enough current carrying capability to change capacitor C3 at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning on. A Schottky diode like 1N5817 can be used for most applications. If the input ramp is less than 10V/ms, a smaller schottky diode like MBR0520LT1 can be used to reduce the circuit size.

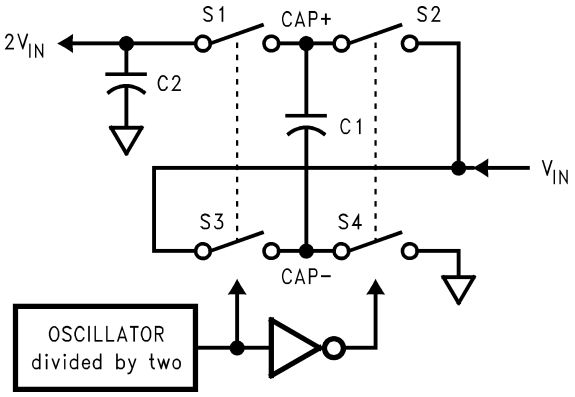


Figure 18. Voltage Doubler Principle

+5 LDO REGULATOR

V_{DBL} is the input to an LDO regulator that regulates it to a +5 output voltage at V_{05}. V_{PSW} is tied to V_{05} through a series switch PSW. The LDO output capacitor (4.7µF Tantalum) may be tied to either V_{05} or V_{PSW}.

INVERTER

From the V_{05} output, a −5V output is created at V_{NEG} by means of an inverting charge pump. This negative output is unregulated, meaning that it's output will droop as the load current at V_{NEG} increases. The inverter contains four large CMOS switches which are in a sequence to invert the input supply voltage. Figure 19 illustrates the voltage conversion scheme. When S1 and S3 are closed, C1 charges to the supply voltage V_{05}. During this time interval, switches S2 and S4 are open. In the second time interval, S1 and S3 are open;at the same time, S2 and S4 are closed, C1 is charging C2. After a number of cycles, the voltage cross C2 will be pumped to V_{05}. Since the anode of C2 is connected to ground, the output at the cathode of C2 equals $-(V_{05})$ when there is no load current. The output voltage drop when a load is added is determined by the parasitic resistance (R_{ds}(on) of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors.

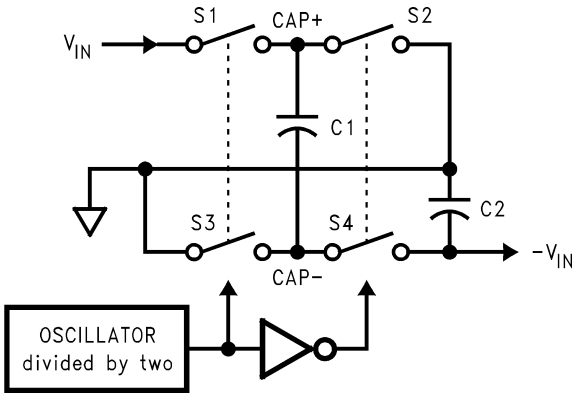


Figure 19. Voltage Inverter Principle

SHUTDOWN AND LOAD DISCONNECT

In addition to the nominal charge pump and regulator functions, the LM2685 features shutdown and load disconnect circuitry. CE (chip enable) and SDP (shutdown positive) perform the same task with opposite input polarities. When CE is low or SDP is high, all circuit blocks are disabled and V_{05} falls to ground potential. This is the same result as when the die temperature exceeds 150°C (typical), and the device's internal thermal shutdown is triggered.

Forcing SDN (shutdown negative) high disables only the inverting charge pump. The doubling charge pump and the LDO regulator continue to operate, so the V_{05} and the V_{PSW} remain at 5V.

The LM2685 incorporates two low impedance switches tied to the V_{05} and V_{NEG} outputs, because some special applications require load disconnect and this is achievable via the switches. Switch PSW connects V_{05} to V_{PSW}, and switch NSW connects V_{NEG} to V_{NSW}. In normal operation, these switches are closed, allowing 5V loads to be tied to either V_{05} or V_{PSW} and −5V loads to be tied to either V_{NEG} or V_{NSW}. Driving SDN high opens switch NSW only, while forcing CE low or SDP high, opens both the PSW and NSW.

APPLICATION INFORMATION

CAPACITOR SELECTION

The output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors.

VOLTAGE DOUBLER EXTERNAL CAPACITORS

The selection of capacitors are based on the specifications of the dropout voltage (which equals I_{OUT} R_{OUT}), the output voltage ripple, and the converter efficiency.

$$R_{OUT} = 2 R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4 ESR_{C_1} + ESR_{C_3}$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches as shown in Figure 18

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the capacitor C3.

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C_3}$$

High capacitance (2.2µF to higher), low ESR capacitors can reduce the output resistance and the voltage ripple.

$$\text{Power efficiency of} = \frac{P_{OUT}}{P_{IN}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{OUT} + I_Q (V+)}$$

where

- $I_Q(V+)$ is the quiescent power loss of the IC device
- $I^2_L R$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs

Low ESR capacitors (table to be referenced) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

+5 LDO REGULATOR EXTERNAL CAPACITORS

The voltage doubler output capacitor, C3, serves as the input capacitor of the +5 LDO regulator. The output capacitor C4, must meet the requirement for minimum amount of capacitance and appropriate ESR (Equivalent Serving Resistance) for proper operation. The ESR value must remain within the regions of stability as shown in Figure 20, Figure 21 and Figure 22 to ensure output's stability. A minimum capacitance of 1µF is required at the output. This can be increased without limit, but a 4.7µF tantalum capacitor is recommended for loads ranging upto the maximum specification. With lighter loads of less or equal to 10mA, ceramic capacitor of at least 1µF and ESR in the milliohms can be used. This has to be connected to V_{PSW} pin instead of the V_{05} pin.

Any output capacitor used should have a good tolerance over temperature for capacitance and ESR values. The larger the capacitor, with ESR within the stable region, the better the stability and noise performance.

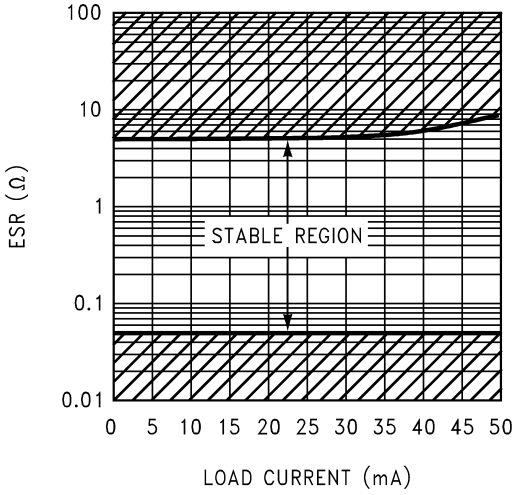


Figure 20. ESR Curve for C_{OUT} = 2.2µF

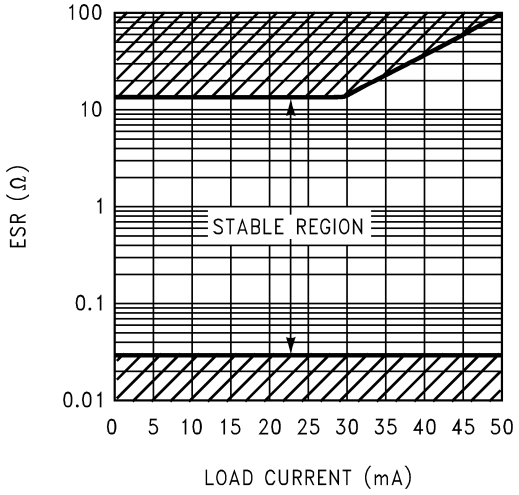


Figure 21. ESR Curve for C_{OUT} = 4.7µF

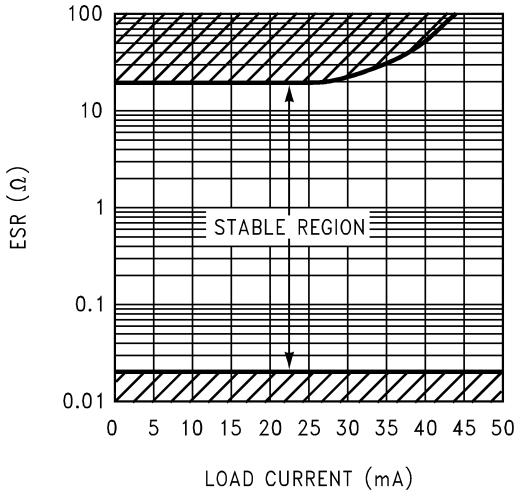


Figure 22. ESR Curve for C_{OUT} =10µF

INVERTER EXTERNAL CAPACITORS

As discussed in the +5 LDO Regulator External Capacitors section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. A minimum of 1µF capacitor with good tolerance over temperature for capacitance and ESR values. The capacitance value can be increased without limit while still maintain high low ESR value. 2.2µF capacitors are recommended for the two external capacitors, C_2 and C_5 of the inverter.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265