LM2686 Regulated Switched Capacitor Voltage Converter

Check for Samples: LM2686

FEATURES

- **+5V Regulated Output**
- **Doubles Input Supply Voltage**
- **TSSOP 14 Package**
- **80% Typical Conversion Efficiency at 25mA**
- **Input Voltage Range of 2.85V to 6.5V**
- **Independent Shutdown Control Pins**

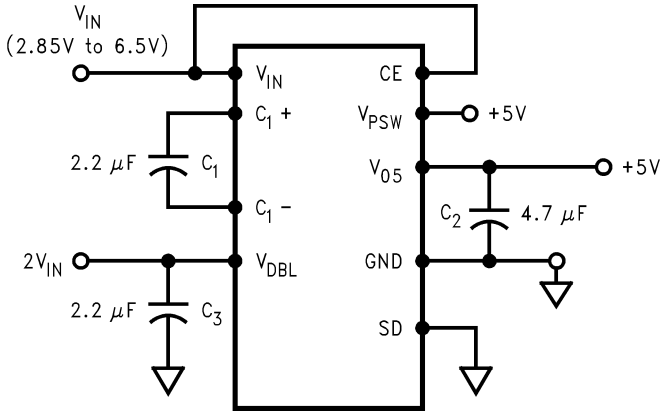
APPLICATIONS

- **Cellular Phones**
- **Pagers**
- **PDAs**
- **Handheld Instrumentation**
- **3.3V to 5V Voltage Conversion Applications**

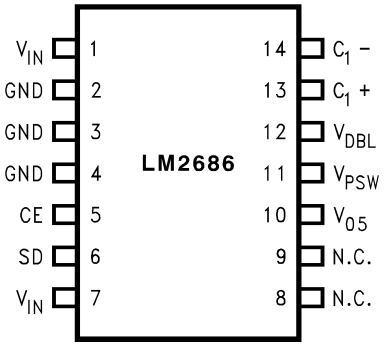
DESCRIPTION

The LM2686 CMOS charge-pump voltage converter operates as an input voltage doubler and a +5V regulator for an input voltage in the range of +2.85V to +6.5V. Three low cost capacitors are used in this circuit to provide up to 50mA of output current at +5.0V (± 5%). The LM2686 operates at a 130 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 450µA (operating efficiency greater than 80% with most loads) and 6.0µA typical shutdown current, the LM2686 is ideal for use in battery powered systems. The device is in a small 14-pin TSSOP package.

Typical Application and Connection Diagram



14-Pin TSSOP



PIN DESCRIPTIONS

Pin No.	Name	Function
1	V_{IN}(1)	Power supply input voltage.
2	GND(2)	Power supply ground.
3	GND(2)	Power supply ground.
4	GND(2)	Power supply ground.
5	CE	Chip enable input. This pin is high for normal operation and low for shutdown and V_{PSW} load disconnect.
6	SD	Shutdown input. This pin is low for normal operation and high for shutdown and V_{PSW} load disconnect.
7	V_{IN}(1)	Power supply input voltage.
8	NC	No connection.
9	NC	No connection.
10	V_{05}	Regulated +5V output.
11	V_{PSW}	V_{05} output connected through a series switch, PSW.
12	V_{DBL}	Output of doubled input voltage.
13	C_1^+	The positive terminal of doubling charge-pump capacitor, C1.
14	C_1^-	The negative terminal of doubling charge-pump capacitor, C1.

(1) All V_{IN} pins, pin 1 and pin 7 must be tied together for proper operation.
(2) All ground pins, pin 2, pin 3 and pin 4 must be tied together for proper operation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{IN} to GND)	6.8V
SD, CE	(GND − 0.3V) to (V_{In} + 0.3V)
V_{05} Continuous Output Current	80mA
V_{05} Short-Circuit Duration to GND (3)	Indefinite
Continuous Power Dissipation (T_A = 25°C) (4)	600mW
T_{JMAX} (4)	150°C
θ_{JA} (4)	140°C/W
Operating Ambient Temp. Range	−40°C to 85°C
Operating Junction Temperature Range	−40°C to 125°C
Storage Temp. Range	−65°C to 150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD Rating (5)	2kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.

(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**

(3) V_{05} may be shorted to GND without damage. For temperature above 85°C, V_{05} must not be shorted to GND or device may be damaged.

(4) The maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} — T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, $T_A$is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the specified package.

(5) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

ELECTRICAL CHARACTERISTICS

Limits with standard typeface apply for T_J = 25°C, and limits in **boldface type** apply over the full temperature range. Unless otherwise specified V_{IN} = 3.6V, $C_1 = C_3$ = 2.2µF. C_2 = 4.7µF. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V^+	Supply Voltage		**2.85**		**6.5**	V
I_Q	Supply Current	No Load		450	**950**	µA
I_{SD}	Shutdown Supply Current	V_{IN} = 6.5V		6	30	µA
V_{SD}	Shutdown Pin Input Voltage for CE, SD	Logic Input High @ 6.5V	**2.4**			V
		Logic Input Low @ 6.5V			**0.8**	
I_L (+5V)	Output Current at V_{05}	2.85V < V_{IN} < 6.5V			**50**	mA
F_{SW}	Switch Frequency		**85**	130	**180**	kHz
P_{EFF}	Average Power Efficiency at V_{05}	2.85V < V_{IN} < 6.5V I_L = 25mA to GND		82		%
V_{05}	Output Regulation	1mA < I_L < 50mA, V_{IN} = 6.5V (2)	4.848	5.05	5.252	V
		1mA < I_L < 50mA, V_{IN} = 6.5V (2)	**4.797**	5.05	**5.303**	V
G_{LINE}	Line Regulation	2.85V < V_{IN} < 3.6V		0.25		%/V
		3.6V < V_{IN} < 6.5V		0.05		
G_{LOAD}	Load Regulation	1mA < I_L < 50mA, V_{IN} = 6.5V		0.3	1.0	%
R_{SW}	Series Switch Resistance from V_{05} to V_{PSW}	V_{IN} > 2.85V		5.0		Ω

(1) In the typical operating circuit, capacitors C_1 and C_3 are 2.2µF, 0.3Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.

(2) The 50mA maximum current assumes no current is drawn from V_{DBL} pin. See Voltage Doubler section in the Detailed Device Description.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, T_A = 25°C, V_{IN} = 3.6V.

Supply Current vs Input Voltage

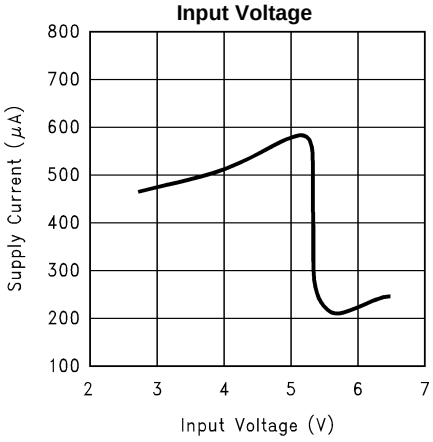


Figure 1.

Supply Current vs Temperature

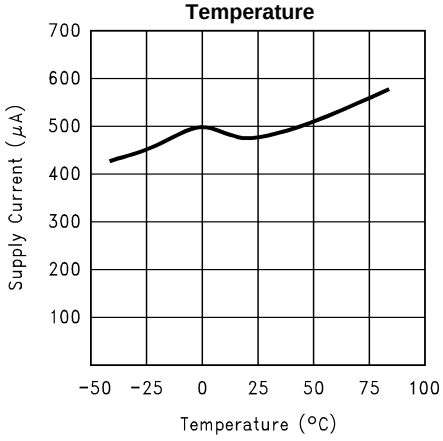


Figure 2.

Efficiency vs Load Current (V_{IN} = 3.0V)

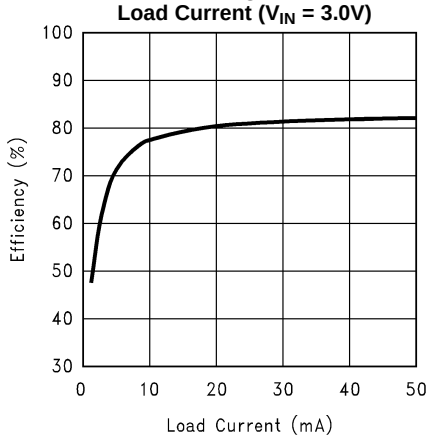


Figure 3.

Output Resistance (VDBL) vs. Temperature (V_{IN} = 3.6V)

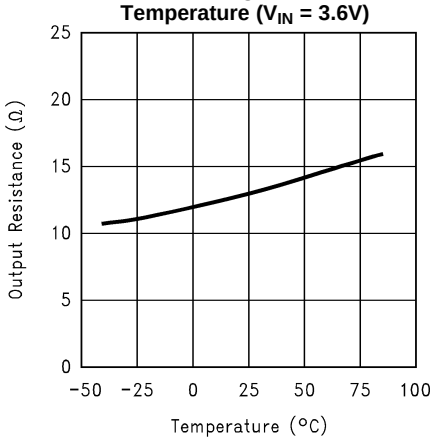


Figure 4.

Switch Frequency vs. Temperature (V_{IN} = 3.6V)

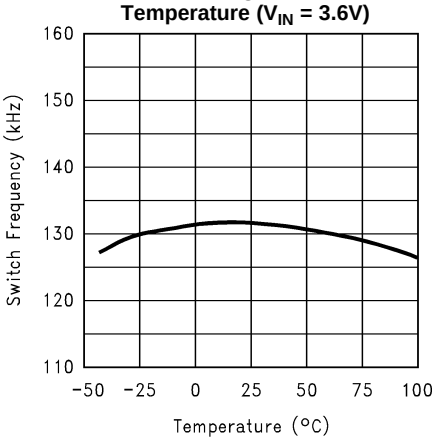
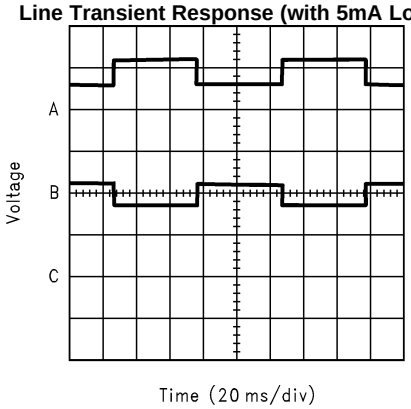


Figure 5.

Line Transient Response (with 5mA Load)

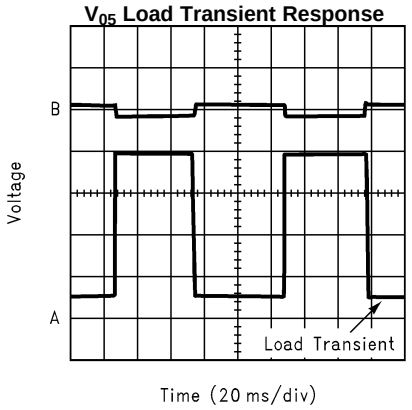


A: INPUT VOLTAGE: V_{IN} = 3.2V to 6.0V, 5V/div
B: OUTPUT VOLTAGE: V_{PSW}: 100mV/div

Figure 6.

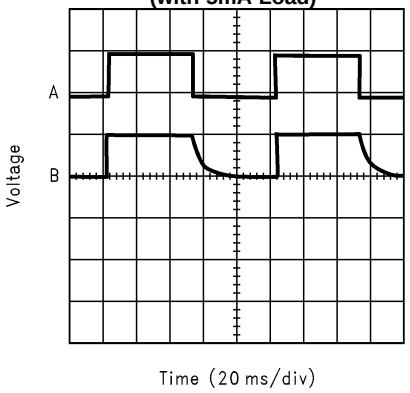
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V_{IN} = 3.6V.



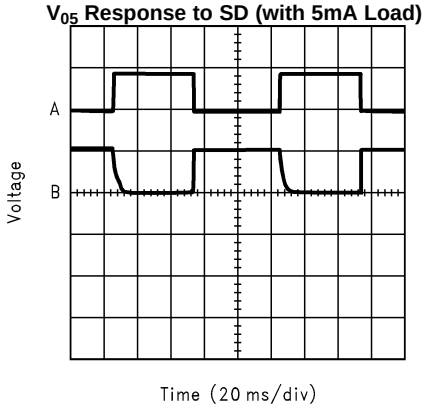
A: LOAD CURRENT: I_{LOAD} = 5mA to 39.6mA, 10mA/div
B: OUTPUT VOLTAGE: V_{05}: 10mV/div

Figure 7.



A: CE INPUT: 5V/div
B: OUTPUT VOLTAGE: V_{PSW}: 5V/div

Figure 8.



A: SD INPUT: 5V/div
B: OUTPUT VOLTAGE: 5V/div

Figure 9.

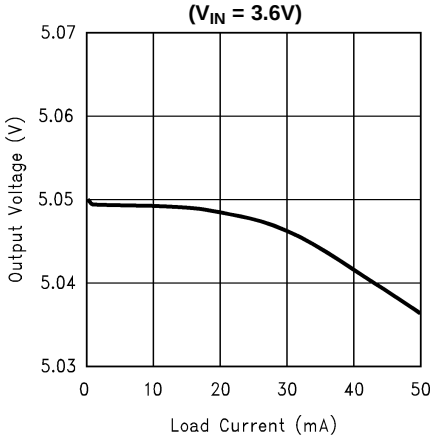


Figure 10.

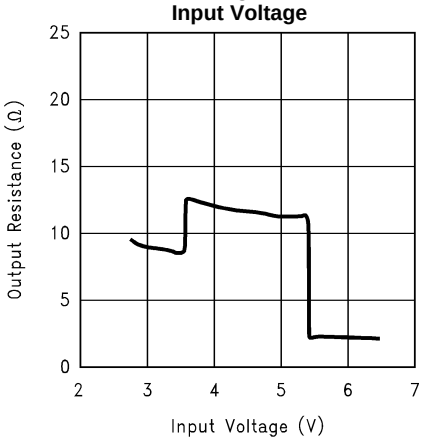


Figure 11.

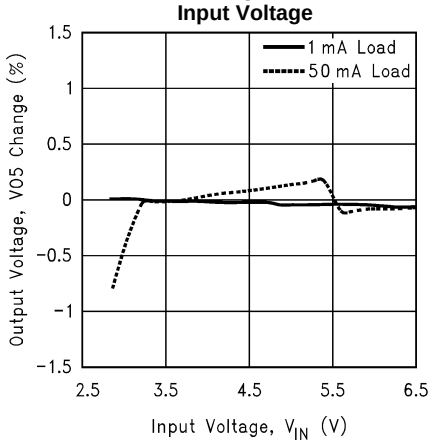


Figure 12.

DETAILED DEVICE DESCRIPTION

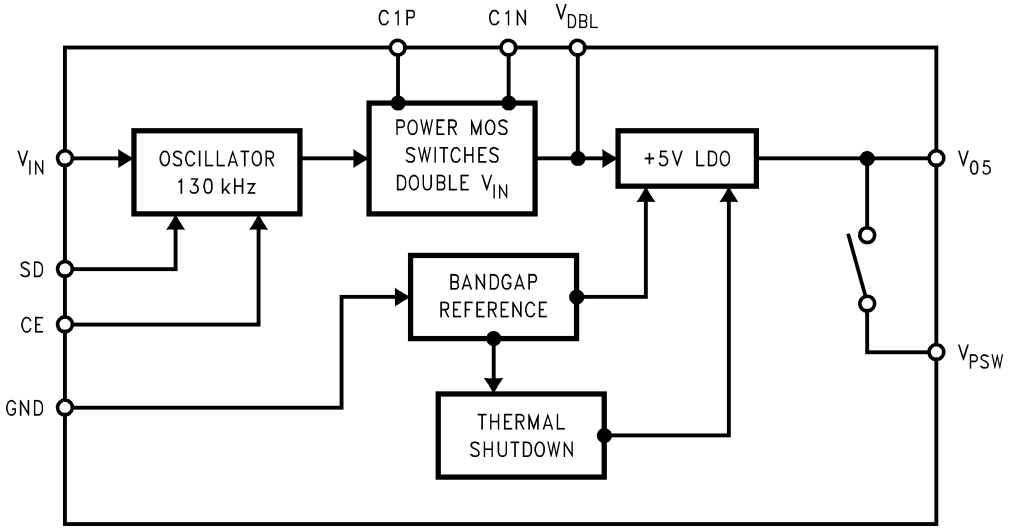


Figure 13. Functional Block Diagram

The LM2686 CMOS charge pump voltage converter operates as an input voltage doubler, +5V regulator for an input voltage in the range of +2.85V to +6.5V. It delivers maximum load currents of 50mA for the regulated +5V, with an operating current of only 450µA. It also has a typical shutdown current of 6µA. All these performance qualities make the LM2686 an ideal device for battery powered systems.

The LM2686 has two main functional blocks: a voltage doubler and a low dropout (LDO) regulator. Figure 13 shows the LM2686 functional block diagram.

VOLTAGE DOUBLER

The voltage doubler ties directly to V_{IN} and doubles the input voltage in the range from +2.85V to +5.4V up to 5.7V to 10.8V at the V_{DBL} pin. For V_{IN} above 5.4V, the doubler shuts off and the input voltage is passed directly to VDBL via an internal power switch.

The doubler contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Figure 14 illustrates the voltage conversion scheme. When S2 and S4 are closed, C1 charges to the supply voltage V_{IN}. During this time interval, switches S1 and S3 are open. In the next time interval, S2 and S4 are opened at the same time, S1 and S3 are closed, the sum of the input voltage V_{IN} and the voltage across C1 gives the $2V_{In}$ and the voltage across C2 gives the $2V_{IN}$ at V_{DBL} output. V_{DBL} supplies the LDO regulator. It is recommended not to load V_{DBL} when V_{05} has a load of 50mA. For proper operation, the sum of V_{DBL} and V_{05} loads must not be more than 50mA.

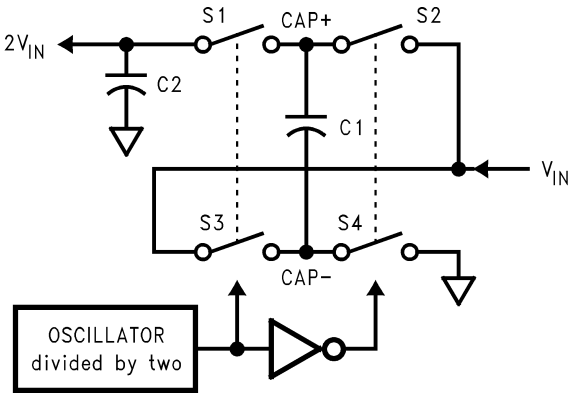


Figure 14. Voltage Doubler Principle

+5 LDO REGULATOR

V_{DBL} is the input to an LDO regulator that regulates it to a +5 output voltage at V_{05}. V_{PSW} is tied to V_{05} through a series switch PSW. The LDO output capacitor (4.7µF Tantalum) may be connected to either V_{05} or V_{PSW}.

SHUTDOWN AND LOAD DISCONNECT

In addition to the nominal charge pump and regulator functions, the LM2686 features shutdown and load disconnect circuitry. CE (chip enable) and SD (shutdown positive) perform the same task with opposite input polarities. When CE is low or SD is high, all circuit blocks are disabled and V_{05} falls to ground potential. This is the same result as when the die temperature exceeds 150°C, and the device's internal thermal shutdown is triggered.

The LM2686 incorporates a low impedance switch tied to the V_{05} output, because some special applications require load disconnect and this is achievable via the switch. Switch PSW connects V_{05} to V_{PSW}. In normal operation, this switch is closed, allowing 5V loads to be tied to either V_{05} or V_{PSW}. Forcing CE low or SD high opens the PSW.

APPLICATION INFORMATION

CAPACITOR SELECTION

The output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors.

VOLTAGE DOUBLER EXTERNAL CAPACITORS

The selection of capacitors are based on the specifications of the dropout voltage (which equals I_{OUT} R_{OUT}), the output voltage ripple, and the converter efficiency.

$$R_{OUT} = 2 R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4 ESR_{C_1} + ESR_{C_3}$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches as shown in Figure 14

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the capacitor C3.

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C_3}$$

High capacitance (2.2µF to higher), low ESR capacitors can reduce the output resistance and the voltage ripple.

$$\text{Power efficiency of} = \frac{P_{OUT}}{P_{IN}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{OUT} + I_Q (V+)} \quad (1)$$

where

- $I_Q(V+)$ is the quiescent power loss of the IC device
- $I^2_L R$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs

Low ESR capacitors (table to be referenced) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

+5 LDO REGULATOR EXTERNAL CAPACITORS

The voltage doubler output capacitor, C3, serves as the input capacitor of the 5 LDO regulator. The output capacitor C4, must meet the requirement for minimum amount of capacitance and appropriate ESR (Equivalent Serving Resistance) for proper operations. The ESR value must remain within the regions of stability as shown in Figure 15, Figure 16 and Figure 17 to ensure output's stability. A minimum capacitance of 1µF is required at the output. This can be increased without limit, but a 4.7µF tantalum capacitor is recommended for loads ranging upto the maximum specification. In lighter loads of less or equal to 10mA, ceramic capacitor of at least 1µF and ESR in the milliohms can be used. This has to be connected to V_{PSW} pin instead of the V_{05} pin.

Any output capacitor used should have a good tolerance over temperature for capacitance and ESR values. The larger the capacitor, with ESR within the stable region, the better the stability and noise performance.

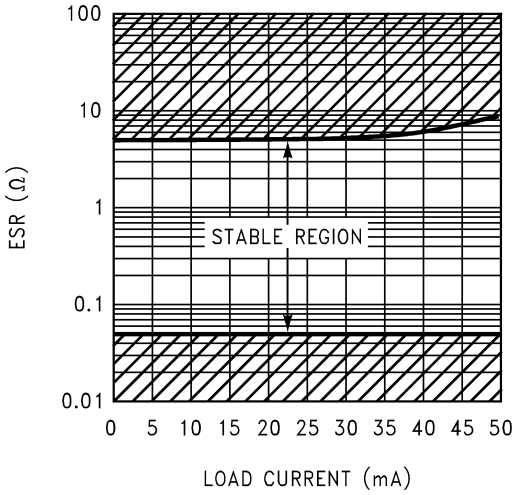


Figure 15. ESR Curve for C_{OUT} = 2.2µF

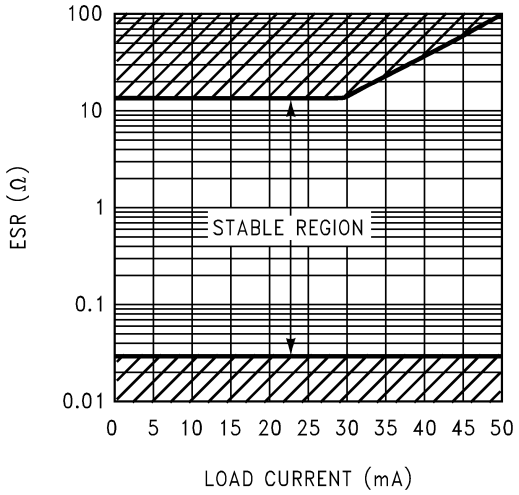


Figure 16. ESR Curve for C_{OUT} = 4.7µF

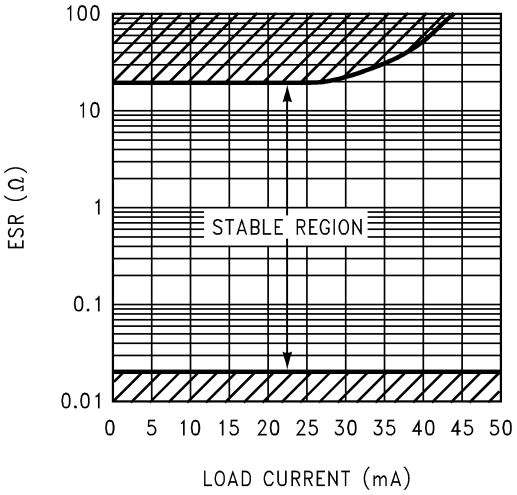


Figure 17. ESR Curve for C_{OUT} =10µF

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