LM2720 5-Bit Programmable, High Frequency Multi-phase PWM Controller

Check for Samples: LM2720

FEATURES

- **Ultra Fast Load Transient Response**
- **Enables All Surface-Mount-Design**
- **Selectable 2, 3, 4 Phase Operation**
- **Clock Frequency from 40 kHz to 10 MHz**
- **Precision Load Current Sharing**
- **5-bit Programmable from 3.5V to 1.3V**
- **VID Code Compatible to VRM 8.X Specification**
- **Output Voltage is 2.0V for VID Code 11111**
- **Selectable Internal or External Clock**
- **Digital 16-Step Soft Start**
- **Input Under-Voltage Lock-Out, Over-Current Protection**
- **Open-Drain Power Good Signal Output**

APPLICATIONS

- **Servers and Workstations**
- **High Current, Ultra-Fast Transient Microprocessors**

DESCRIPTION

The LM2720 provides an attractive solution for power supplies of high power microprocessors exhibiting ultra fast load transients. Compared to a conventional single-phase supply, an LM2720 based multi-phase supply distributes the thermal and electrical loading among components in multiple phases and greatly reduces the corresponding stress in each component. The LM2720 can be programmed to control either a 3-phase converter or a 4-phase converter. Phase shift among the phases is 120° in the case of three phase and 90° with four-phase. Because the power channels are out of phase, there can be significant ripple cancellation for both the input and output current, resulting in reduced input and output capacitor size. Due to the nominal operating frequency of 2 MHz per phase, the size of the output inductors can be greatly reduced which results in a much faster load transient response and a dramatically shrunk output capacitor bank. Microprocessor power supplies with all surface mount components can be easily built.

The internal high speed transconductance amplifier specifies good dynamic performance.

The internal master clock frequency of up to 8 MHz is set by an external reference resistor. An external clock of 10 MHz can also be used to drive the chip to achieve frequency control and multi-chip operation.

The LM2720 also provides input under-voltage lock-out with hysteresis, input over-current protection and output voltage power good detection.

Pin Configuration

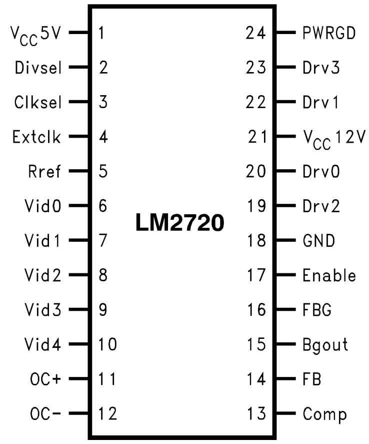


Figure 1. 24-Pin Plastic SOIC (Top View)
See Package Number DW0024B

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V_{CC}5V	7V
PWRGD	(V_{CC} 5V + 0.2V)
V_{CC}12V	20V
Junction Temperature	125°C
Power Dissipation(3)	1.6W
Storage Temperature	−65°C to +150°C
ESD Susceptibility(4)	2 kV
Soldering Time, Temperature	10 sec., 300°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** do not imply specified performance limits.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$. The junction-to-ambient thermal resistance, θ_{JA}, for LM2720 is 78°C/W. For a T_{JMAX} of 150°C and T_A of 25°C, the maximum allowable power dissipation is 1.6W.
(4) ESD ratings is based on the human body model, 100pF discharged through 1.5kΩ.

Operating Ratings(1)

V_{CC} 5V	4.5V to 5.5V
V_{CC} 12V	10V to 18V
Junction Temperature Range	0°C to 70°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** do not imply specified performance limits.

Electrical Characteristics

V_{CC}5V = 5V, V_{CC}12V = 12V unless otherwise specified. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DACOUT}	5-bit DAC Output Voltage	See (1)	***N***−1.5%	***N***	***N***+1.5%	V
I_{CC}12V	Quiescent V_{CC}12V Current	Enable = 5V, VID = 00001, DRV Outputs Floating		1	**2**	mA
I_{CC}5V	Operating V_{CC}5V Current	V_{OUT} = 2.00V		4.3	**8**	mA
V_{REF}	Rref Pin Voltage			1.225		V
V_{INL}	Vid0:4, Clksel, Divsel, and Enable Pins Logic Threshold	Logic Low (2)		1.8	1.5	V
V_{INH}		Logic High (3)	3.5	2.8		V
I_{INL}	Vid0:4 and Enable Pins Internal Pullup Current	The Corresponding Pin = 0V	60	100	140	µA
	Clksel, Divsel Pins Internal Pullup Current		−10	0	10	
	Gate Driver Resistance When Sinking Current	I_{SINK} = 50 µA, V_{CC}12V = 14V		12		Ω
V_{DRV}	DRV0:3 Output Voltage	I_{DRV} = 10 mA, V_{CC}12V = 14V	V_{CC}12V − 1.5V	V_{CC}12V −1.0V		V
t_{fall}	DRV0:3 Fall Time	See (4)		7		ns
I_{SRC}	DRV0:3 Source Current	DRV0:3 = 0V, V_{CC}12V = 14V	40	60		mA
I_{SINK}	DRV0:3 Sink Current	DRV0:3 = 5V, V_{CC}12V = 14V	90	160	250	mA
VB_{gOUT}	B_{gOUT} Voltage	Current Limit Not Activated		4		V
		Current Limit Activated		0		
IB_{gOUT}	B_{gOUT} Sink Current	B_{gOUT} = 1V	1.0	2.4	5	mA
I_{FB}	FB Pin Bias Current	FB = 2V		30		nA
F_{OSC}	Oscillator Frequency	8.02kΩ from Rref Pin to Ground	7.0	8.0	8.7	MHz
Δ_D	DRV0:3 Duty Cycle Match	Duty Cycle = 50%	−1		+1	%
Δ_{ph}	DRV0:3 Phase Accuracy	Duty Cycle = 50%, F_{clock} = 8 MHz	−1		+1	Deg
T_{off}	PWM Off time	Divide by 4		22		%
		Divide by 3		22		
V_{PWRGD}	Power Good Detection Window, ΔV_{OUT}	1.3V ≤ V_{OUT} ≤ 1.9V		±100		mV
	Hysteresis			50		
	Power Good Detection Window, ΔV_{OUT}	2V ≤ V_{OUT} ≤ 3.5V		±150		
	Hysteresis			50		
I_{PWRGD}	Power Good Sink Current	V_{PWRGD} = 0.4V	0.8	1		mA
V_{OCC_CM}	Over-current Comparator Common Mode Range		**3**		**12**	V
IB_OC+	OC+ Input Bias Current	V_{IN} = 5V, OC+ = 5V, OC− = 4V	100	145	200	µA
IB_OC−	OC− Input Bias Current	V_{IN} = 5V, OC+ = 6V, OC− = 5V	85	120	165	µA
V_{OS_OCC}	Over-current Comparator Input Offset Voltage	V_{IN} = 5V	2	16	42	mV
		V_{IN} = 12V		21		
D_{MAX}	Maximun Duty Cycle	FB = 0V		78		%
gm	Error Amplifier Transconductance			1.36		mmho
V_{ramp}	Ramp Signal Peak-to-Peak Amplitude			2		V

(1) The letter ***N*** stands for the typical output voltages appearing in ***italic boldface*** type in Table 1.
(2) **Max** value of logic low means any voltage below this value is specified to be taken as logic low whereas a voltage higher than this value is not specified to be taken as a logic low.
(3) **Min** value of logic high means any voltage above this value is specified to be taken as logic high whereas a voltage lower than this value is not specified to be taken as a logic high.
(4) When driving bipolar FET drivers in the typical application circuit.

Electrical Characteristics (continued)

V_{CC}5V = 5V, V_{CC}12V = 12V unless otherwise specified. Typicals and limits appearing in plain type apply for $T_A = T_J = +25°C$. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{comp}	COMP Pin Source Current		250	360	550	µA
I_{comp}	COMP Pin Sink Current		160	260	400	µA
V_{comp_hi}	COMP Pin High Clamp			2.9		V
V_{comp_lo}	COMP Pin Low Clamp			0.19		V
V_{POR}	Power On Reset Trip Point	Vcc5V Pin Voltage Rising		4.0		V
		Vcc5V Pin Voltage Falling		3.6		
	Vcc12V Minimum Working Voltage	See (5)		3.8		V
t_{SS}	Soft Start Delay	F_{OSC} = 8MHz		1.6		ms

(5) When Vcc12V pin goes below this voltage, all DRV pins go to 0V.

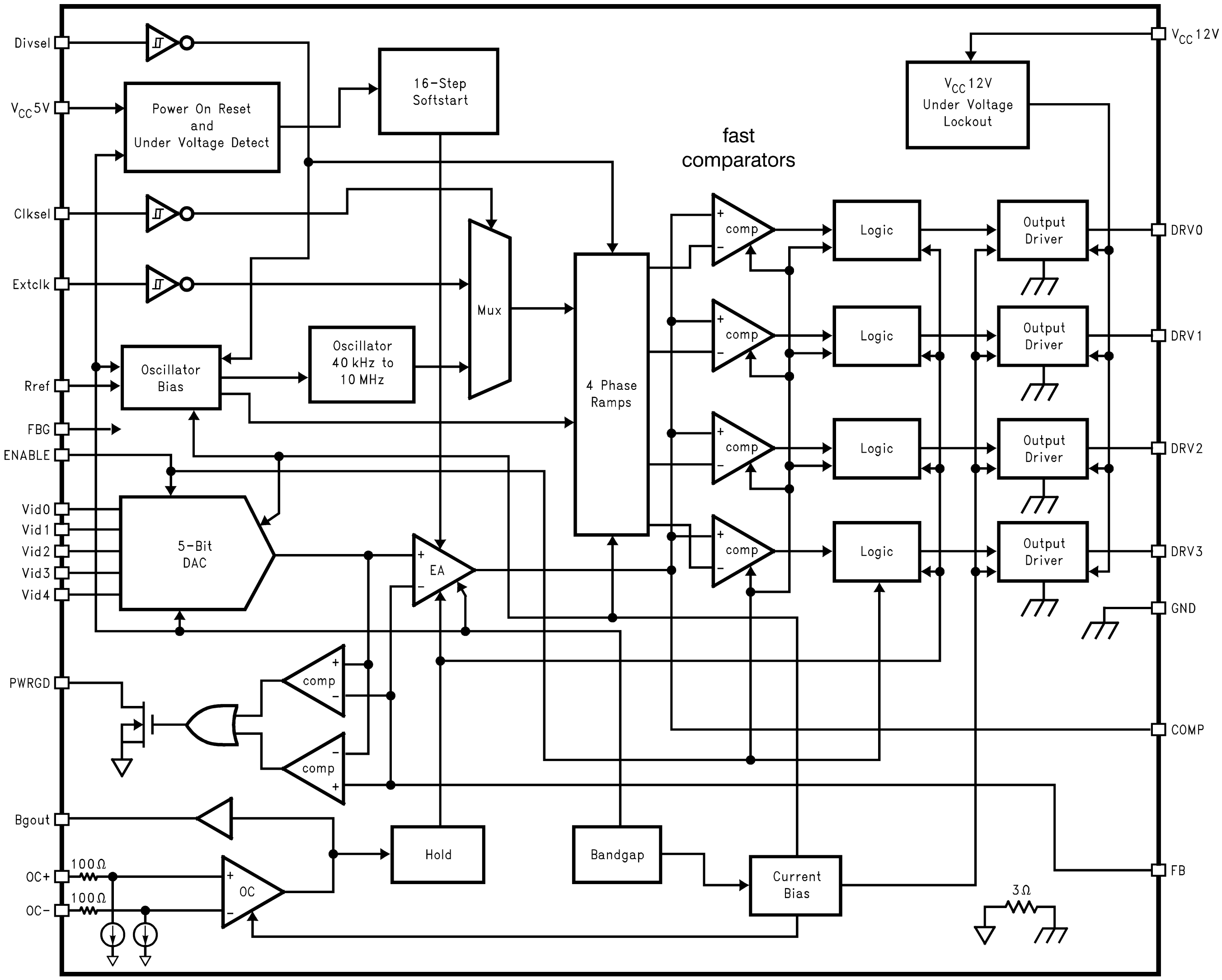
Table 1. 5-Bit DAC Output Voltage Table

Symbol	Parameter	Conditions	Typical	Units
V_{DACOUT}	5-Bit DAC Output Voltages for Different VID Codes	VID4:0 = 01111	***1.30***	V
		VID4:0 = 01110	1.35	
		VID4:0 = 01101	***1.40***	
		VID4:0 = 01100	1.45	
		VID4:0 = 01011	***1.50***	
		VID4:0 = 01010	1.55	
		VID4:0 = 01001	***1.60***	
		VID4:0 = 01000	1.65	
		VID4:0 = 00111	***1.70***	
		VID4:0 = 00110	1.75	
		VID4:0 = 00101	***1.80***	
		VID4:0 = 00100	1.85	
		VID4:0 = 00011	***1.90***	
		VID4:0 = 00010	1.95	
		VID4:0 = 00001	***2.00***	
		VID4:0 = 00000	2.05	
		VID4:0 = 11111	2.0	
		VID4:0 = 11110	2.1	
		VID4:0 = 11101	***2.2***	
		VID4:0 = 11100	2.3	
		VID4:0 = 11011	2.4	
		VID4:0 = 11010	2.5	
		VID4:0 = 11001	2.6	
		VID4:0 = 11000	2.7	
		VID4:0 = 10111	***2.8***	
		VID4:0 = 10110	2.9	
		VID4:0 = 10101	3.0	
		VID4:0 = 10100	3.1	
		VID4:0 = 10011	3.2	
		VID4:0 = 10010	***3.3***	
		VID4:0 = 10001	3.4	
		VID4:0 = 10000	3.5	

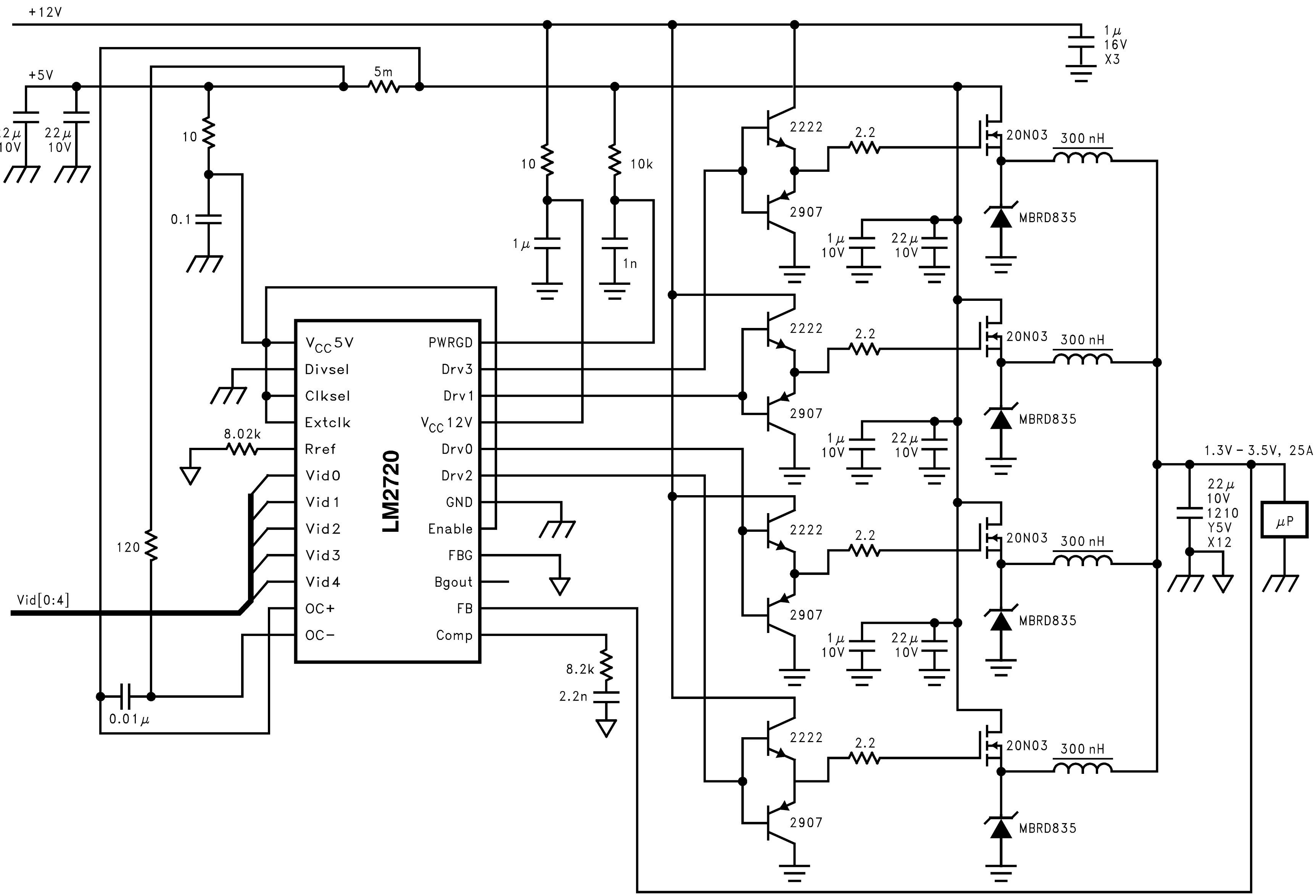
Pin Description

Pin	Pin Name	Pin Function
1	Vcc5V	Supply Voltage Input (5V nominal)
2	Divsel	Selects Phase Mode. Logic low selects 4 phase. Logic high selects 3 phase. 2 phase operation is achieved by using 2 outputs in 4 phase mode.
3	Clksel	Clock Select: Logic high selects internal clock. Logic low selects external clock.
4	Extclk	External Clock Input. Output frequency = Clock Input / No. of Phases. Connect to Vcc5V to select internal clock.
5	Rref	Connects to external reference resistor. Sets the operating frequency of the internal clock and the ramp time for the PWM. Reference voltage at this pin is 1.26V.
6	Vid0	5-Bit DAC Input (LSB).
7	Vid1	5-Bit DAC Input.
8	Vid2	5-Bit DAC Input.
9	Vid3	5-Bit DAC Input.
10	Vid4	5-Bit DAC Input (MSB)
11	OC+	Over-current Comparator. Non-inverting input.
12	OC−	Over-current Comparator. Inverting input.
13	COMP	Compensation Pin. This is the output of the internal transconductance amplifier. Compensation network should be connected between this pin and feedback ground FBG.
14	FB	Feedback Input. Normally Kelvin connected to supply output.
15	Bgout	Current Limit Flag. Goes to logic low when current limit is activated. When over-current condition is removed, this pin is weakly pulled up to Vcc5V.
16	FBG	Feedback Ground. This pin should be connected to the ground at the supply output.
17	ENABLE	Output Enable Pin. Tie to logic high to enable and logic low to disable.
18	GND	Power Ground Pin.
19	DRV2	Phase 2 Output.
20	DRV0	Phase 0 Output.
21	Vcc12V	Supply Voltage for FET Drivers DRV0:3.
22	DRV1	Phase 1 Output.
23	DRV3	Phase 3 Output.
24	PWRGD	Power Good. This is an open-drain output that goes low (low impedance to ground) when the output voltage travels out of the threshold window, and resume to open-drain state when V_{OUT} recovers into the 50mV hysteresis window. The power good window threshold, i.e. ±100mV for 1.3V ≤ V_{OUT} ≤ 1.9V or ±150mV for 2V ≤ V_{OUT} ≤ 3.5V, is automatically set according to VID code. Connect a 1nF capacitor to ground to filter out the switching noise coupling from DRV3 to this pin.

Block Diagram



Typical Application



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