# LM2765 Switched Capacitor Voltage Converter

**Check for Samples: LM2765**

## FEATURES

- **Doubles Input Supply Voltage**
- **SOT-23 6-Pin Package**
- **20Ω Typical Output Impedance**
- **90% Typical Conversion Efficiency at 20 mA**
- **0.1µA Typical Shutdown Current**

## APPLICATIONS

- **Cellular Phones**
- **Pagers**
- **PDAs**
- **Operational Amplifier Power Supplies**
- **Interface Power Supplies**
- **Handheld Instruments**

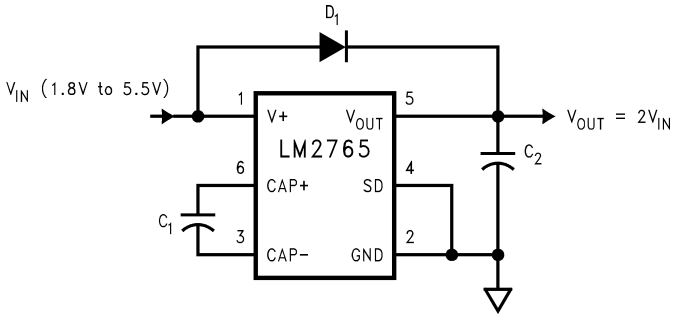
## DESCRIPTION

The LM2765 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of +1.8V to +5.5V. Two low cost capacitors and a diode are used in this circuit to provide up to 20 mA of output current.

The LM2765 operates at 50 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 130 µA (operating efficiency greater than 90% with most loads) and 0.1µA typical shutdown current, the LM2765 provides ideal performance for battery powered systems. The device is manufactured in a SOT-23 6-pin package.

### Basic Application Circuits

**Figure 1. Voltage Doubler**




### Connection Diagram

#### 6-Pin Small Outline Package

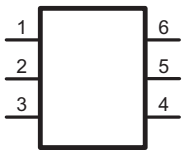



**Figure 2. DBV Package Top View**

**Figure 3. Actual Size**

## Pin Description

| Pin | Name | Function |
|---|---|---|
| 1 | V+ | Power supply positive voltage input. |
| 2 | GND | Power supply ground input. |
| 3 | CAP− | Connect this pin to the negative terminal of the charge-pump capacitor. |
| 4 | SD | Shutdown control pin, tie this pin to ground in normal operation. |
| 5 | $V_{OUT}$ | Positive voltage output. |
| 6 | CAP+ | Connect this pin to the positive terminal of the charge-pump capacitor. |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)

| | |
|---|---|
| Supply Voltage (V+ to GND, or V+ to $V_{OUT}$) | 5.8V |
| SD | (GND − 0.3V) to (V+ + 0.3V) |
| $V_{OUT}$ Continuous Output Current | 40 mA |
| Output Short-Circuit Duration to GND(3) | 1 sec. |
| Continuous Power Dissipation ($T_A$ = 25°C)(4) | 600 mW |
| $T_{JMax}$(4) | 150°C |

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) $V_{OUT}$ may be shorted to GND for one second without damage. However, shorting $V_{OUT}$ to V+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/\theta_{JA}$, where $T_{JMax}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance of the specified package.

## Operating Ratings

| | | |
|---|---|---|
| $\theta_{JA}$(1) | | 210°C/W |
| Junction Temperature Range | | −40° to 100°C |
| Ambient Temperature Range | | −40° to 85°C |
| Storage Temperature Range | | −65°C to 150°C |
| Lead Temp. (Soldering, 10 seconds) | | 240°C |
| ESD Rating (2) | Human Body Model | 2kV |
| | Machine Model | 200V |

(1) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/\theta_{JA}$, where $T_{JMax}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance of the specified package.
(2) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

## Electrical Characteristics

Limits in standard typeface are for $T_J$ = 25°C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V+ = 5V, $C_1 = C_2$ = 3.3 µF.(1)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| V+ | Supply Voltage | | **1.8** | | **5.5** | V |
| $I_Q$ | Supply Current | No Load | | 130 | **450** | µA |
| $I_{SD}$ | Shutdown Supply Current | | | 0.1 | 0.5 | µA |
| | | $T_A$ = 85°C | | 0.2 | | |
| $V_{SD}$ | Shutdown Pin Input Voltage | Shutdown Mode | **2.0** | | | V |
| | | Normal Operation | | | **0.6** | |
| $I_L$ | Output Current | 2.5V ≤ $V_{IN}$ ≤ 5.5V | **20** | | | mA |
| | | 1.8V ≤ $V_{IN}$ < 2.5V | **10** | | | |
| $R_{OUT}$ | Output Resistance(2) | $I_L$ = 20 mA | | 20 | **40** | Ω |
| $f_{OSC}$ | Oscillator Frequency | See(3) | **40** | 100 | **200** | kHz |
| $f_{SW}$ | Switching Frequency | See(3) | **20** | 50 | **100** | kHz |
| $P_{EFF}$ | Power Efficiency | $I_L$ = 20 mA to GND | | 92 | | % |
| $V_{OEFF}$ | Voltage Conversion Efficiency | No Load | | 99.96 | | % |

(1) In the test circuit, capacitors $C_1$ and $C_2$ are 3.3 µF, 0.3Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.
(2) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in the application information for positive voltage doubler.
(3) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.

## Test Circuit

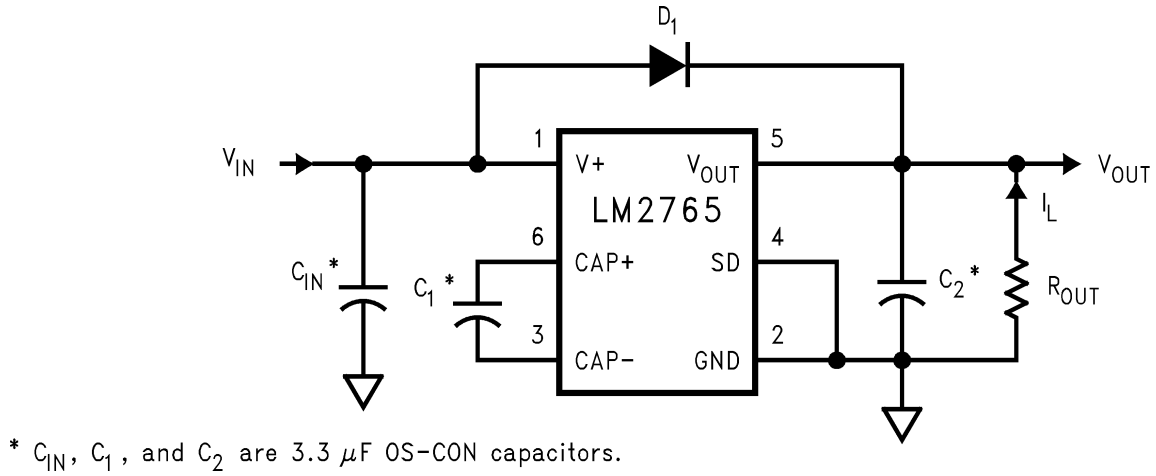



**Figure 4. LM2765 Test Circuit**

## Typical Performance Characteristics

(Circuit of Figure 4, $V_{IN}$ = 5V, $T_A$ = 25°C unless otherwise specified)

**Supply Current vs Supply Voltage**

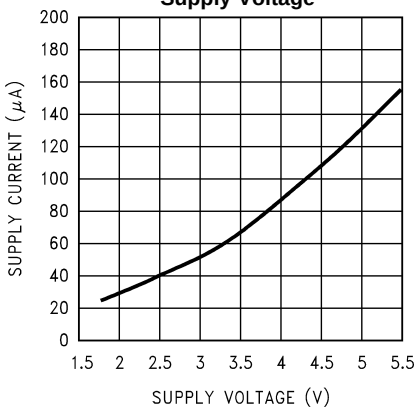



**Figure 5.**

**Output Resistance vs Capacitance**

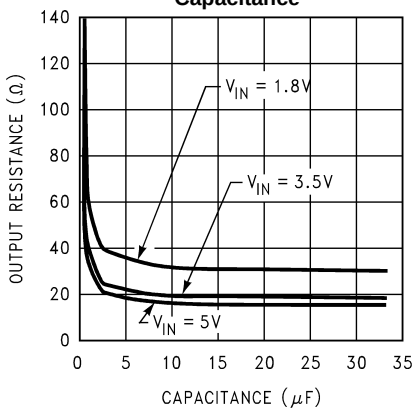



**Figure 6.**

**Output Resistance vs Supply Voltage**

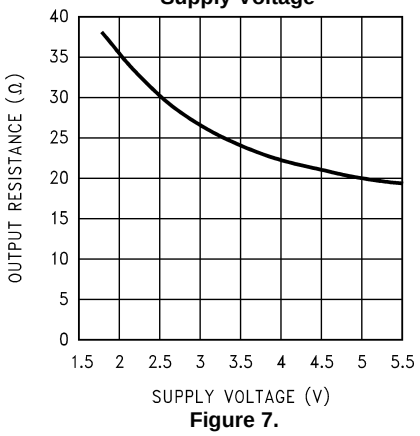



**Figure 7.**

**Output Resistance vs Temperature**

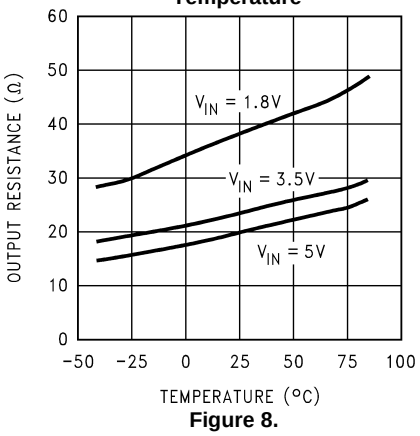



**Figure 8.**

**Output Voltage vs Load Current**

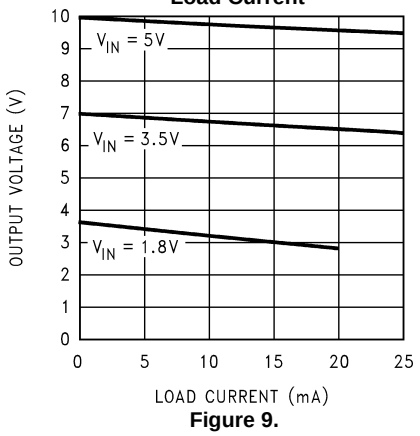



**Figure 9.**

**Efficiency vs Load Current**

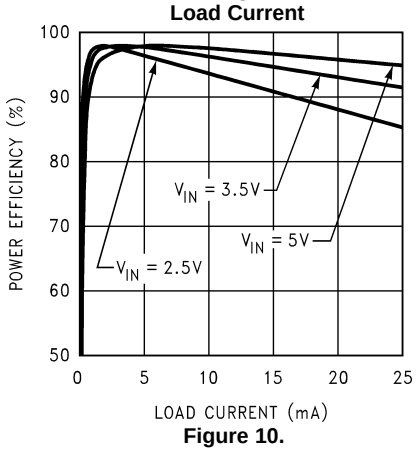



**Figure 10.**

## Typical Performance Characteristics (continued)

(Circuit of Figure 4, $V_{IN}$ = 5V, $T_A$ = 25°C unless otherwise specified)

**Switching Frequency vs Supply Voltage**

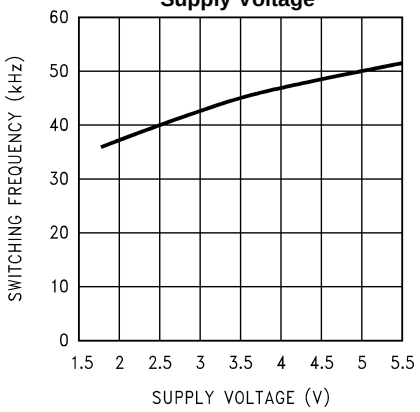



**Figure 11.**

**Switching Frequency vs Temperature**

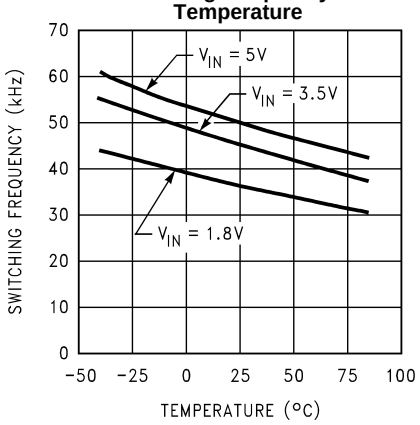



**Figure 12.**

**Output Ripple vs Load Current**

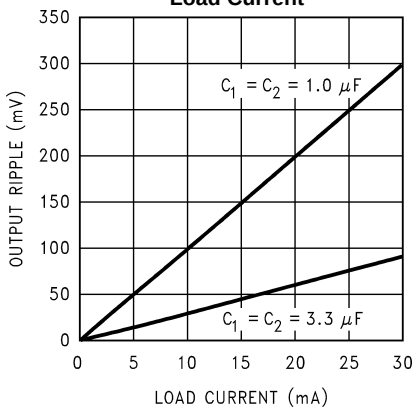



**Figure 13.**

## CIRCUIT DESCRIPTION

The LM2765 contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 14 illustrates the voltage conversion scheme. When $S_2$ and $S_4$ are closed, $C_1$ charges to the supply voltage V+. During this time interval, switches $S_1$ and $S_3$ are open. In the next time interval, $S_2$ and $S_4$ are open; at the same time, $S_1$ and $S_3$ are closed, the sum of the input voltage V+ and the voltage across $C_1$ gives the 2V+ output voltage when there is no load. The output voltage drop when a load is added is determined by the parasitic resistance ($R_{ds(on)}$ of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors. Details will be discussed in the following application information section.

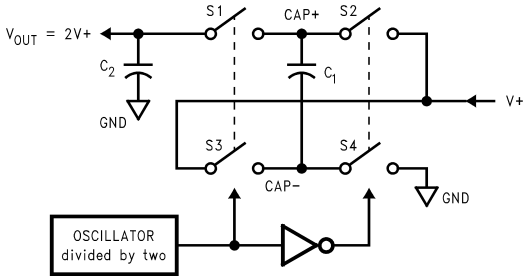



**Figure 14. Voltage Doubling Principle**

## POSITIVE VOLTAGE DOUBLER

The main application of the LM2765 is to double the input voltage. The range of the input supply voltage is 1.8V to 5.5V.

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals 2V+. The output resistance $R_{out}$ is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, and the capacitance and ESR of $C_1$ and $C_2$. Since the switching current charging and discharging $C_1$ is approximately twice as the output current, the effect of the ESR of the pumping capacitor $C_1$ will be multiplied by four in the output resistance. The output capacitor $C_2$ is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation of $R_{out}$ is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2} \quad (1)$$

where $R_{SW}$ is the sum of the ON resistance of the internal MOSFET switches shown in Figure 14. $R_{SW}$ is typically 8Ω for the LM2765.

The peak-to-peak output voltage ripple is determined by the oscillator frequency as well as the capacitance and ESR of the output capacitor $C_2$:

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

High capacitance, low ESR capacitors can reduce both the output resistance and the voltage ripple.

The Schottky diode $D_1$ is only needed to protect the device from turning-on its own parasitic diode and potentially latching-up. During start-up, $D_1$ will also quickly charge up the output capacitor to $V_{IN}$ minus the diode drop thereby decreasing the start-up time. Therefore, the Schottky diode $D_1$ should have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

## SHUTDOWN MODE

A shutdown (SD) pin is available to disable the device and reduce the quiescent current to 0.1 µA. In normal operating mode, the SD pin is connected to ground. The device can be brought into the shutdown mode by applying to the SD pin a voltage greater than 40% of the V+ pin voltage.

## CAPACITOR SELECTION

As discussed in the *Positive Voltage Doubler* section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_L{}^2 R_L}{I_L{}^2 R_L + I_L{}^2 R_{OUT} + I_Q (V+)} \quad (3)$$

Where $I_Q(V+)$ is the quiescent power loss of the IC device, and $I_L{}^2R_{out}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

The selection of capacitors is based on the specifications of the dropout voltage (which equals $I_{out}$ $R_{out}$), the output voltage ripple, and the converter efficiency. Low ESR capacitors (Table 1) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

**Table 1. Low ESR Capacitor Manufacturers**

| Manufacturer | Phone | Website | Capacitor Type |
|---|---|---|---|
| Nichicon Corp. | (847)-843-7500 | www.nichicon.com | PL & PF series, through-hole aluminum electrolytic |
| AVX Corp. | (843)-448-9411 | www.avxcorp.com | TPS series, surface-mount tantalum |
| Sprague | (207)-324-4140 | www.vishay.com | 593D, 594D, 595D series, surface-mount tantalum |
| Sanyo | (619)-661-6835 | www.sanyovideo.com | OS-CON series, through-hole aluminum electrolytic |
| Murata | (800)-831-9172 | www.murata.com | Ceramic chip capacitors |
| Taiyo Yuden | (800)-348-2496 | www.t-yuden.com | Ceramic chip capacitors |
| Tokin | (408)-432-8020 | www.tokin.com | Ceramic chip capacitors |

## Other Applications

### PARALLELING DEVICES

Any number of LM2765s can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor $C_1$, while only one output capacitor $C_{out}$ is needed as shown in Figure 15. The composite output resistance is:

$$R_{OUT} = \frac{R_{OUT} \text{ of each LM2765}}{\text{Number of Devices}} \quad (4)$$

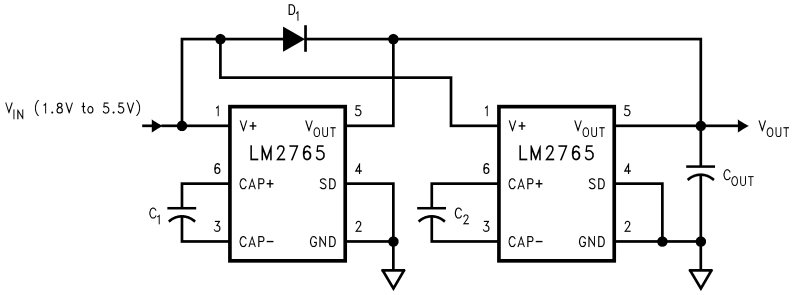



**Figure 15. Lowering Output Resistance by Paralleling Devices**

### CASCADING DEVICES

Cascading the LM2765s is an easy way to produce a greater voltage (A two-stage cascade circuit is shown in Figure 16).

The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = 1.5R_{out\_1} + R_{out\_2} \quad (5)$$

Note that increasing the number of cascading stages is pracitically limited since it significantly reduces the efficiency, increases the output resistance and output voltage ripple.

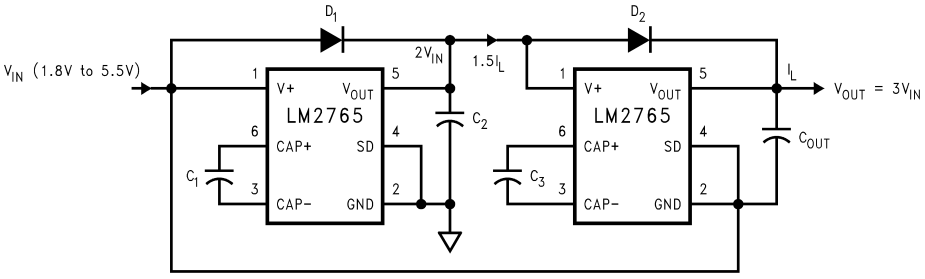



**Figure 16. Increasing Output Voltage by Cascading Devices**

## REGULATING $V_{OUT}$

It is possible to regulate the output of the LM2765 by use of a low dropout regulator (such as LP2980-5.0). The whole converter is depicted in Figure 17.

A different output voltage is possible by use of LP2980-3.3, LP2980-3.0, or LP2980-adj.

Note that the following conditions must be satisfied simultaneously for worst case design:

$$2V_{in\_min} > V_{out\_min} + V_{drop\_max} \text{ (LP2980)} + I_{out\_max} \times R_{out\_max} \text{ (LM2765)} \quad (6)$$

$$2V_{in\_max} < V_{out\_max} + V_{drop\_min} \text{ (LP2980)} + I_{out\_min} \times R_{out\_min} \text{ (LM2765)} \quad (7)$$

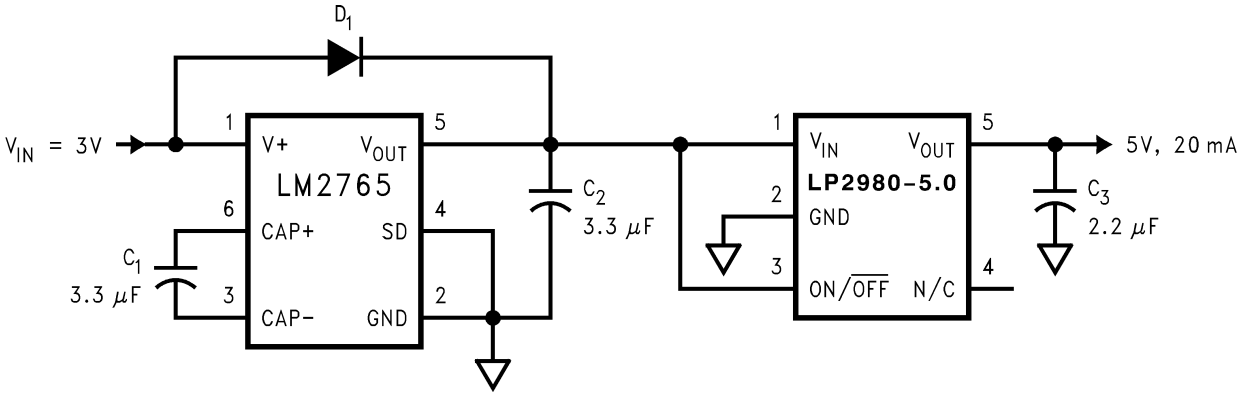



**Figure 17. Generate a Regulated +5V from +3V Input Voltage**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2765M6X | ACTIVE | SOT-23 | DBV | 6 | 3000 | TBD | Call TI | Call TI | -40 to 85 | S15B | Samples |
| LM2765M6X/NOPB | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | S15B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

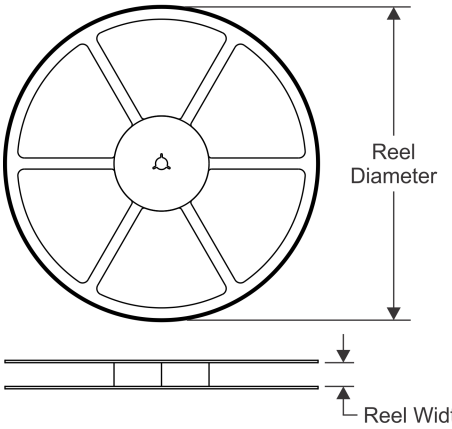
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

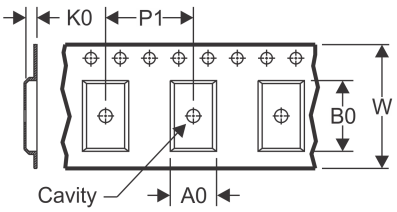
(4) Only one of markings shown within the brackets will appear on the physical device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

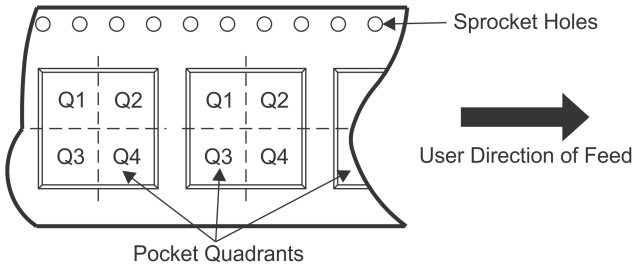



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

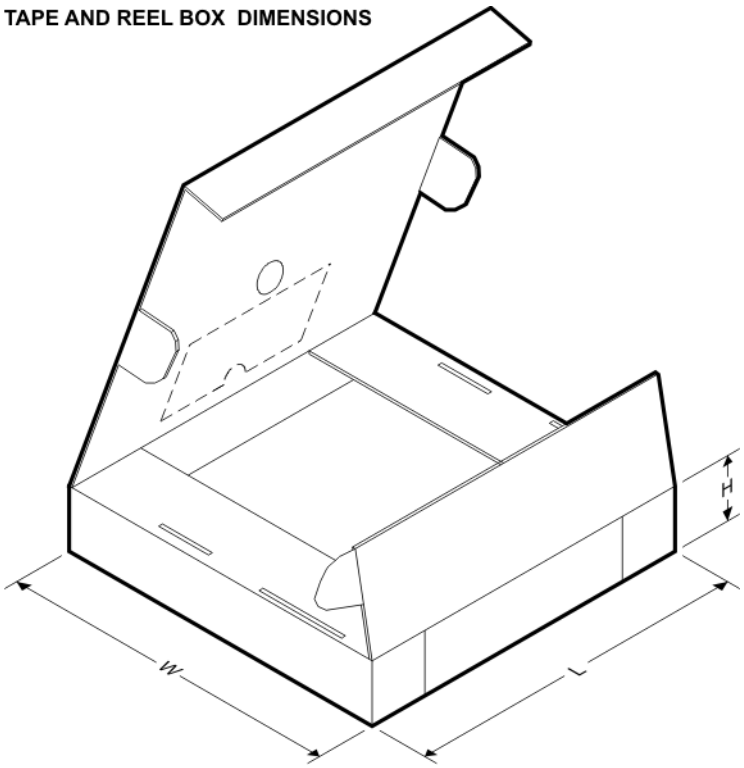
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2765M6X | SOT-23 | DBV | 6 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM2765M6X/NOPB | SOT-23 | DBV | 6 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

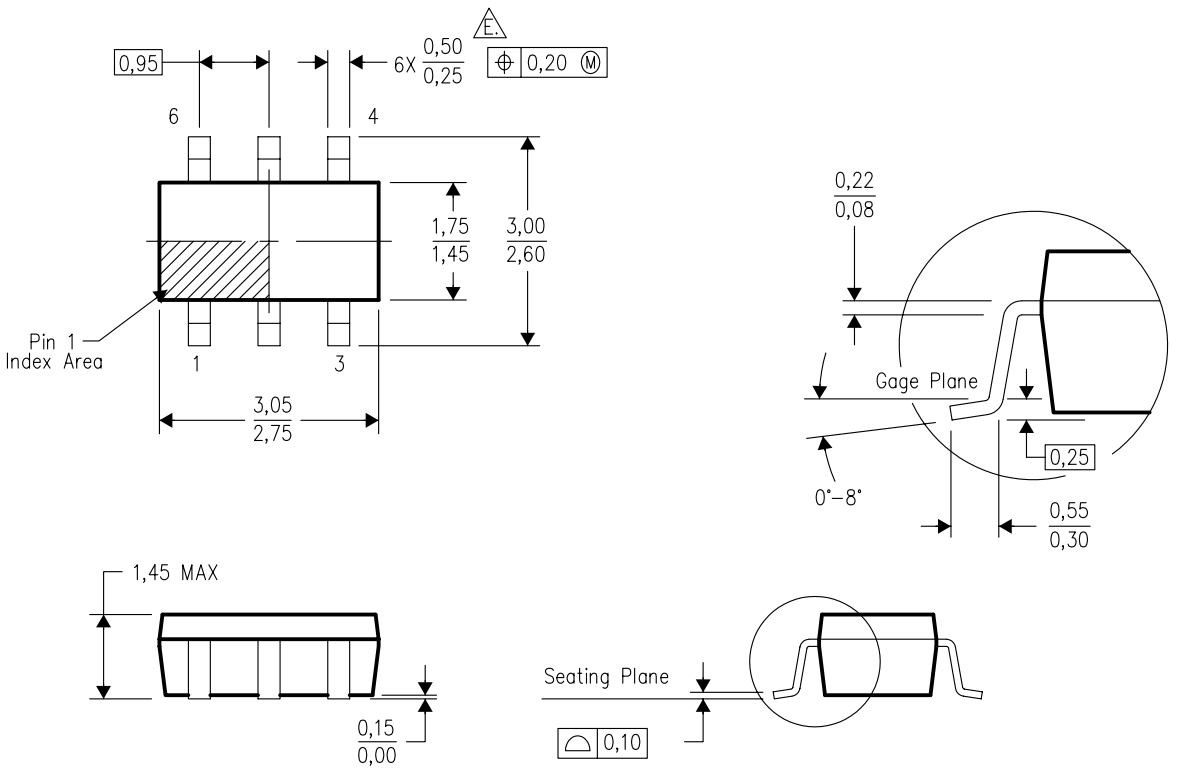
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM2765M6X | SOT-23 | DBV | 6 | 3000 | 206.0 | 191.0 | 90.0 |
| LM2765M6X/NOPB | SOT-23 | DBV | 6 | 3000 | 206.0 | 191.0 | 90.0 |

## DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

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