LINEAR INTEGRATED CIRCUITS

LM 339
LM 339A

PRELIMINARY DATA

QUAD VOLTAGE COMPARATOR

The LM 339 and the LM 339A are monolithic integrated circuits in a 14-lead dual in-line plastic package and in a 14-lead micropackage. They consists of four independent precision voltage comparators and are specially designed to offer a versatility as high as possible; application areas include limit comparators, A/D converters, waveforms generators, high voltage logic gates and so on. Furthermore, the open collector output stage provides easy interfacing with all types of logic circuitry.
The LM 339/LM 339A main features are:

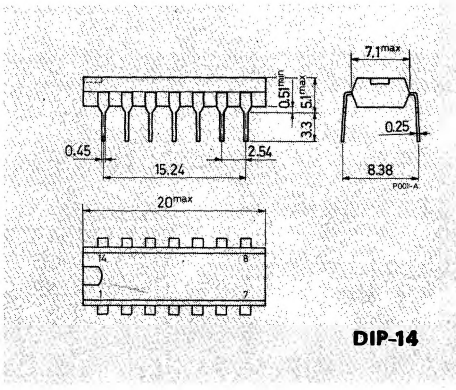
- Wide supply range (2 to 36V)
- **Single or split supply operation**
- Very low current consumption (0.8 mA, regardless of supply voltage)
- Ground input compatibility
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Output short circuit to ground continuous

ABSOLUTE MAXIMUM RATINGS

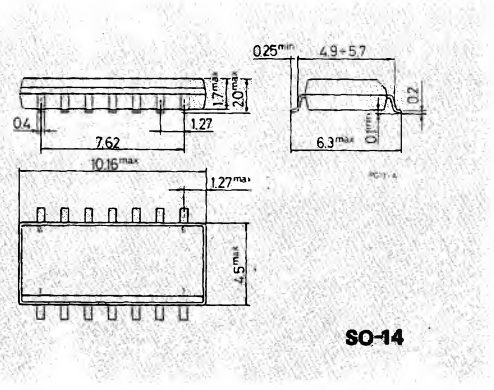
V_s	Supply voltage	± 18 or +36	V
V_I	Input voltage range	-0.3 to 36	V
V_i	Differential input voltage	36	V
I_i	Input current ($V_{in} < -0.3\ V_{dc}$)	50	mA
P_{tot}	Total power dissipation at $T_{amb} = 25°C$	600	mW
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage and junction temperature	-65 to 150	°C

MECHANICAL DATA

Dimensions in mm

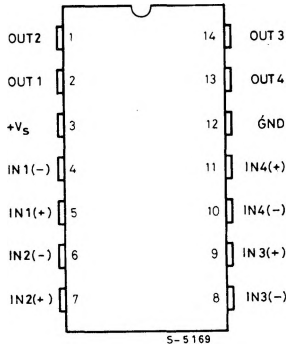


DIP-14



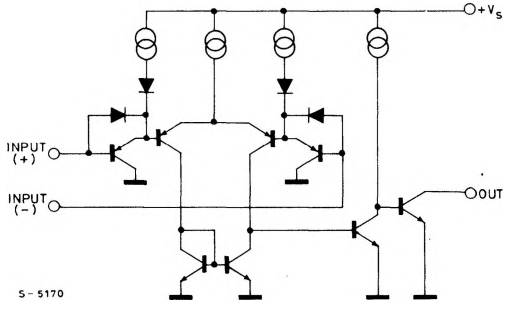
SO-14

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Type	DIP14	SO-14
LM 339 LM 339A	LM 339N LM 339AN	LM 339CM —

SCHEMATIC DIAGRAM
(each section)



THERMAL DATA

			DIP-14	SO-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200 °C/W	200 °C/W*

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s = +5V for the LM 339; V_s = +15V for the LM 339A; T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		LM 339A			L339			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	At out.switch point; $V_o \cong 1.4V$; $R_g = 0$ $V_{REF} = 1.4\ V_{dc}$			± 1	± 2		± 2	± 5	mV
			T_{amb} = 0 to 70°C			± 4			± 9	
I_b	Input bias current (1)	Output in linear range			25	250		25	250	nA
			T_{amb} = 0 to 70°C			400			400	
I_{os}	Input offset current				± 5	±50		± 5	±50	nA
			T_{amb} = 0 to 70°C			±150			±150	
	Input Common-Mode voltage range (2)			0		V_s-1.5	0		V_s-1.5	V
			T_{amb} = 0 to 70°C	0		V_s-2	0		V_s-2	
I_s	Supply current	$R_L = \infty$			0.8	2		0,8	2	mA
G_v	Voltage gain	$R_L \geq 15\ K\Omega$		94	106			106		dB
	Large signal response time	V_{IN} = TTL logic swing; V_{REF} = +1.4V; R_L = 5.1 KΩ V_{RL} = 5V			300			300		nsec
	Response time (3)	V_{RL} = 5V; R_L = 5.1 KΩ			1.3			1.3		μsec
I_o	Output sink current	$V_{IN(-)} \geq 1V$; $V_{IN(+)} = 0V$; $V_o \leq 1.5V$		6	16		6	16		mA
V_{sat}	Output saturation voltage	$V_{IN(-)} \geq 1V$ $V_{IN(+)} = 0V$ $I_{sink} \leq 4\ mA$			250	500		250	500	mV
			T_{amb} = 0 to 70°C			700			700	
$I_{o\ leak}$	Output leakage current	$V_{IN(+)} \geq 1V$ $V_{IN(-)} = 0V$	V_o = 5V		0.1			0.1		nA
			T_{amb} = 0 to 70°C V_o = 30V			1			1	μA
	Differential input voltage	All $V_{IN} \geq 0V$ (or $-V_s$ if split supply is used); T_{amb} = 0 to 70°C				36			36	V

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This condition is not destructive providing the input current is limited to less than 50 mA.

(3) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 nsec can be obtained.

APPLICATION INFORMATION

The LM 339 includes four high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.
To minimize this problem, PC board layout should be designed to reduce stray input-output coupling; reducing the input resistors to less than 10 KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.
It is good design practice to ground all unused pins.
The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than -0.3V should not be used: an input clamping diode can be used as protection.

The output of the LM 339 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.
The output sink current capability is approximately 16 mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.
Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

Fig. 1 - Basic comparator

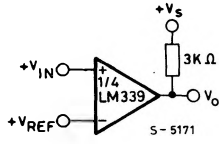


Fig. 2 - Non-inverting comparator with Hysteresis

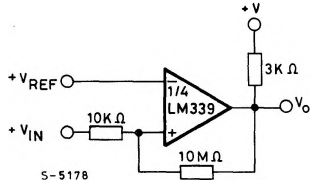


Fig. 3 - Inverting comparator with Hysteresis

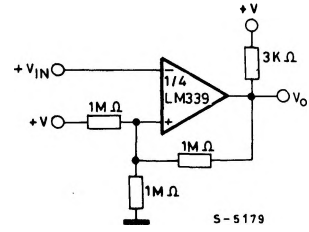


Fig. 4 - Driving C/MOS

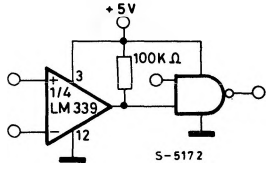
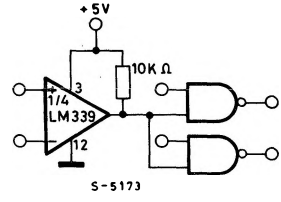


Fig. 5 - Driving TTL



APPLICATION INFORMATION (continued)

Fig. 6 - AND gate

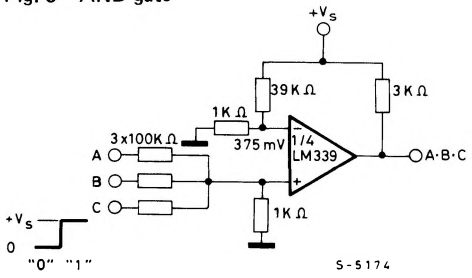


Fig. 7 - OR gate

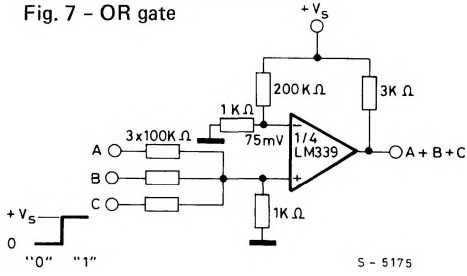


Fig. 8 - Large fan-in AND gate

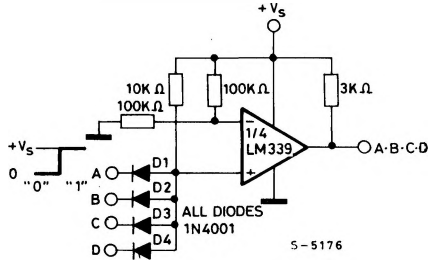


Fig. 9 - Squarewave oscillator

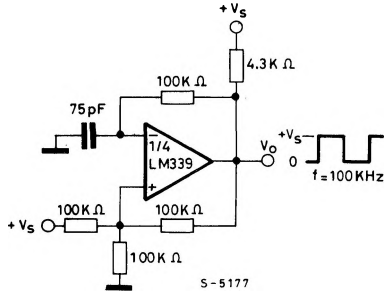


Fig. 10 - Time delay generator

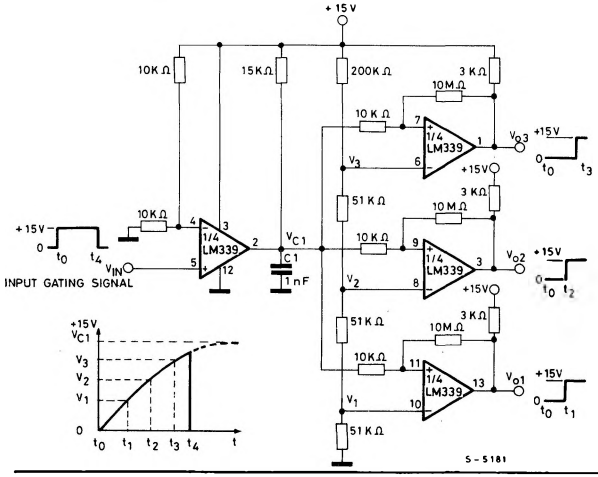
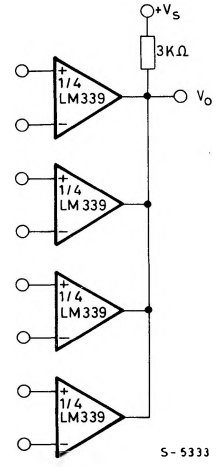


Fig. 11 - ORing the outputs



APPLICATION INFORMATION (continued)

Fig. 12 - Peak audio level display

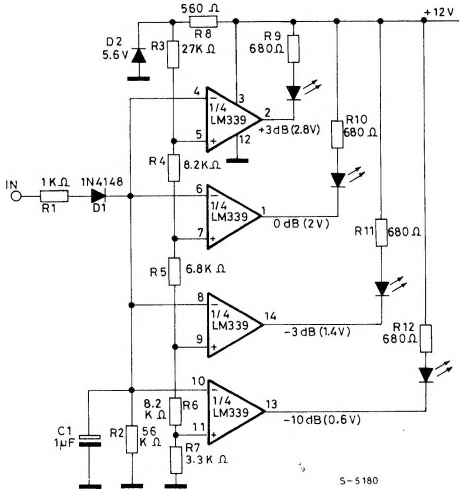


Fig. 13 - PC Board and component layout of the circuit of fig. 12

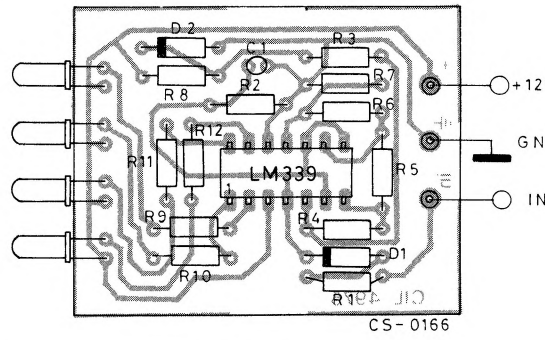
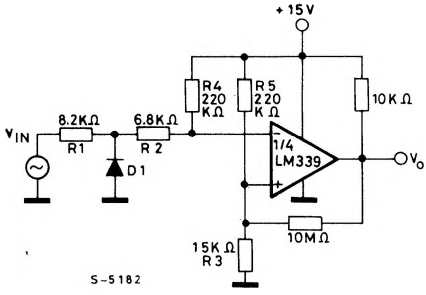


Fig. 14 - Zero crossing detector (single supply)



D1 prevents input from going negative by more than 0.6V:

$$R1 + R2 = R3$$

$$R3 \leqslant \frac{R5}{10}$$ for smaller error in zero crossing

Fig. 15 - Zero crossing detector (split supplies)

$V_{INmin} \approx 0.4V$ peak for 1% phase distortion ($\Delta\ \theta$)