Ultra Small 33V, 1A Constant On-Time Buck Switching Regulator with Intelligent Current Limit

Check for Samples: LM34930

FEATURES

- **Operating Input Voltage Range: 8V to 33V**
- **Input Over-Voltage Shutdown at 36V**
- **Input Absolute Maximum Rating of 44V**
- **Integrated 1A N-Channel Buck Switch**
- **Adjustable Output Voltage From 2.5V**
- **Switching Frequency Adjustable to 2 MHz**
- **Switching Frequency Remains Nearly Constant With Load Current and Input Voltage**
- **Ultra-Fast Transient Response**
- **No Loop Compensation Required**
- **Adjustable Soft-Start Timing**
- **Thermal Shutdown**
- **Precision 2% Feedback Reference**
- **Input Over-Voltage Indicator at 19V**
- **Current Limit Scheme Helps Prevent Inductor From Saturation in Load Fault Conditions**

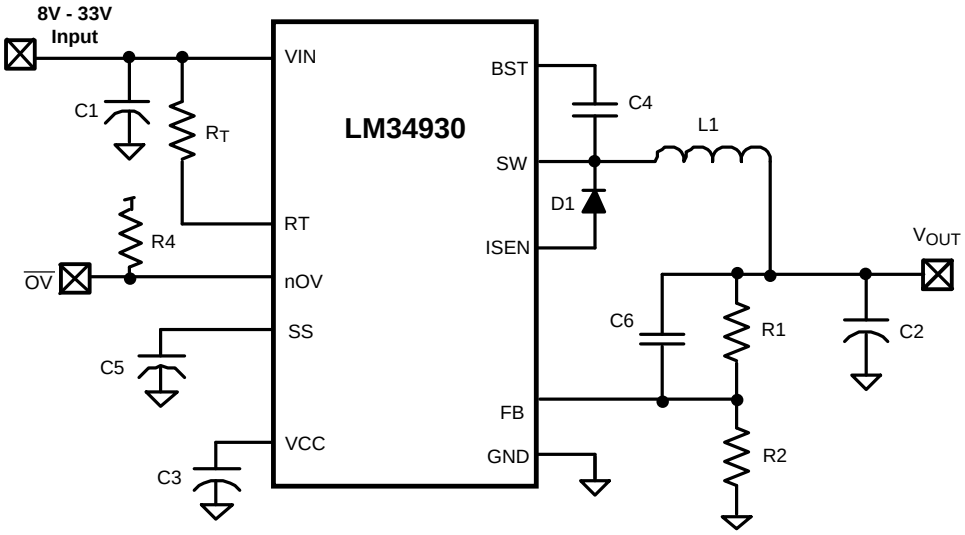
PACKAGE

- **DSBGA-12, 1.77 mm x 2.1 mm**

DESCRIPTION

The LM34930 constant On-Time Step Down Switching Regulator features all the functions needed to implement a low cost, efficient, buck bias regulator capable of supplying in excess of 1A load current. This high voltage regulator contains an N-Channel Buck Switch, and is available in a DSBGA bumped package. The constant on-time regulation principle requires no loop compensation, results in fast load transient response, and simplifies circuit implementation. The operating frequency remains constant with line and load. The valley current limit results in a smooth transition from constant voltage to constant current mode when current limit is detected without the use of current limit foldback. To reduce the possibility of saturating the inductor the valley current limit threshold reduces as the input voltage increases, and the on-time is reduced when current limit is detected. Additional features include: Over-voltage indicator, Input over-voltage shutdown, Vcc under-voltage lock-out, thermal shutdown, and maximum duty cycle limiting.

Typical Application, Basic Step-Down Regulator



Connection Diagram

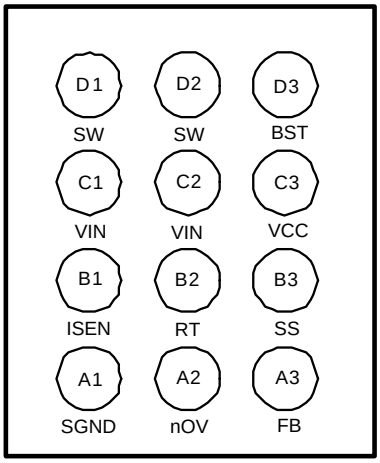


Figure 1. Bump Side

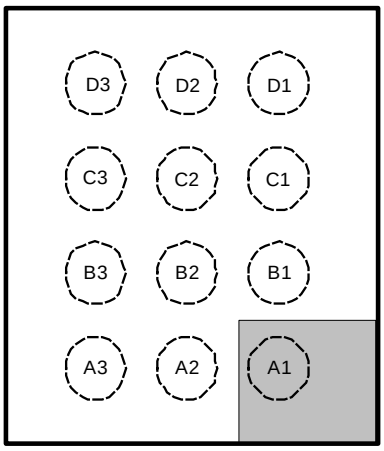


Figure 2. Top View

PIN DESCRIPTIONS

Pin No.	Name	Description	Application Information
A1	GND	Ground	Ground for all internal circuitry
A2	nOV	Input over-voltage indicator	Open drain output switches low when Vin exceeds the over-voltage indicator threshold
A3	FB	Output voltage feedback	Internally connected to the regulation comparator. The regulation level is 2.52V.
B1	ISEN	Current sense	The re-circulating current flows out of this pin to the free-wheeling diode.
B2	RT	On-time control	An external resistor from VIN to this pin sets the buck switch on-time, and the switching frequency.
B3	SS	Soft-Start	An internal current source charges an external capacitor to provide the soft-start function.
C1, C2	VIN	Input supply voltage	Operating input range is 8V to 33V, with over-voltage shutdown internally set at 36V. Absolute maximum transient capability is 44V.
C3	VCC	Output of the internal bias regulator	Nominally regulated at 7V.
D1, D2	SW	Switching node	Internally connected to the buck switch source. Connect to the external inductor, free wheeling diode, and bootstrap capacitor.
D3	BST	Bootstrap capacitor connection of the buckswitch gate driver	Connect a 0.022 µF capacitor from SW to this pin. The capacitor is charged during the buck switch off-time via an internal diode.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

VIN to GND		44V
BST to GND		52V
SW to GND (Steady State)		-1.5V to 44V
BST to SW		14V
VCC to GND		-0.3V to 8V
All Other Inputs to GND		-0.3 to 7V
Current out of ISEN		(See text)
ESD Rating (3)	Human Body Model	2kV
Storage Temperature Range		-65°C to +150°C
Junction Temperature		150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings(1)

V_{IN} Voltage	8V to 33V
Junction Temperature	−40°C to + 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications with standard type are for T_J = 25°C only; limits in **boldface** type apply over the Operating Junction Temperature (T_J) range of −40°C to + 125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V, R_T = 50 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Start-Up Regulator, V_{CC}(1)						
V_{CC}Reg	V_{CC} regulated voltage		**6.6**	7.0	**7.4**	V
	V_{IN} - V_{CC} dropout voltage	I_{CC} = 0 mA, V_{CC} = $UVLO_{VCC}$ + 250 mV		1.3		V
	V_{CC} output impedance	V_{IN} = 8V		155		Ω
	V_{CC} current limit	V_{CC} = 0V		15		mA
$UVLO_{VCC}$	V_{CC} under-voltage lockout threshold	V_{CC} increasing		5.25		V
	$UVLO_{VCC}$ hysteresis	V_{CC} decreasing		150		mV
	$UVLO_{VCC}$ filter delay	100 mV overdrive		2		µs
I_Q	I_{IN} operating current	Non-switching, FB = 3V		0.8	**1.5**	mA
Switch Characteristics						
Rds(on)	Buck Switch Rds(on)	I_{TEST} = 200 mA		0.33	**0.7**	Ω
$UVLO_{GD}$	Gate Drive UVLO		**2.7**	3.7	**4.5**	V
	$UVLO_{GD}$ hysteresis			300		mV
Softstart Pin						
V_{SS}	Pull-up voltage	SS open		2.52		V
I_{SS}	Internal current source			10		µA
V_{SS-SH}	Shutdown Threshold			70		mV

(1) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading

Electrical Characteristics (continued)

Specifications with standard type are for T_J = 25°C only; limits in **boldface** type apply over the Operating Junction Temperature (T_J) range of −40°C to + 125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V, R_T = 50 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Current Limit						
I_{LIM}	Threshold	V_{IN} = 8V	**0.95**	1.15	**1.35**	A
		V_{IN} = 30V	**0.90**	1.1	**1.30**	
	Resistance from ISEN to SGND			98		mΩ
Over-Voltage Indicator						
nOV_{TH}	Threshold voltage at VIN	V_{IN} increasing	**17.5**	19	**20.0**	V
nOV_{HYS}	Threshold hysteresis			1.95		V
nOV_{VOL}	Output low voltage	I_{noV} = 1 mA, VIN = 22V		100	**200**	mV
nOV_{LKG}	Off state leakage	V_{noV} = 7V		0.1		µA
On Timer						
t_{ON} - 1	On-time	V_{IN} = 10V, R_T = 50 kΩ	190	292	430	ns
t_{ON} - 2	On-time	V_{IN} = 33V, R_T = 50 kΩ		127		ns
t_{ON} - 3	On-time (current limit)	V_{IN} = 10V, R_T = 50 kΩ		150		ns
Off Timer						
t_{OFF}	Minimum Off-time			90		ns
Regulation Comparator (FB Pin)						
V_{REF}	FB regulation threshold	SS Pin = steady state	**2.470**	2.52	**2.575**	V
	FB bias current			1		nA
Input Over-voltage Shutdown						
$V_{IN(OV)}$	Threshold voltage at V_{IN}	V_{IN} increasing	**34.0**	36	**38.3**	V
$V_{IN(OV)-HYS}$	Hysteresis			0.4		V
Thermal Shutdown						
T_{SD}	Thermal shutdown	T_J increasing		155		°C
	Thermal shutdown hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient 0 LFPM Air Flow	JEDEC 4 layer board (2)		65		°C/W

(2) JEDEC test board description can be found in JESD 51-7.

Typical Performance Characteristics

Efficiency at 1.5 MHz

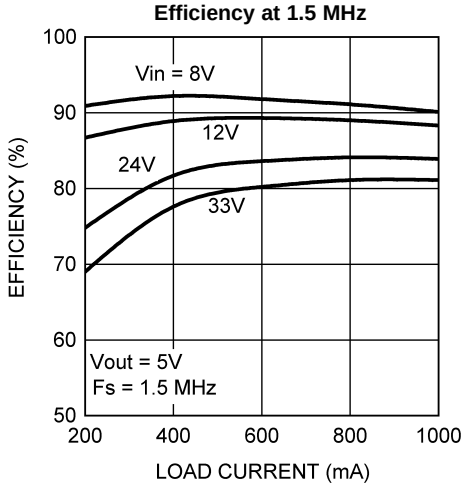


Figure 3.

Efficiency at 2 MHz

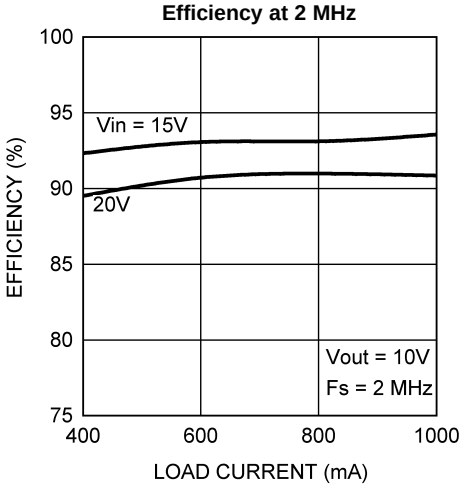


Figure 4.

V_{CC} vs V_{IN}

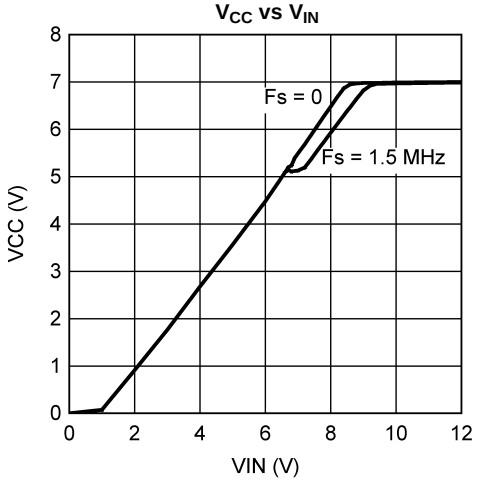


Figure 5.

V_{CC} vs I_{CC}

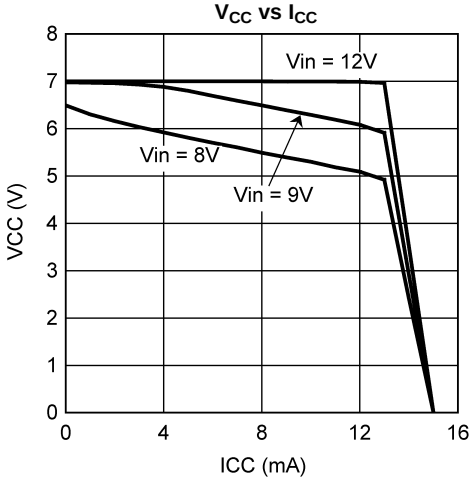


Figure 6.

ON-TIME vs V_{IN} and R_T

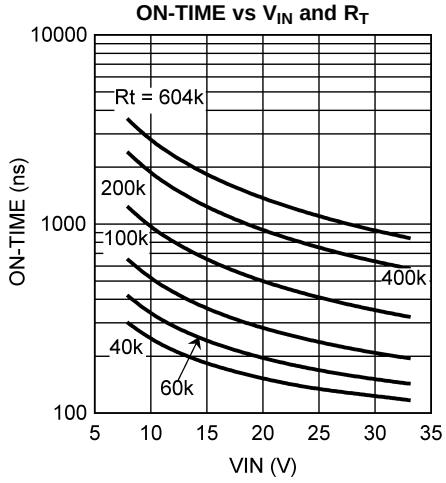


Figure .

Voltage at the R_T Pin

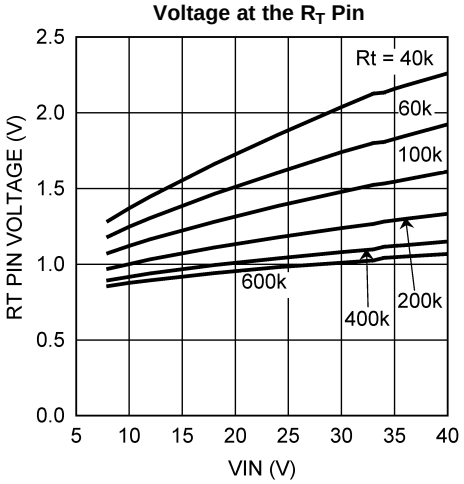


Figure 7.

Typical Performance Characteristics (continued)

Shutdown Current into V_{IN}

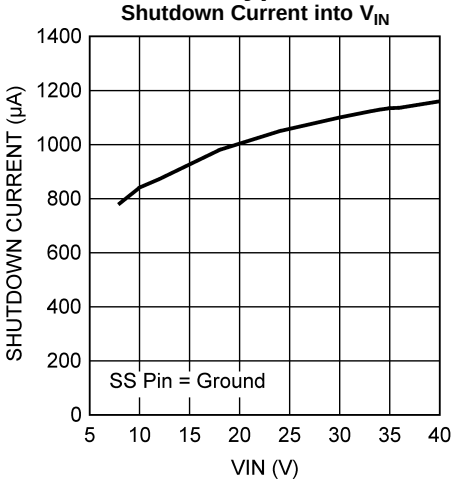


Figure .

Operating Current into V_{IN}

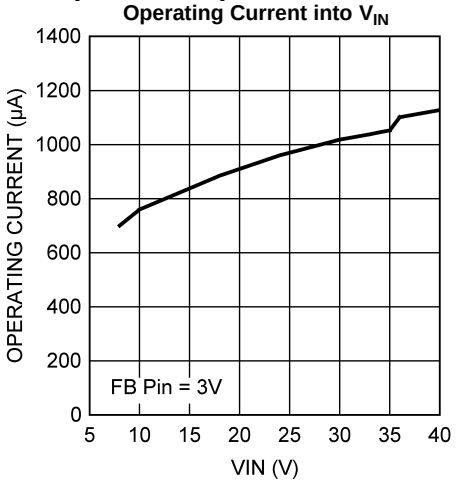


Figure 8.

Current Limit Valley Threshold vs V_{IN}

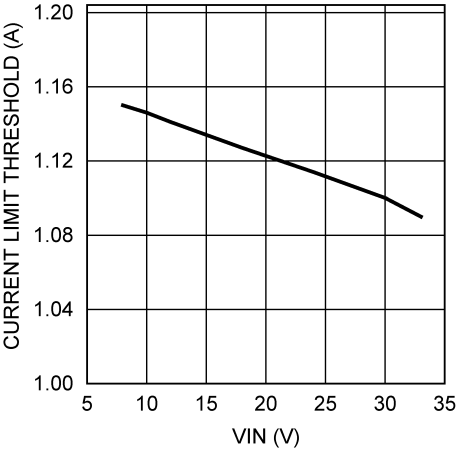


Figure 9.

nOV Low Voltage vs Sink Current

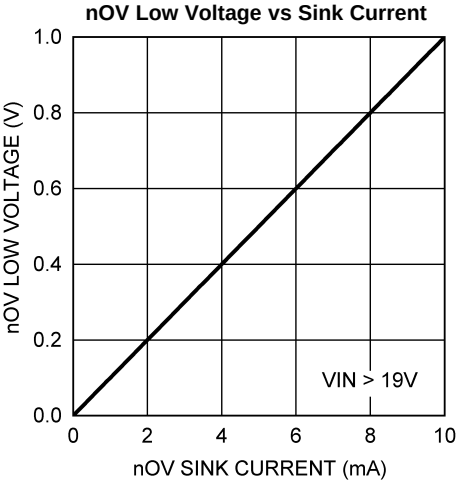


Figure 10.

Reference Voltage vs Temperature

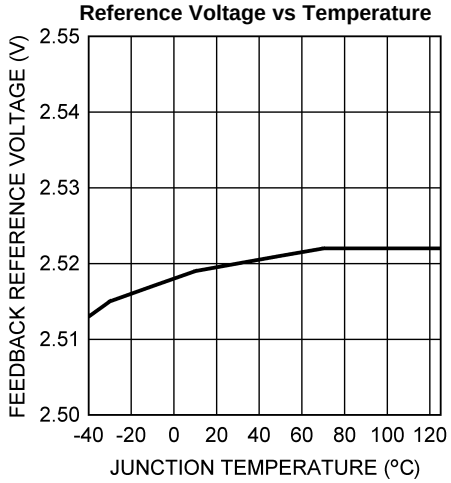


Figure 11.

Current Limit Threshold vs Temperature

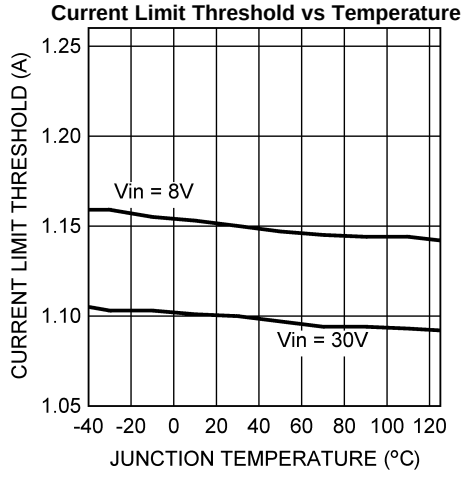


Figure 12.

Typical Performance Characteristics (continued)

V_{CC} Voltage vs Temperature

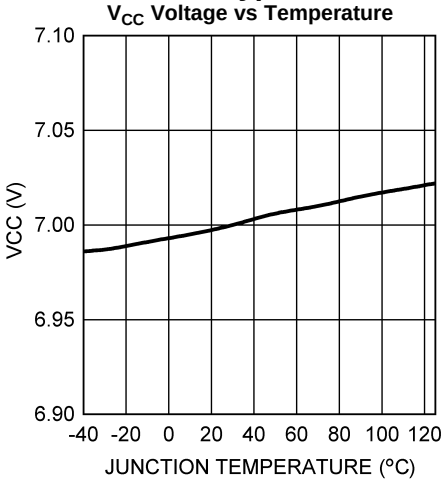


Figure 13.

On-Time vs Temperature

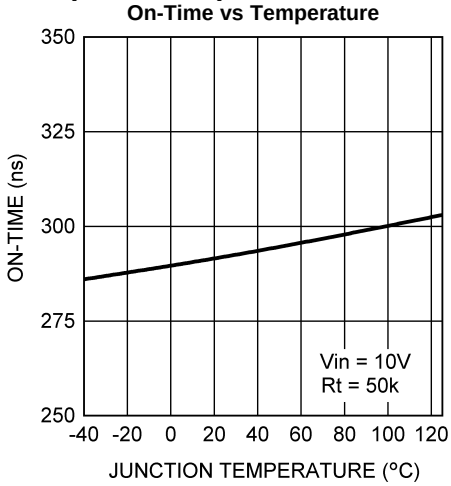
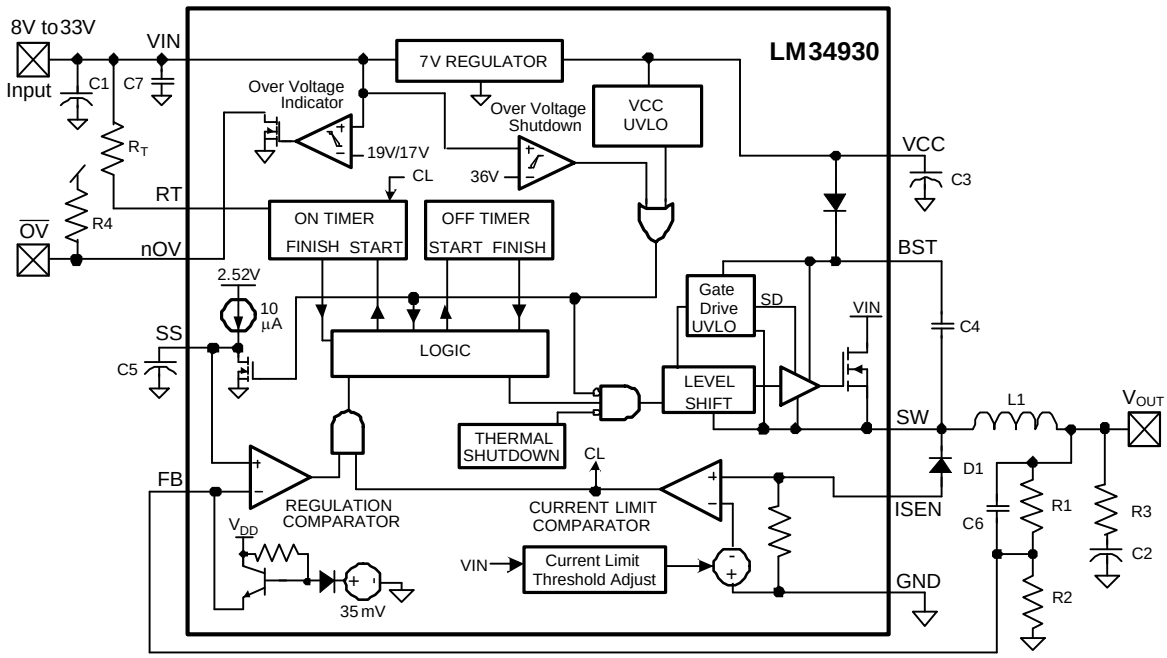


Figure 14.

TYPICAL APPLICATION CIRCUIT AND BLOCK DIAGRAM



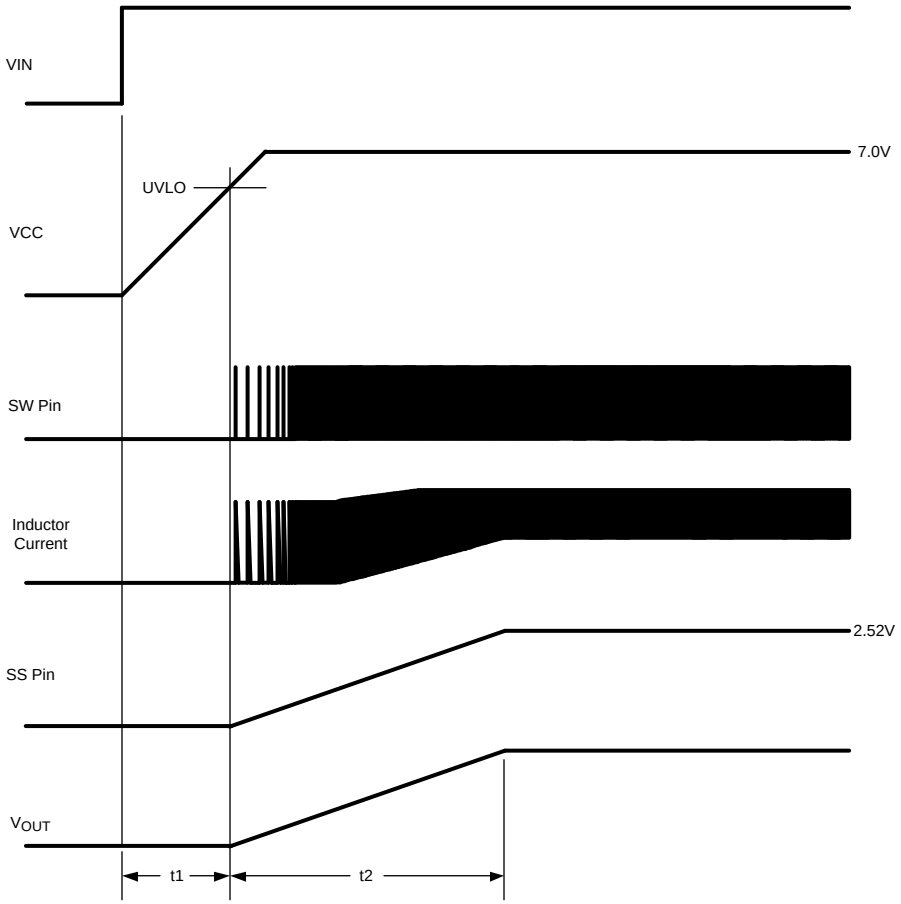


Figure 15. Start Up Sequence

FUNCTIONAL DESCRIPTION

The LM34930 Constant On-Time Step Down Switching Regulator features all the functions needed to implement a low cost, efficient buck bias power converter capable of supplying at least 1.0A to the load. This high voltage regulator contains an N-Channel buck switch, is easy to implement, and is available in a 12 bump DSBGA package. The regulator's operation is based on a constant on-time control principle where the on-time is inversely proportional to the input voltage. This feature results in the operating frequency remaining relatively constant with load and input voltage variations. The constant on-time feedback control principle requires no loop compensation resulting in very fast load transient response. The valley current limit detection results in a smooth transition from constant voltage to constant current when current limit is reached. To aid in controlling excessive switch current due to a possible saturating inductor the valley current limit threshold reduces as the input voltage increases, and the on-time is reduced by ≅50% when current limit is detected.

The LM34930 can be applied in numerous applications to efficiently step down higher voltages in non-isolated applications. Additional features include: Thermal shutdown, V_{CC} under-voltage lock-out, gate driver under-voltage lock-out, maximum duty cycle limiting, input over-voltage shutdown, and input over-voltage indicator.

Control Circuit Overview

The LM34930 buck regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (2.52V). If the FB voltage is below the reference the buck switch is switched on for the one-shot timer period which is a function of the input voltage and the programming resistor (R_T). Following the on-time the switch remains off until the FB voltage falls below the reference, but never less than the minimum off-time forced by the off-time one-shot timer. When the FB pin voltage falls below the reference and the off-time one-shot period expires, the buckswitch is then turned on for another on-time one-shot period.

When in regulation, the LM34930 operates in continuous conduction mode at heavy load currents and discontinuous conduction mode at light load currents. In continuous conduction mode the inductor's current is always greater than zero, and the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The approximate operating frequency is calculated as follows:

$$F_S = \frac{V_{OUT} \times (V_{IN} - 0.8V)}{[(4.15 \times 10^{-11} \times (R_T + 0.5\ k)) + ((V_{IN} - 0.8V) \times 65\ ns)] \times V_{IN}} \quad (1)$$

The buck switch duty cycle is approximately equal to:

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times F_S = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In discontinuous conduction mode, the inductor's current reaches zero during the off-time because of the longer-than-normal off-time. The operating frequency is lower than in continuous conduction mode, and varies with load current. Conversion efficiency is maintained at light loads since the switching losses are reduced with the reduction in load and frequency. The approximate discontinuous operating frequency can be calculated as follows:

$$F_S = \frac{V_{OUT}^2 \times L1 \times 1.16 \times 10^{21}}{R_L \times R_T^2} \quad (3)$$

where R_L = the load resistance, and L1 is the circuit's inductor.

The output voltage is set by the two feedback resistors (R1, R2 in the Block Diagram). The regulated output voltage is calculated as follows:

$$V_{OUT} = 2.52 \times (R1 + R2) / R2 \quad (4)$$

Output voltage regulation requires a minimum of 25 mVp-p ripple voltage be supplied to the feedback pin (FB). In the typical application circuit shown with the Block Diagram, ripple is generated by the inductor's ripple current passing through R3 in series with the output capacitor. The output ripple is passed to the FB pin by C6, avoiding attenuation by resistors R1 and R2.

On-Time Timer

The on-time for the LM34930 is determined by the R_T resistor and the input voltage (V_{IN}), calculated from:

$$t_{ON} = \frac{4.15 \times 10^{-11} \times (R_T + 0.5\ k)}{V_{IN} - 0.8V} + 65\ ns \quad (5)$$

The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. To set a specific continuous conduction mode switching frequency (F_S), the R_T resistor is determined from the following:

$$R_T = \left[\left(\frac{V_{OUT}}{V_{IN} \times F_S} - 65\ ns\right) \times \frac{(V_{IN} - 0.8V)}{4.15 \times 10^{-11}}\right] - 0.5\ k\Omega \quad (6)$$

The on-time must be chosen greater than 90 ns for proper operation. Equation 1, Equation 5, and Equation 6 are valid only when the regulator is not in current limit. When the LM34930 operates in current limit, the on-time is reduced by ≅50%. This feature reduces the peak inductor current which may be excessively high if the load current and the input voltage are simultaneously high. This feature operates on a cycle-by-cycle basis until the load current is reduced and the output voltage resumes its normal regulated value.

The maximum continuous current into the RT pin must be less than 2 mA. For high frequency applications, the maximum switching frequency is limited at the maximum input voltage by the minimum on-time one-shot period. At minimum input voltage the maximum switching frequency is limited by the minimum off-time one-shot period, which may prevent achievement of the proper duty cycle.

Current Limit

Current limit detection occurs during the off-time by monitoring the recirculating diode current flowing out of the ISEN pin. Referring to the Block Diagram, during the off-time the inductor current flows through the load, into the GND pin, through the internal sense resistor, out of ISEN and through D1 to the inductor. If that current exceeds the current limit threshold the current limit comparator delays the start of the next on-time period. The next on-time starts when the current out of ISEN reduces to the threshold **and** the voltage at FB is below 2.52V. The operating frequency is typically lower in the current limited condition due to longer-than-normal off-times.

The valley current limit threshold is a function of the input voltage (V_{IN}) as shown in the graph “Current Limit Valley Threshold vs. V_{IN}”. This feature reduces the inductor current’s peak value at high line and load. To further reduce the inductor’s peak current, the next on-time after current limit detection is reduced by ≅50% if the voltage at the FB comparator is below its threshold when the inductor current falls below the current limit threshold (V_{OUT} is low due to current limiting).

Figure 16 illustrates the inductor current waveform during normal operation and in current limit. During the first “Normal Operation” interval the load current is I_{O1}, the average of the inductor current waveform. As the load resistance is reduced, the inductor current increases until the lower peak of the inductor ripple current exceeds the current limit threshold. During the “Current Limited” portion of Figure 16, each on-time is reduced by ≅50%, resulting in lower ripple amplitude for the inductor’s current. During this time the LM34930 is in a constant current mode with an average load current equal to the current limit threshold plus half the ripple current (I_{OCL}), and the output voltage is below the normal regulated value. Normal operation resumes when the load current is reduced to I_{O2}, allowing V_{OUT} and the on-time to return to their normal values. Note that in the second period of “Normal Operation”, even though the inductor’s peak current exceeds the current limit threshold during part of each cycle, the circuit is not in current limit since the inductor current falls below the current limit threshold during each off time.

The peak current allowed through the buck switch, and the ISEN pin, is 2A, and the maximum allowed average current is 1.5A.

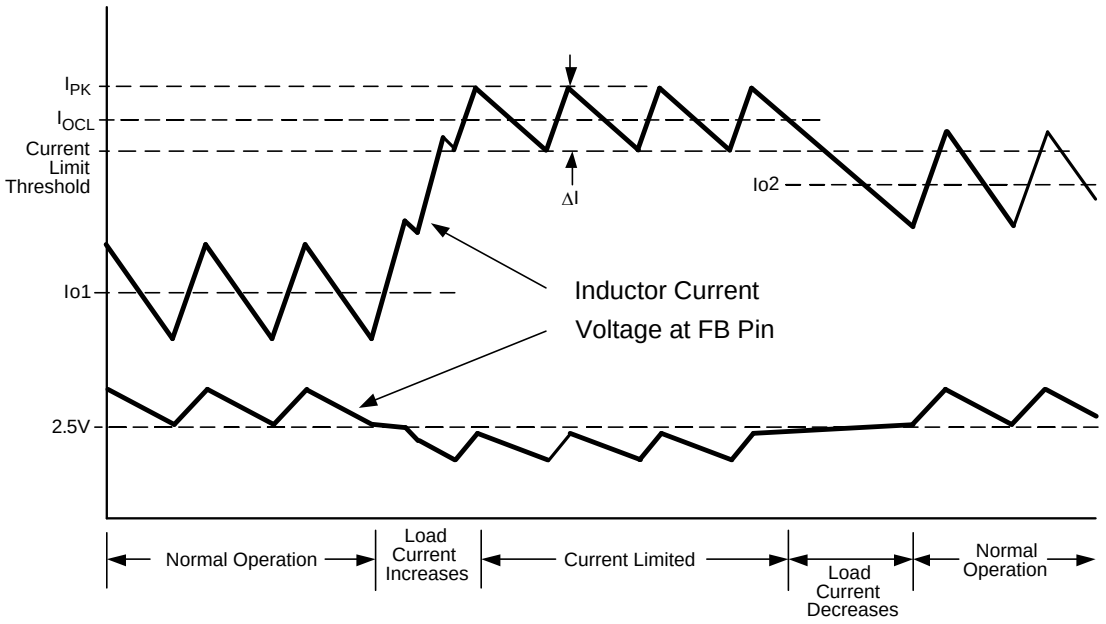


Figure 16. Inductor Current - Normal and Current Limit Operation

Startup Regulator, V_{CC}

The startup bias regulator is integral to the LM34930. The input pin (VIN) can be connected directly to the main power source, and has transient capability to 44V. The VCC output is regulated at 7.0V, and is current limited to approximately 15 mA. Upon power up, the regulator sources current into the external capacitor at VCC. When the voltage on the VCC pin reaches the under-voltage lock-out (UVLO) threshold, the buck switch is enabled and the Soft-start pin is released to allow the Soft-start capacitor to charge. The minimum input voltage is determined by the regulator's dropout voltage, the VCC UVLO falling threshold, and the switching frequency. When VCC falls below the falling threshold the V_{CC} UVLO activates to shut off the buck switch.

Over-Voltage Indicator

The nOV pin, an open drain logic output, switches low when the voltage at VIN exceeds 19V. The over-voltage indicator comparator provides 1.95V hysteresis to reject noise and ripple on the VIN pin. A pull-up resistor is required at the nOV output pin to a voltage that does not exceed 7 volts. The pull-up voltage can exceed the voltage at VIN. When nOV is low, the current into the pin must not exceed 10 mA.

Input Over-Voltage Shutdown

If the input voltage at VIN increases above 36V an internal comparator disables the buck switch, and grounds the soft-start pin. The over-voltage shutdown comparator provides 400 mV hysteresis to reject noise and ripple on the VIN pin. Normal operation resumes when the voltage at VIN is reduced below the lower threshold.

N-Channel Buck Switch and Driver

The LM34930 integrates an N-Channel buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.022 µF capacitor (C4) connected between BST and SW provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately -1V, and C4 is recharged from V_{CC} through the internal diode. The minimum off-time ensures a sufficient time each cycle to recharge the bootstrap capacitor.

Soft-Start, Remote Shutdown

The soft-start feature allows the converter to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. Upon turn-on, when V_{CC} reaches its under-voltage threshold, an internal 10 µA current source charges the external capacitor at the SS pin to 2.52V (t2 in Figure 15). The ramping voltage at SS ramps the non-inverting input of the regulation comparator, and the output voltage, in a controlled manner.

An internal switch grounds the SS pin if V_{CC} is below its under-voltage lockout threshold, or if the input voltage at VIN is above the Over-Voltage Shutdown threshold. The SS pin can be used to shutdown the LM34930 by grounding the pin as shown in Figure 17. Releasing the pin allows normal operation to resume.

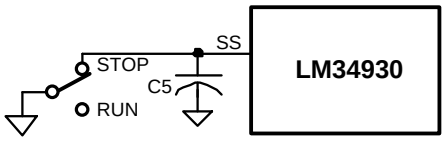


Figure 17. Shutdown Implementation

Thermal Shutdown

The LM34930 should be operated such that the junction temperature does not exceed 125°C. If the junction temperature increases above that, an internal Thermal Shutdown circuit activates typically at 155°C. In thermal shutdown the controller enters a low power non-switching state by disabling the buck switch. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature reduces below 135°C (typical hysteresis = 20°C) normal operation resumes.

APPLICATIONS INFORMATION

EXTERNAL COMPONENTS

The procedure for calculating the external components is illustrated with the following design example. Referring to the Block Diagram, the circuit is to be configured for the following specifications:

- V_{OUT} = 5V
- V_{IN} = 8V to 30V
- Minimum load current for continuous conduction mode ($I_{OUT(min)}$) = 200 mA
- Maximum load current ($I_{OUT(max)}$) = 1000 mA
- Switching Frequency (F_S) = 1.5 MHz
- Soft-start time = 5 ms

R1 and R2: These resistors set the output voltage. The ratio of the feedback resistors is calculated from:

$$R1/R2 = (V_{OUT}/2.52V) - 1 \quad (7)$$

For this example, R1/R2 = 0.98. R1 and R2 should be chosen from standard value resistors in the range of 1.0 kΩ – 10 kΩ which satisfy the above ratio. For this example, 2.32 kΩ is chosen for R1 and 2.37 kΩ is chosen for R2.

R_T: This resistor sets the on-time, and (by default) the switching frequency. First check that the desired frequency does not require an on-time or off-time shorter than the minimum allowed (90 ns each). The minimum on-time occurs at the maximum V_{IN}:

$$t_{ON(min)} = \frac{V_{OUT}}{V_{IN(max)} \times F_S} = \frac{5V}{30V \times 1.5\ MHz} = 111\ ns \quad (8)$$

The minimum off-time occurs at the minimum V_{IN}. For this example

$$t_{OFF(min)} = \frac{V_{IN(min)} - V_{OUT}}{V_{IN(min)} \times F_S} = \frac{8V - 5V}{8V \times 1.5\ MHz} = 250\ ns \quad (9)$$

This off-time is acceptable since it is significantly greater than the 90 ns minimum off-time. The R_T resistor is calculated from Equation 6 using the minimum input voltage:

$$R_T = \left[\left(\frac{5V}{8V \times 1.5\ MHz} - 65\ ns\right) \times \frac{(8V - 0.8V)}{4.15 \times 10^{-11}}\right] - 0.5\ k\Omega = 60.5\ k\Omega \quad (10)$$

A standard value 60.4 kΩ resistor is selected, resulting in a nominal frequency of 1.50 MHz. The minimum on-time calculates to 152 ns at Vin = 30V, which is acceptably longer than the minimum allowed 90 ns. The maximum on-time calculates to 416 ns at Vin = 8V.

L1: The main parameter controlled by the inductor is the inductor current ripple amplitude (I_{OR}). The minimum load current is used to determine the maximum allowable ripple in order to maintain continuous conduction mode (the lower peak does not reach 0 mA). This is not a requirement of the LM34930, but serves as a guideline for selecting L1. For this example, the maximum ripple current should be less than:

$$I_{OR(MAX)} = 2 \times I_{OUT(min)} = 400\ mAp\text{-}p \quad (11)$$

For applications where the minimum load current is zero, a good starting point for allowable ripple is 20% of the maximum load current. In this case substitute 20% of $I_{OUT(max)}$ for $I_{OUT(min)}$ in Equation 11. The ripple amplitude calculated in Equation 11 is then used in the following equation:

$$L1_{(min)} = \frac{t_{on(min)} \times (V_{IN(max)} - V_{OUT})}{I_{OR(max)}} = 9.5\ \mu H \quad (12)$$

A standard value 10 µH inductor is chosen. The maximum ripple amplitude, which occurs at maximum V_{IN}, calculates to 379 mAp-p, and the peak current is 1190 mA at maximum load current. Ensure the selected inductor is rated for this peak current.

C2, R3 and C6: C2 should typically be no smaller than 3.3 µF, although that is dependent on the frequency and the desired output characteristics. C2 should be a low ESR good quality ceramic capacitor. Experimentation is usually necessary to determine the minimum value for C2, as the nature of the load may require a larger value. A load which creates significant transients requires a larger value for C2 than a non-varying load. Ripple voltage is created at V_{OUT} as the inductor's ripple current passes through R3 into C2. That ripple voltage is AC coupled directly to the FB pin by C6 without the attenuation of R1 and R2, allowing the minimum ripple at V_{OUT} to be set at 25 mVp-p. The minimum inductor ripple current occurs at minimum VIN, and is calculated by re-arranging Equation 12 to the following:

$$I_{OR(min)} = \frac{t_{ON(max)} \times (V_{IN(min)} - V_{OUT})}{L1} = 125\ mAp\text{-}p \quad (13)$$

The minimum value for R3 is then equal to 25 mV/125 mA = 0.2Ω. The next larger standard value resistor should be used for R3 to allow for tolerances. The minimum value for C6 is equal to:

$$C6 = \frac{3 \times t_{ON\ (max)}}{(R1//R2)} = 1064\ pF \quad (14)$$

The next larger standard value capacitor should be used for C6.

C1 and C7: The purpose of C1 is to supply most of the switch current during the on-time, and limit the voltage ripple at V_{IN}, since it is assumed the voltage source feeding V_{IN} has some amount of source impedance. At maximum load current, when the buck switch turns on, the current into V_{IN} suddenly increases to the lower peak of the inductor's ripple current, then ramps up to the upper peak, then drops to zero at turn-off. The average current during the on-time is the average load current. For a worst case calculation, C1 must supply this average load current during the maximum on-time, without letting the voltage at the VIN pin drop below a minimum operating level of 7.5V. The minimum value for C1 is calculated from:

$$C1 = \frac{I_{OUT\ (max)} \times t_{ON}}{\Delta V} = 0.83\ \mu F \quad (15)$$

where t_{ON} is the maximum on-time, and ΔV is the allowable ripple voltage at V_{IN} (0.5V at V_{IN} = 8V). The purpose of C7 is to minimize transients and ringing due to long lead inductance leading to the VIN pin. A low ESR 0.1 µF ceramic chip capacitor is recommended, and C7 must be located close to the VIN and GND pins.

C3: The capacitor at the VCC pin provides noise filtering and stability for the V_{CC} regulator. C3 should be no smaller than 0.1 µF, and should be a good quality, low ESR ceramic capacitor. The value of C3, and the V_{CC} current limit, determine a portion of the turn-on-time (t1 in Figure 15).

C4: The recommended value for C4 is 0.022 µF. A high quality ceramic capacitor with low ESR is recommended as C4 supplies a surge current to charge the buck switch gate at each turn-on. A low ESR also helps ensure a complete recharge during each off-time.

C5: The capacitor at the SS pin determines the soft-start time, i.e. the time for the output voltage to reach its final value (t2 in Figure 15). For soft-start time of 5 ms, the capacitor value is determined from the following:

$$C5 = \frac{5\ ms \times 10\ \mu A}{2.52V} = 0.02\ \mu F \quad (16)$$

D1: A Schottky diode is recommended. Ultra-fast recovery diodes are not recommended as the high speed transitions at the SW pin may affect the regulator's operation due to the diode's reverse recovery transients. The diode must be rated for the maximum input voltage, the maximum load current, and the peak current which occurs when the current limit and maximum ripple current are reached simultaneously. The diode's average power dissipation is calculated from:

$$P_{D1} = V_F \times I_{OUT} \times (1\text{-}D) \quad (17)$$

where V_F is the diode's forward voltage drop, and D is the on-time duty cycle.

FINAL CIRCUIT

The final circuit is shown in Figure 18, and its performance is shown in Figure 19 and Figure 20. The current limit measured approximately 1.28A at Vin = 8V, and 1.18A at Vin = 30V. The output voltage ripple amplitude measured 32 mVp-p at Vin = 8V, and 87 mVp-p at Vin = 30V.

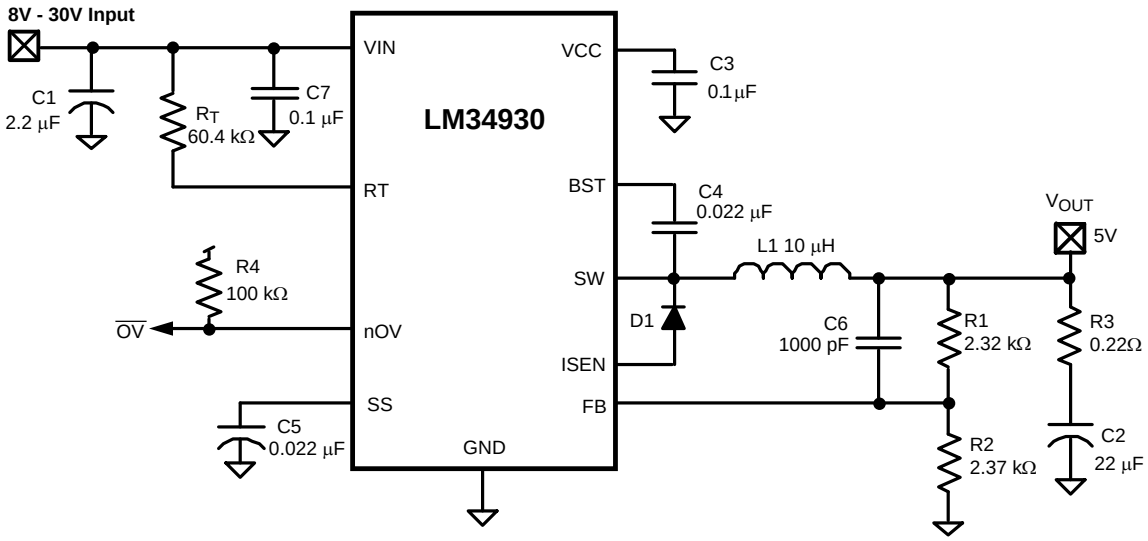


Figure 18. Example Circuit

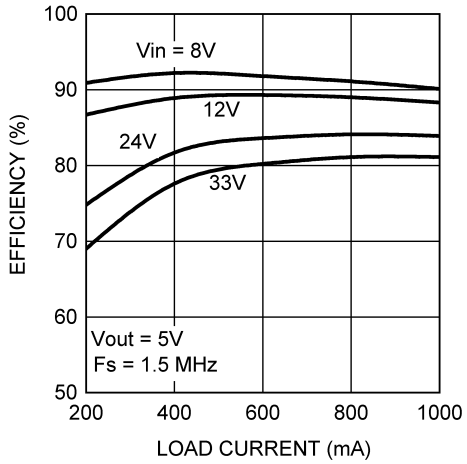


Figure 19. Efficiency vs. Load Current and V_{IN} (Circuit of Figure 18)

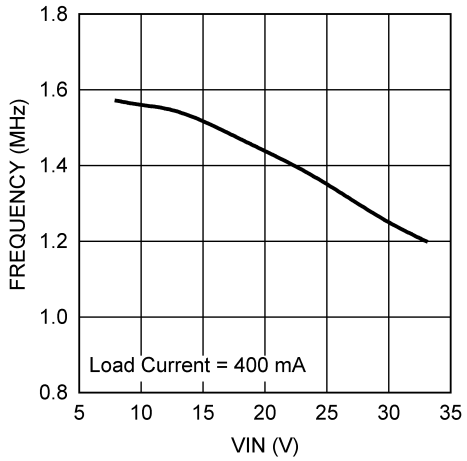


Figure 20. Frequency vs. V_{IN} (Circuit of Figure 18)

ALTERNATE OUTPUT RIPPLE CONFIGURATIONS

For applications which require lower levels of ripple at V_{OUT}, or for those which can accept higher levels of ripple while using one less capacitor, the following two alternatives are available.

a) Minimum ripple configuration: If the application requires a lower value of ripple at V_{OUT} (<25 mVp-p), the circuit of Figure 21 can be used. R3 is removed, and the resulting output ripple voltage is determined by the inductor's ripple current and the characteristics of C2 (value and ESR). RA and CA are chosen to generate a sawtooth waveform at their junction, and that voltage is AC-coupled to the FB pin via CB. To determine the values for RA, CA and CB, use the following procedure:

- Calculate the voltage

$$V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN(min)}))) \quad (18)$$

where V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 0.6V to 1V). V_A is the DC voltage at the RA/CA junction, and is used in the next equation.

Calculate the product

$$RA \times CA = \frac{(V_{IN(min)} - V_A) \times t_{ON}}{\Delta V} \quad (19)$$

where t_{ON} is the maximum on-time (at minimum input voltage), and ΔV is the desired ripple amplitude at the RA/CA junction (typically 40-50 mV). RA and CA are then chosen from standard value components to satisfy the above product. Typically CA is 3000 pF to 10,000 pF, and RA is 10 kΩ to 300 kΩ. CB is then chosen to be large in comparison to CA, typically 0.1 µF. The values of R1 and R2 should each be towards the upper end of the 1 kΩ to 10 kΩ range.

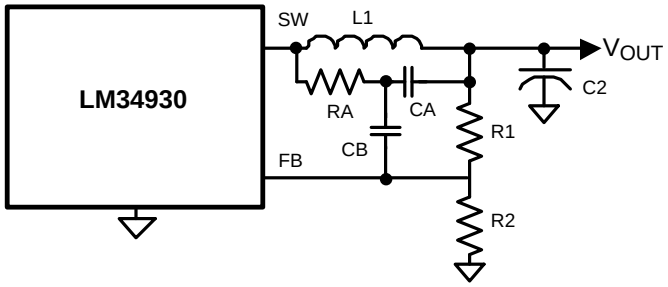


Figure 21. Minimum Output Ripple Using Ripple Injection

b) Slightly higher ripple – In the basic configuration in Figure 22 C6 is removed and R3 is increased since the ripple amplitude from V_{OUT} to FB is attenuated by R1 and R2. The ripple at V_{OUT} is created by the inductor's ripple current passing through R3, and coupled to the FB pin through the feedback resistors (R1, R2). Since the LM34930 requires a minimum of 25 mVp-p ripple at the FB pin, the ripple required at V_{OUT} is 25 mV divided by the attenuation of the feedback resistors. The minimum ripple current ($I_{OR(min)}$) is calculated by re-arranging Equation 12 using $t_{ON(max)}$ and $V_{IN(min)}$. The minimum value for R3 is calculated from:

$$R3_{(min)} = \frac{25\ mV \times (R1 + R2)}{R2 \times I_{OR\ (min)}} \tag{20}$$

The next larger standard value resistor should be used for R3.

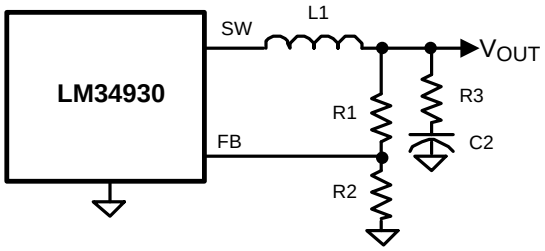


Figure 22. Basic Ripple Configuration

c) Alternate minimum ripple configuration: The low ripple alternative circuit in Figure 23 is the same as that in Figure 22, except the output voltage is taken from the junction of R3 and C2. The ripple at V_{OUT} no longer includes the ripple across R3. It is determined by the inductor's ripple current and the characteristics of C2. However, R3 slightly degrades the load regulation by effectively increasing the output resistance of the regulator. This circuit may be suitable if the load current is fairly constant. R3 is calculated as described in Alternate b above, and must be rated to carry the maximum load current.

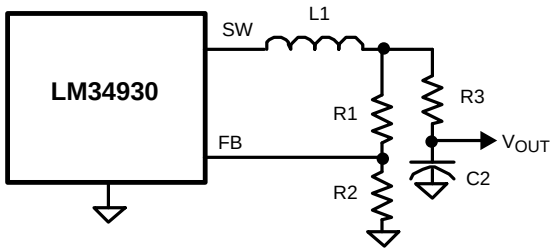


Figure 23. Alternate Minimum Output Ripple Configuration

Minimum Load Current

The LM34930 requires a minimum load current of 1 mA. If the load current falls below that level, the bootstrap capacitor (C4) may discharge during the long off-time, and the circuit will either shutdown, or cycle on and off at a low frequency. If the load current is expected to drop below 1 mA in the application, R1 and R2 should be chosen with low enough values that they provide additional loading to maintain the minimum load requirement.

PC BOARD LAYOUT

Refer to application note AN-1112 (literature number SNVA009) for PC board guidelines for the DSBGA package.

The LM34930 regulation, over-voltage, and current limit comparators are very fast, and respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible, and all of the components must be as close as possible to their associated pins. The two major current loops conduct currents which switch very fast, and therefore those loops should be as small as possible to minimize conducted and radiated EMI. The first loop is formed by C1, through the VIN to SW pins, L1, C2, and back to C1.The second current loop is formed by D1, L1, C2 and the GND and ISEN pins. The ground connection from the LM34930's GND pin to C1 should be as short and direct as possible.

The power dissipation within the LM34930 can be approximated by determining the total conversion loss (P_{IN} - P_{OUT}), and then subtracting the power losses in the free-wheeling diode and the inductor. The power loss in the diode is approximately:

$$P_{D1} = Iout \times V_F \times (1-D) \quad (21)$$

where Iout is the load current, V_F is the diode's forward voltage drop, and D is the on-time duty cycle. The power loss in the inductor is approximately:

$$P_{L1} = Iout^2 \times R_{LDC} \times 1.1 \quad (22)$$

where R_{LDC} is the inductor's DC resistance, and the 1.1 factor is an approximation for the AC losses. If it is expected that the internal dissipation of the LM34930 will produce excessive junction temperatures during normal operation, good use of the PC board's ground plane can help to dissipate heat. Additionally the use of wide PC board traces, where possible, can help conduct heat away from the IC pins. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM34930TL/NOPB	ACTIVE	DSBGA	YZR	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	STCB	Samples
LM34930TLX/NOPB	ACTIVE	DSBGA	YZR	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	STCB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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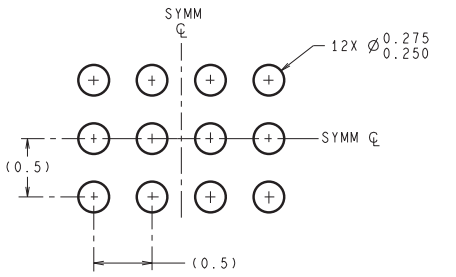
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

YZR0012



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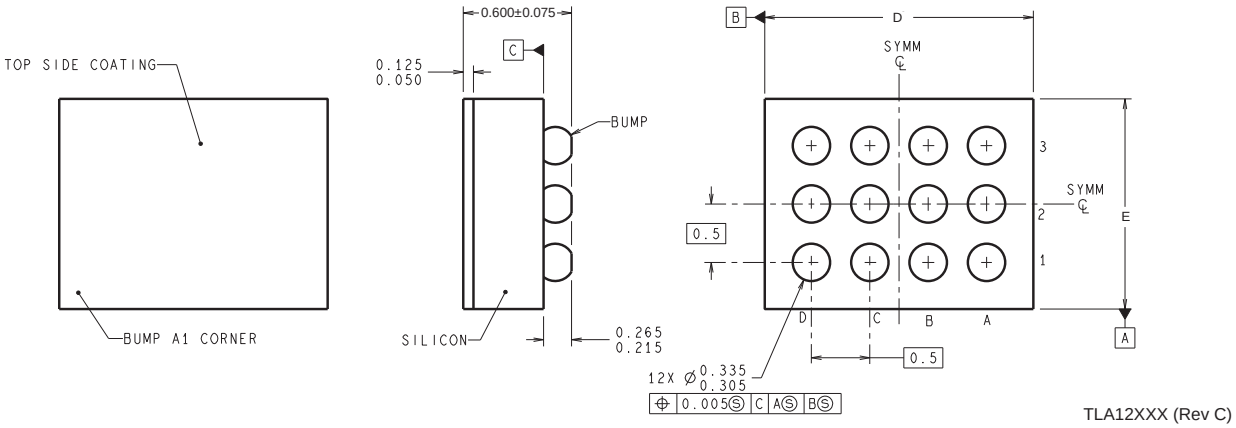

TLA12XXX (Rev C)

D: Max = 2.119 mm, Min =2.018 mm

E: Max = 1.811 mm, Min = 1.71 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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