LM4817 Boomer® Audio Power Amplifier Series 1W Stereo Audio Amplifier Plus Adjustable Output Limiter Plus Adjustable LDO

Check for Samples: LM4817

FEATURES

- **Stereo BTL Amplifier**
- **Adjustable Output Voltage Magnitude Limiter**
- **Adjustable LDO Regulator**
- **"Click and Pop" Suppression Circuitry**
- **LDO is Stable with Small-Value Ceramic Output Capacitors**
- **Unity-Gain Stable Audio Amplifiers**
- **LDO has Over-Current Protection**
- **Thermal Shutdown Protection Circuitry**
- **TSSOP (PWP) Package**

APPLICATIONS

- **Multimedia Monitors**
- **Portable and Desktop Computers**
- **Portable Televisions**

KEY SPECIFICATIONS

- **P_O (BTL): V_{DD} = 5V, THD+N ≤ 1%, R_L = 8Ω: 1.0 W (typ)**
- **Power supply range (amplifier): 3.0 to 5.5 V**
- **Power supply range (LDO): 2.5 to 6.0 V**
- **Shutdown current: 0.07 µA (typ)**
- **LDO output current: 300 mA (min)**
- **LDO dropout voltage (I_{OUT} = 300mA): 120 mV (typ)**
- **LDO quiescent supply current: 90 µA (typ)**
- **LDO shutdown supply current: 1 nA (typ)**
- **LDO PSRR: 60 dB**
- **LDO turn-on time: 120 ms (typ)**
- **LDO ouput noise-voltage: 37 µV_{RMS} (typ)**

DESCRIPTION

The LM4817 combines a bridge-connected (BTL) stereo audio power amplifier with a low dropout voltage regulator (LDO). The audio amplifier delivers 1.0W to a 8Ω load with a less than 1.0% THD+N while operating on a 5V power supply. With V_{LIM} set to 1.0V, the amplifier outputs are clamped to 6V_{p-p}, ±800mV.

With the LM4817's adjustable low-dropout (LDO) CMOS linear regulator delivers an output current of up to 300mA, has shutdown mode (1nA, typ) low quiescent current (90µA, typ) and LDO voltage (120mV, typ). The regulator is stable with small ceramic capacitive load (2.2µF, typ). The regulator includes regulation fault detection, a bandgap voltage reference, and constant current limiting. It is designed for low power, low current applications that can take advantage of its 300mA output current capability.

The LM4817 features an externally controlled micropower shutdown mode and thermal shutdown protection. It also utilizes circuitry that reduces "clicks and pops" during device turn-on and return from shutdown.

Boomer audio power amplifiers are designed specifically to use few external components and provide high quality output power in a surface mount package.

Connection Diagram

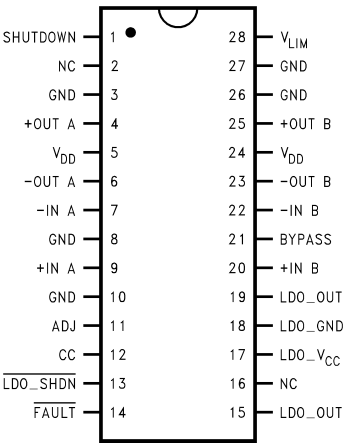
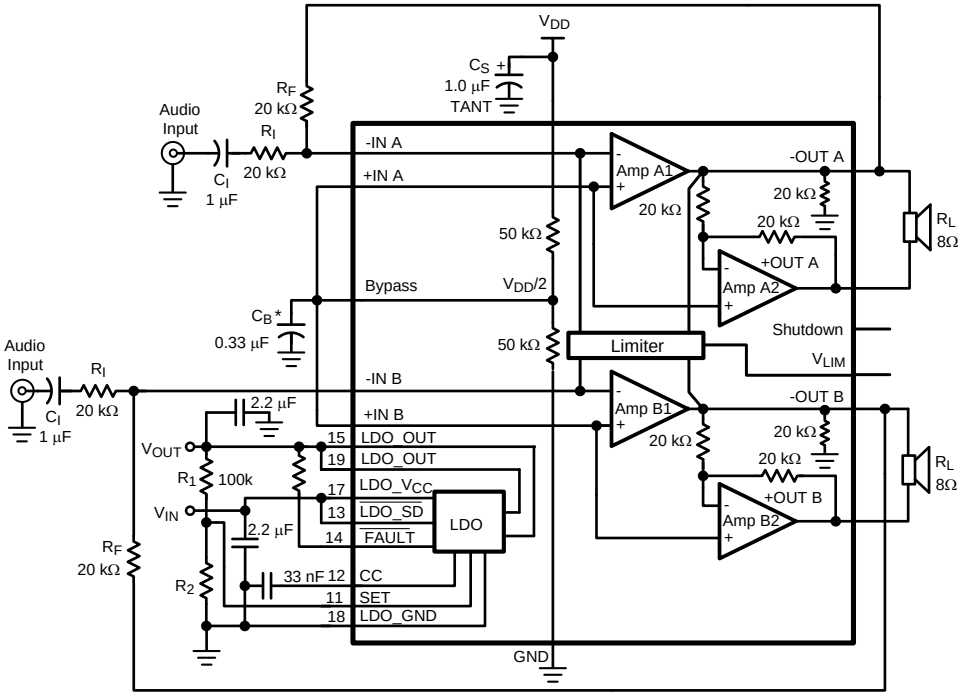


Figure 1. Top View
See Package Number PWP0028A for TSSOP

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings Stereo Amplifier(1)(2)(3)

Amplifier Supply Voltage (pins 5, 24)			6.0V
LDO-V_{CC}, LDO-OUT, LDO-SHDN, ADJ, CC, FAULT (pins 11-15, 17,19)			−0.3V to 6.5V
Fault Sink Current			20mA
Storage Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} +0.3V
Power Dissipation(4)			Internally limited
ESD Susceptibility(5)			2000V
ESD Susceptibility(6)			200V
Junction Temperature			150°C
Solder Information	Small Outline Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
Thermal Resistance		θ_{JC} (typ)—PWP0028A	20°C/W
		θ_{JA} (typ)—PWP0028A(4)	41°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A and must be derated at elevated temperatures. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4817, T_{JMAX} = 150°C. The $\theta_{JA}$for the LM4817 in the 28-pin PWP0028A package, when board mounted and its DAP is soldered to a 2in^2 copper heatsink plane, is 41°C/W.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) Machine model, 220pF–240pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage	Pins 5, 24	3.0V ≤ V_{DD} ≤ 5.5V
	Pin 17	2.5V ≤ V_{CC} ≤ 6.0V

Stereo Amplifier Electrical Characteristics for Entire IC[1][2]

The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4817		Units (Limits)
			Typical[3]	Limit[4]	
V_{DD}	Supply Voltage			3	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A[5]	8	15 5	mA (max) mA (min)
I_{SD}	Shutdown Current	V_{DD} applied to the SHUTDOWN pin	0.07	2	µA (min)
V_{IH}	Shutdown Logic High Input Threshold Voltage			2.7	V (min)
V_{IL}	Shutdown Logic Low Input Threshold Voltage			1.8	V (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	50	mV (max)
P_O	Output Power[6]	THD+N = 1%, f = 1kHz, R_L = 8Ω	1.1	1.0	W (min)
		THD+N = 10%, f = 1kHz, R_L = 8Ω	1.5		W
THD+N	Total Harmonic Distortion+Noise	20Hz ≤ f ≤ 20kHz, A_{VD} = 2 R_L = 8Ω, P_O = 1W	0.13		%
V_{LIM}	Limiter Clamp Voltage	V_{LIM} = 1.0V, R_L = ∞, V_{IN} = 4V_{P-P} $V_{O\ P-P}$ = (V_{OUT+} - V_{OUT-})	6.0	5.2 6.8	V_{P-P} (min) V_{P-P} (max)
PSRR	Power Supply Rejection Ratio	V_{DD} = 5V, V_{RIPPLE} = 200mV_{RMS}, R_L = 8Ω, C_B = 1.0µ, f_{IN} = 1kHz Inputs Floating Inputs terminated with 10Ω	 67 45		 dB dB
X_{TALK}	Channel Separation	f = 1kHz, C_B = 1.0µF	90		dB
SNR	Signal To Noise Ratio	V_{DD} = 5V, P_O = 1W, R_L = 8Ω	98		dB

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
(6) Output power is measured at the device terminals.

LDO Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $V_{IN} = V_O + 0.5V$[1], $V_{\overline{SHDN}} = V_{IN}$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25°C$. **Boldface** limits apply for the operating temperature extremes: −40°C and 85°C.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{IN}	Input Voltage		**2.5**		**6.0**	V
ΔV_O	Output Voltage Tolerance	100µA ≤ I_{OUT} ≤ 300mA $V_{IN} = V_O + 0.5V$[2] SET = OUT	-2.4		+2.4	% of V_{OUT} (NOM)
			-3		**+3**	
V_O	Output Adjust Range		**1.25**		**6**	V
I_O	Maximum Output Current	Average DC Current Rating	**300**			mA
I_{LIMIT}	Output Current Limit		**330**	770		mA
I_Q	Supply Current	I_{OUT} = 0mA		90	**270**	µA
		I_{OUT} = 300mA		225		
	Shutdown Supply Current	V_O = 0V, $\overline{SHDN}$ = GND		0.001	1	µA
V_{DO}	Dropout Voltage[1][4]	I_{OUT} = 1mA		0.4		mV
		I_{OUT} = 200mA		80	**220**	
		I_{OUT} = 300mA		120		
ΔV_O	Line Regulation	I_{OUT} = 1mA, $(V_O + 0.5V) \le V_I \le 6V$[1]	**-0.1**	0.01	**0.1**	%/V
	Load Regulation	100µA ≤ I_{OUT} ≤ 300mA		0.002		%/mA
e_n	Output Voltage Noise	I_{OUT} = 10mA, 10Hz ≤ f ≤ 100kHz		37		μV_{RMS}
	Output Voltage Noise Density	10Hz ≤ f ≤ 100kHz, C_{OUT} = 10µF		190		$nV/\sqrt{Hz}$
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Threshold	V_{IH}, $(V_O + 0.5V) \le V_I \le 6V$[1]	**2**			V
		V_{IL}, $(V_O + 0.5V) \le V_I \le 6V$			**0.4**	
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Bias Current	$\overline{SHDN}$ = GND or IN		0.1	100	nA
I_{SET}	SET Input Leakage	SET = 1.3V		0.1	2.5	nA
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Detection Voltage	$V_O \ge 2.5V$, I_{OUT} = 200mA[5]		120	**280**	mV
	$\overline{FAULT}$ Output Low Voltage	I_{SINK} = 2mA		0.115	**0.25**	V
$I_{\overline{FAULT}}$	$\overline{FAULT}$ Off-Leakage Current	$\overline{FAULT}$ = 3.6V, $\overline{SHDN}$ = 0V		0.1	100	nA
T_{SD}	Thermal Shutdown Temperature			160		°C
	Thermal Shutdown Hysteresis			10		
T_{ON}	Start-Up Time	C_{OUT} = 10µF, V_O at 90% of Final Value		120		µs

(1) Condition does not apply to input voltages below 2.5V since this is the minimum input operating voltage.
(2) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Dropout voltage is measured by reducing V_{IN} until V_O drops 100mV from its nominal value at $V_{IN} - V_O = 0.5V$. Dropout Voltage does not apply to the 1.8 version.
(5) The $\overline{FAULT}$ detection voltage is specified for the input to output voltage differential at which the $\overline{FAULT}$ pin goes active low.

Stereo Amplifier Typical Performance Characteristics

THD+N vs Frequency

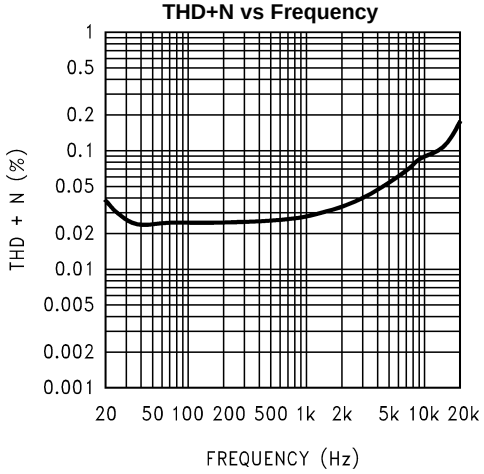


Figure 2. V_{DD} = 3V, R_L = 8Ω, P_{OUT} = 150mW

THD+N vs Frequency

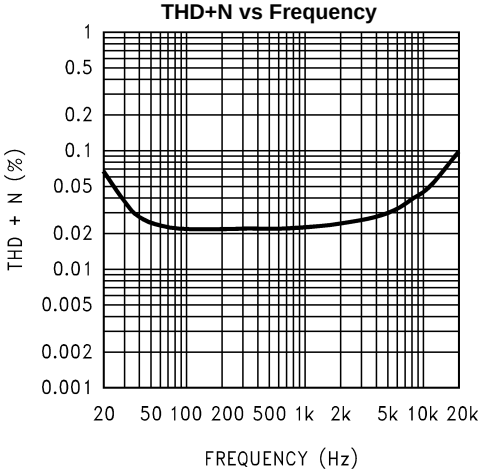


Figure 3. V_{DD} = 5V, R_L = 8Ω, P_{OUT} = 150mW

THD+N vs Frequency

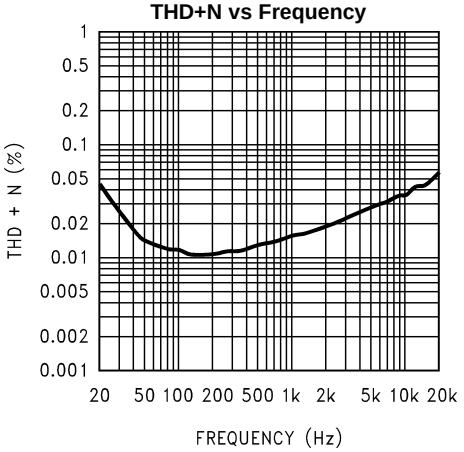


Figure 4. V_{DD} = 5.5V, R_L = 8Ω, P_{OUT} = 150mW

THD+N vs Output Power

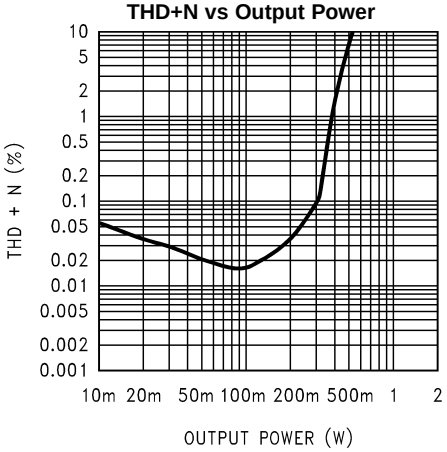


Figure 5. V_{DD} = 3V, R_L = 8Ω, f_{IN} = 1kHz

THD+N vs Output Power

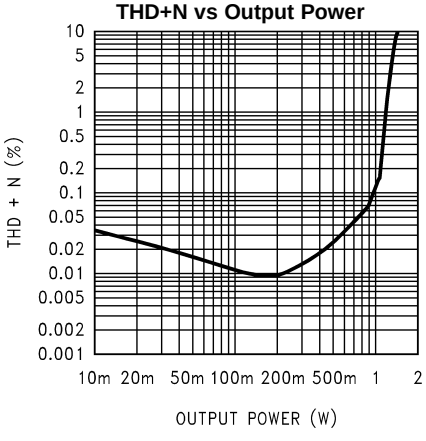


Figure 6. V_{DD} = 5V, R_L = 8Ω, f_{IN} = 1kHz

THD+N vs Output Power

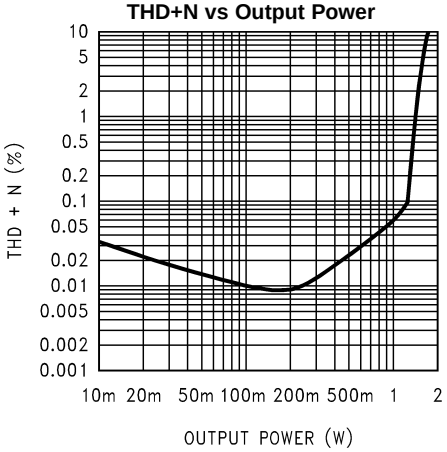


Figure 7. V_{DD} = 5.5V, R_L = 8Ω, f_{IN} = 1kHz

Stereo Amplifier Typical Performance Characteristics (continued)

Output Power vs Supply Voltage

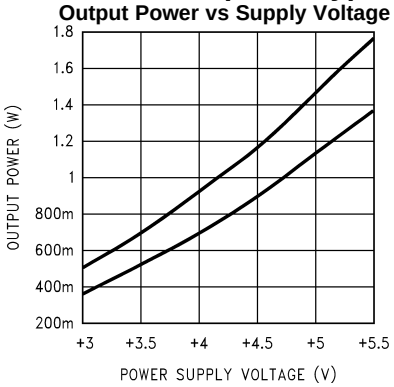


Figure 8. R_L = 8Ω, f_{IN} = 1kHz, at (from top to bottom at 4.5V): THD+N = 10%, THD+N = 1%

Output Power vs Load Resistance

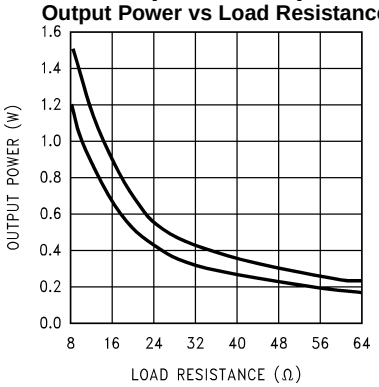


Figure 9. R_L = 8Ω, f_{IN} = 1kHz, at (from top to bottom at 24Ω): THD+N = 10%, THD+N = 1%

Power Dissipation vs Load Dissipation

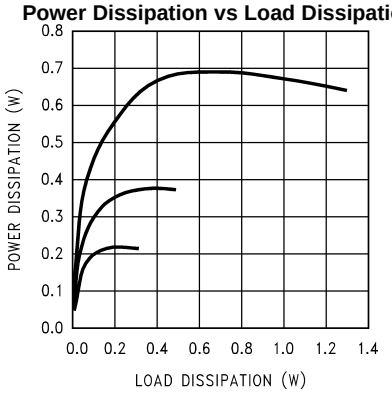


Figure 10. V_{DD} = 5V, f_{IN} = 1kHz, at (from top to bottom at 0.2W): R_L = 8Ω, R_L = 16Ω, R_L = 32Ω

Dropout Voltage vs Supply Voltage

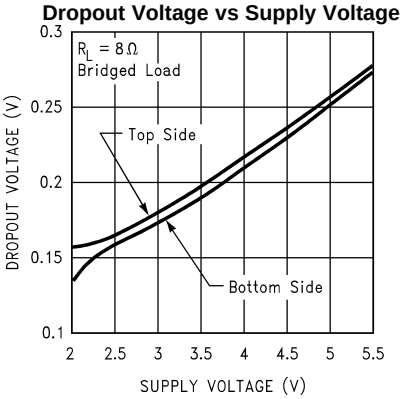


Figure 11. Dropout Voltage vs Supply Voltage

Power Derating Curve

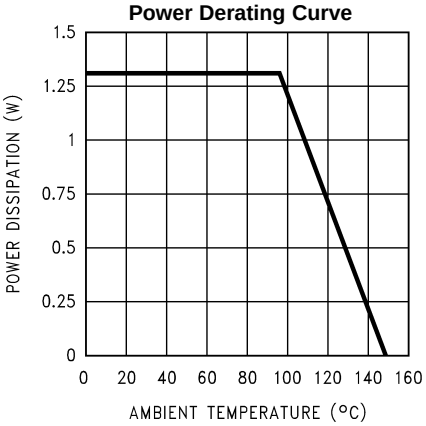


Figure 12. V_{DD} = 5V, R_L = 8Ω, f_{IN} = 1kHz 2in^2 copper heatsink area

Cross Talk

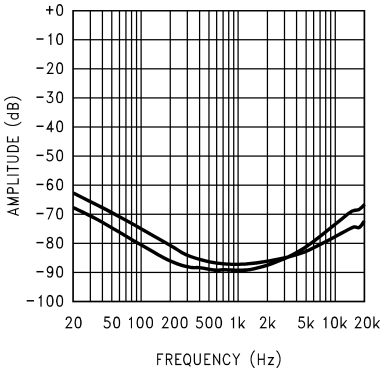


Figure 13. V_{DD} = 3V, R_L = 8Ω, P_{OUT}= 150mW, at (from top to bottom at 2kHz): -IN A driven, V_{OUTB} measured; -IN B driven, V_{OUTA} measured

Stereo Amplifier Typical Performance Characteristics (continued)

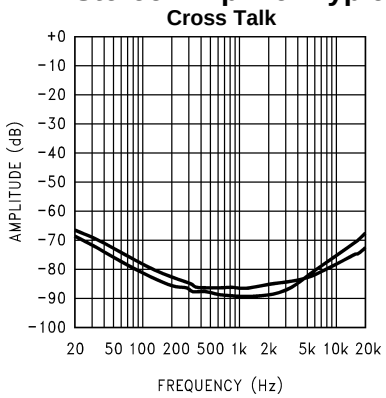


Figure 14. V_{DD} = 5V, R_L = 8Ω, P_{OUT}= 150mW, at (from top to bottom at 2kHz):
-IN A driven, V_{OUTB} measured;
-IN B driven, V_{OUTA} measured

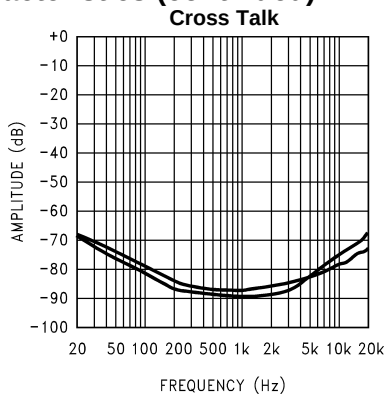


Figure 15. V_{DD} = 5.5V, R_L = 8Ω, P_{OUT}= 150mW, at (from top to bottom at 2kHz):
-IN A driven, V_{OUTB} measured;
-IN B driven, V_{OUTA} measured

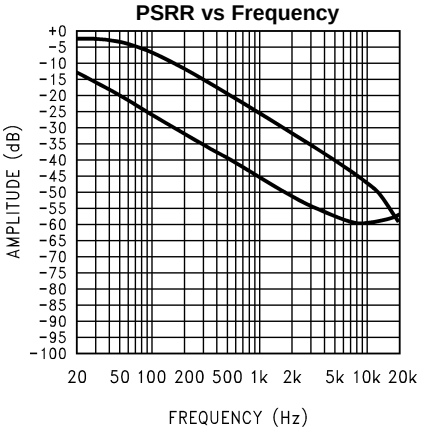


Figure 16. V_{DD} = 3V, R_L = 8Ω, R_{SOURCE}= 10Ω,
V_{RIPPLE} = 200mVP-P, at (from top to bottom at 500Hz):
C_{BYPASS} = 0.1µF, C_{BYPASS} = 1.0µF

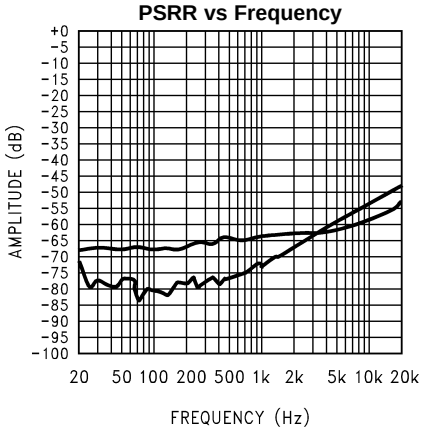


Figure 17. V_{DD} = 3V, R_L = 8Ω, R_{SOURCE}= ∞,
V_{RIPPLE} = 200mV_{P-P}, at (from top to bottom at 500Hz):
C_{BYPASS} = 0.1µF, C_{BYPASS} = 1.0µF

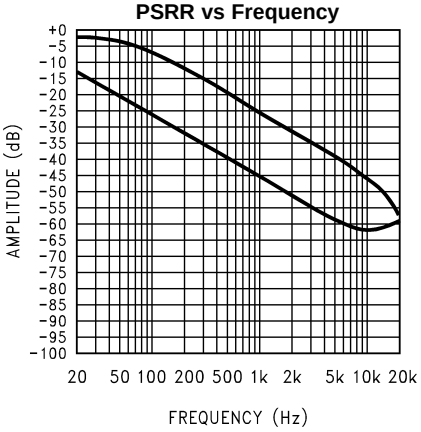


Figure 18. V_{DD} = 5V, R_L = 8Ω, R_{SOURCE}= 10Ω,
V_{RIPPLE} = 200mV_{P-P}, at (from top to bottom at 500Hz):
C_{BYPASS} = 0.1µF, C_{BYPASS} = 1.0µF

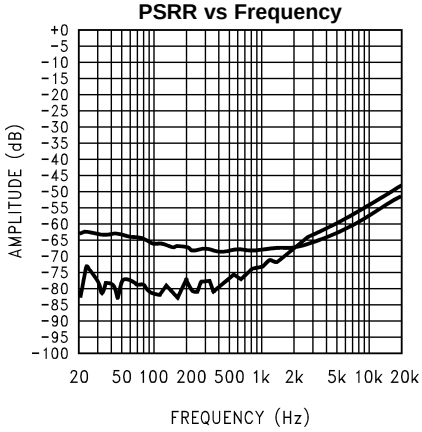


Figure 19. V_{DD} = 5V, R_L = 8Ω, R_{SOURCE}= ∞,
V_{RIPPLE} = 200mV_{P-P}, at (from top to bottom at 500Hz):
C_{BYPASS} = 0.1µF, C_{BYPASS} = 1.0µF

Stereo Amplifier Typical Performance Characteristics (continued)

Open Loop Frequency Response

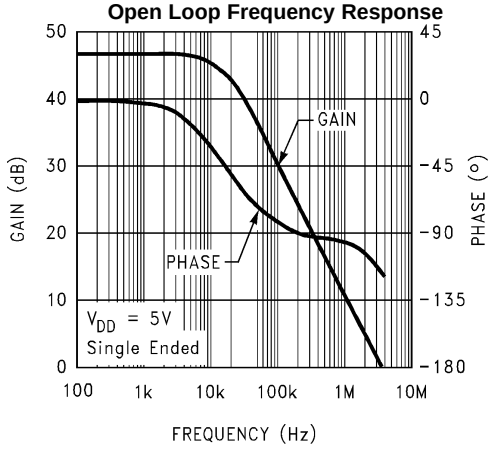


Figure 20. Open Loop Frequency Response

Power Supply Current vs Power Supply Voltage

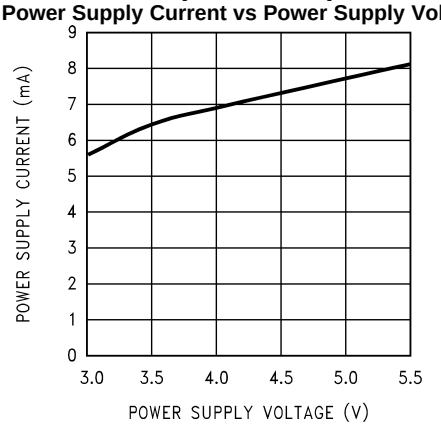


Figure 21. R_L = ∞, R_{SOURCE} = 50Ω, V_{IN} = 0V

THD+N vs Output Power

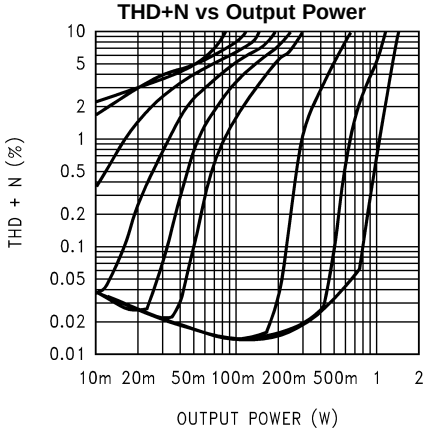


Figure 22. V_{DD} = 5V, R_L = 8Ω, f_{IN} = 1kHz, at (from left to right at 7% THD+N): V_{LIM} = 2V, 1.9V, 1.8V, 1.7V, 1.6V, 1.5V, 1.0V, 0.5V, 0V

LDO Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.5V$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25°C$, $V_{\overline{SHDN}} = V_{IN}$.

Dropout Voltage vs Load Current (For Different Output Voltages)

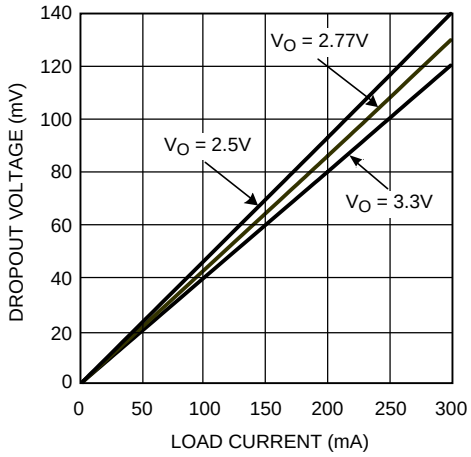


Figure 23.

Dropout Voltage vs Load Current (For Different Output Temperatures)

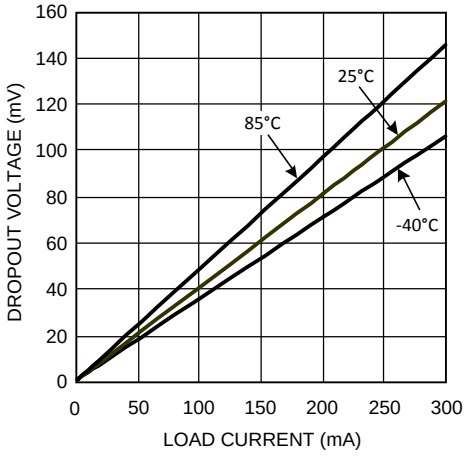


Figure 24.

$\overline{FAULT}$ Detect Threshold vs Load Current

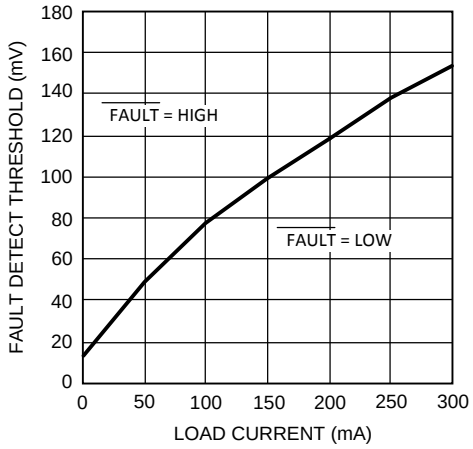


Figure 25.

Supply Current vs Input Voltage

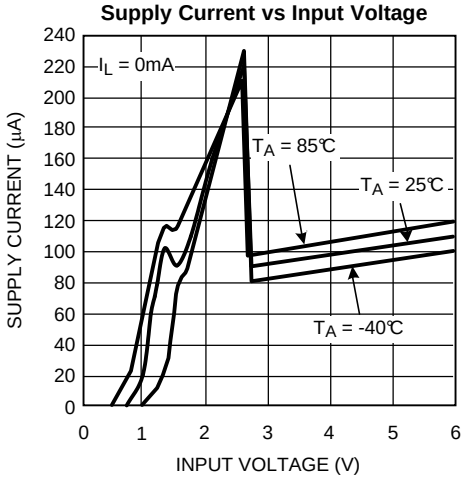


Figure 26.

Supply Current vs Load Current

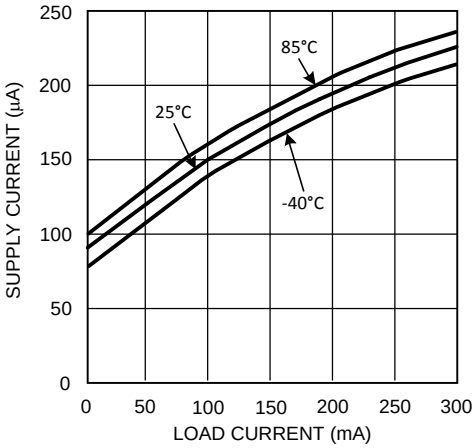


Figure 27.

Power Supply Rejection Ratio vs Frequency

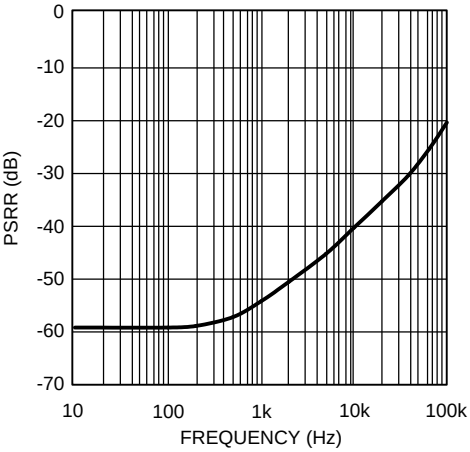


Figure 28.

LDO Typical Performance Characteristics (continued)

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.5V$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25°C$, $V_{\overline{SHDN}} = V_{IN}$.

Output Noise Spectral Density

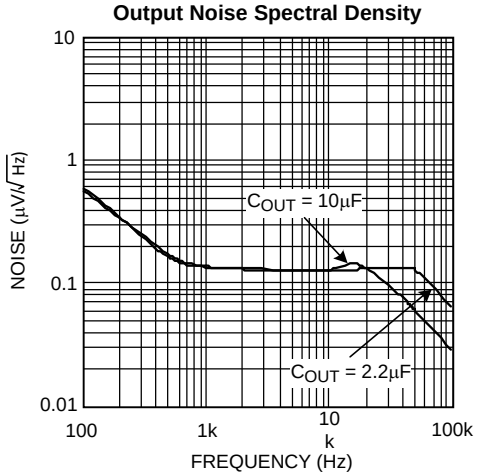


Figure 29.

Output Noise (10Hz to 100kHz)

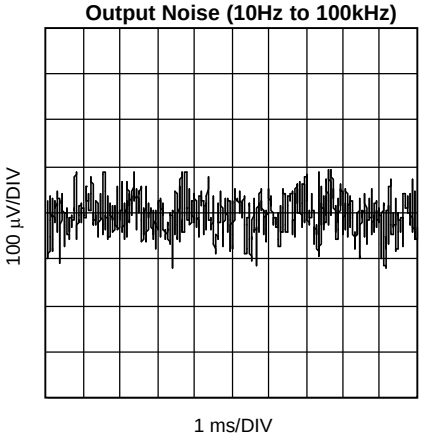


Figure 30.

Output Impedance vs Frequency

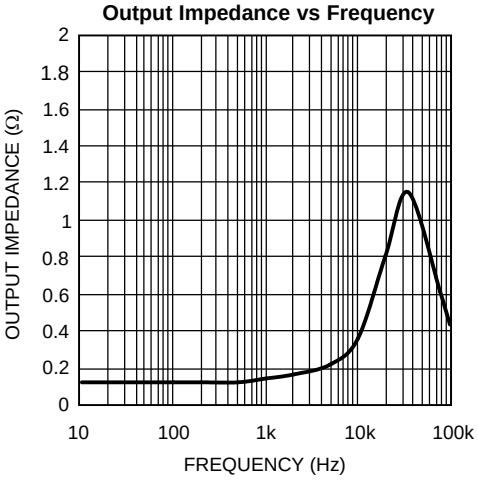


Figure 31.

Line Transient Response

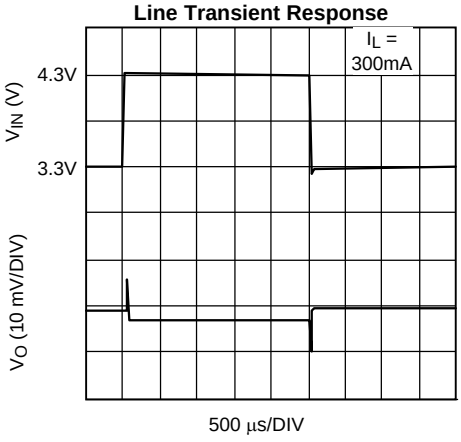


Figure 32.

Load Transient

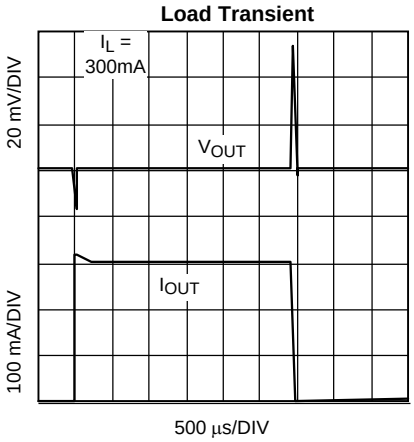


Figure 33.

Shutdown Response

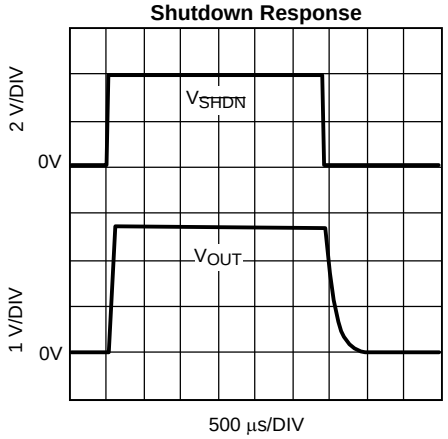


Figure 34.

LDO Typical Performance Characteristics (continued)

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.5V$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25°C$, $V_{\overline{SHDN}} = V_{IN}$.

Power-Up Response

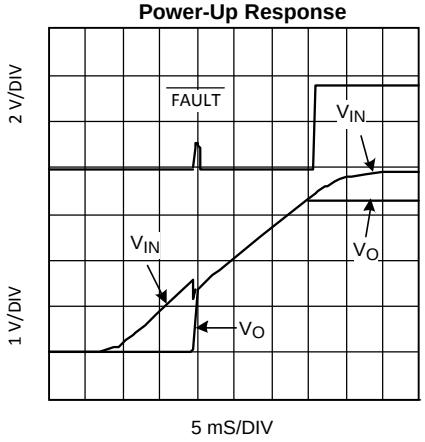


Figure 35.

Power-Down Response

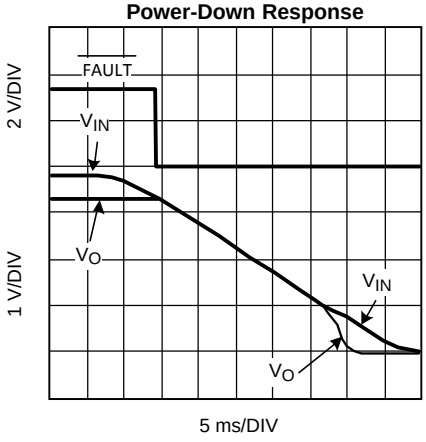


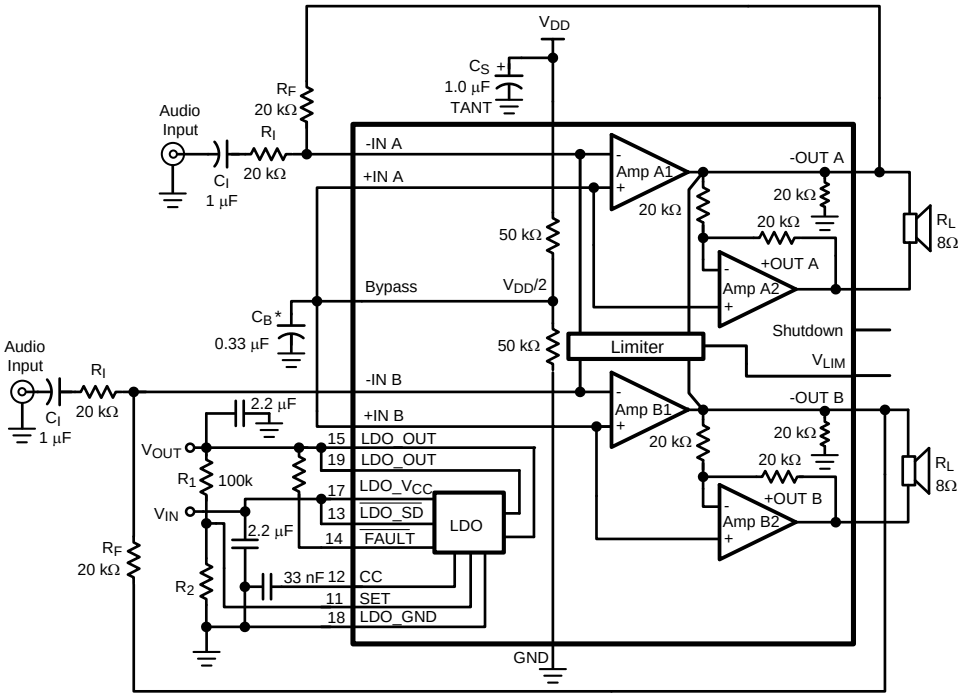
Figure 36.

Table 1. External Components Description

Components		Functional Description
1.	R_i	The Inverting input resistance, along with R_f, set the closed-loop gain. R_i, along with C_i, form a high pass filter with $f_c = 1/(2\pi R_i C_i)$.
2.	C_i	The input coupling capacitor blocks DC voltage at the amplifier's input terminals. C_i, along with R_i, create a highpass filter with $f_c = 1/(2\pi R_i C_i)$. Refer to SELECTING PROPER EXTERNAL COMPONENTS for an explanation of determining the value of C_i.
3.	R_f	The feedback resistance, along with R_i, set the closed-loop gain.
4.	C_s	The supply bypass capacitor. Refer to POWER SUPPLY BYPASSING for information about properly placing, and selecting the value of, this capacitor.
5.	C_B	The capacitor, C_B, filters the half-supply voltage present on the BYPASS pin. Refer to SELECTING PROPER EXTERNAL COMPONENTS for information concerning proper placement and selecting C_B's value.
6.	R_1	Combined with R_2, sets the LDO's output voltage according to Equation 1: $R_1 = R_2 ((V_{OUT} / 1.25V) - 1)$ (1)
7.	R_2	Combined with R_1, sets the LDO's output voltage according to Equation 2: $R_2 = (1.25V \times R_1) / (V_{OUT} - 1.25V)$ (2)

APPLICATION INFORMATION

BRIDGE CONFIGURATION EXPLANATION



A. Refer to the section SELECTING PROPER EXTERNAL COMPONENTS for a detailed discussion of C_B size.

B. Pin out shown for the WQFN package. Refer to the Connection Diagrams for the pinout of the TSSOP package.

Figure 37. Typical Audio Amplifier Application Circuit

As shown in Figure 37, the LM4817 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.) External resistors R_f and R_i set the closed-loop gain of Amp1A, whereas two internal 20kΩ resistors set Amp2A's gain at -1. The LM4817 drives a load, such as a speaker, connected between the two amplifier outputs, -OUTA and +OUTA.

Figure 37 shows that Amp1A's output serves as Amp2A's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between -OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 \times (R_f / R_i) \quad (3)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to AUDIO POWER AMPLIFIER DESIGN.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ Single-Ended} \quad (4)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4817 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (3), assuming a 5V power supply and an 8Ω load, the maximum single channel power dissipation is 0.633W or 1.27W for stereo operation.

$$P_{DMAX} = 4 \times (V_{DD})^2 / (2\pi^2 R_L) \text{ Bridge Mode} \quad (5)$$

The LM4817's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \quad (6)$$

The LM4817's T_{JMAX} = 150°C. In the PWP package soldered to a DAP pad that expands to a copper area of $2in^2$ on a PCB , the LM4817's θ_{JA} is 41°C/W. At any given ambient temperature $T_{J\A}$, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting P_{DMAX} for P_{DMAX}' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4817's maximum junction temperature.

$$T_A = T_{JMAX} - 2 \times P_{DMAX} \theta_{JA} \quad (7)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 98°C for the PWP package.

$$T_{JMAX} = P_{DMAX} \theta_{JA} + T_A \quad (8)$$

Equation (6) gives the maximum junction temperature T_{JMAX}. If the result violates the LM4817's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If twice the value given by Equation (3) exceeds the result of Equation (4), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, $_{CS}$ is the case-to-sink thermal impedance, and $\theta_{SA}$is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

OUTPUT VOLTAGE LIMITER

The LM4817's adjustable output voltage limiter can be used to set a maximum and minimum output voltage swing magnitude. The voltage applied to the V_{LIM} input (pin 28) controls the amount voltage limit magnitude.

Without the limiter's influence (V_{LIM} = 0V), the LM4817's maximum BTL output swing is nominally

$2 \times V_{DD}$

When the limiter input voltage is greater than 0V, the BTL output voltage swing is

$V_{OUT-BTL} = (2 \times V_{DD}) - (4 \times V_{LIM})$

For any given value of V_{LIM}, the actual output swing will be limited to within ±200mV.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4817's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation in the output signal. Keep the length of leads and traces that connect capacitors between the LM4817's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in SELECTING PROPER EXTERNAL COMPONENTS), system cost, and size constraints.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4817's shutdown function. Activate micro-power shutdown by applying V_{DD} to the SHUTDOWN pin. When active, the LM4817's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically $V_{DD}/2$. The low 0.7µA typical shutdown current is achieved by applying a voltage that is as near as V_{DD} as possible to the SHUTDOWN pin. A voltage thrat is less than V_{DD} may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 10kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to V_{DD} through the pull-up resistor, activating micro-power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

Table 2. Logic Level Truth Table for Shutdown Operation

SHUTDOWN	OPERATIONAL MODE
Low	Full power, stereo BTL amplifiers
High	Micro-power Shutdown

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4817's performance requires properly selecting external components. Though the LM4817 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4817 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to AUDIO POWER AMPLIFIER DESIGN for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 37). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, C_i has an affect on the LM4817's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_f. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency.

A shown in Figure 37, the input resistor (R_I) and the input capacitor, C_I produce a −3dB high pass filter cutoff frequency that is found using Equation (7).

$$f_{-3\,dB} = \frac{1}{2\pi R_{IN} C_1} \tag{9}$$

As an example when using a speaker with a low frequency limit of 150Hz, C_I, using Equation (4), is 0.063µF. The 1.0µF C_I shown in Figure 37 allows the LM4817 to drive high efficiency, full range speaker whose response extends below 30Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4817 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4817's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4817 contains circuitry to minimize turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4817's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. Although the bypass pin current cannot be modified, changing the size of C_B alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of C_B and the turn-on time. Here are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.01µF	20 ms
0.1µF	200 ms
0.22µF	440 ms
0.47µF	940 ms
1.0µF	2 Sec

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops".

NO LOAD STABILITY

The LM4817 may exhibit low level oscillation when the load resistance is greater than 10kΩ. This oscillation only occurs as the output signal swings near the supply voltages. Prevent this oscillation by connecting a 5kΩ between the output pins and ground.

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	$1W_{RMS}$
Load Impedance:	8Ω
Input Level:	$1V_{RMS}$
Input Impedance:	20kΩ
Bandwidth:	100Hz−20 kHz ± 0.25 dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in Stereo Amplifier Typical Performance Characteristics. Another way, using Equation (4), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in Stereo Amplifier Typical Performance Characteristics, must be added to the result obtained by Equation (8). The result in Equation (9).

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (10)$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (11)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4817 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in Power Dissipation.

After satisfying the LM4817's power dissipation requirements, the minimum differential gain is found using Equation (10).

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (12)$$

Thus, a minimum gain of 2.83 allows the LM4817's to reach full output swing and maintain low noise and THD+N performance. For this example, let $A_{VD} = 3$.

The amplifier's overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (11).

$$R_f/R_i = A_{VD}/2 \quad (13)$$

The value of R_f is 30kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \quad (14)$$

and an

$$F_H = 20kHz \times 5 = 100kHz \quad (15)$$

As mentioned in Table 1, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (14).

$$C_i \geq \frac{1}{2\pi R_i f_c} \quad (16)$$

the result is

$$1/(2\pi * 20k\Omega * 20Hz) = 0.398\mu F \quad (17)$$

Use a 0.39µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain, A_{VD}, determines the upper passband response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4817's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-lrestricting bandwidth limitations.

LDO General Information

Figure 38 shows the LM4817's LDO functional block diagram. A 1.25V bandgap reference, an error amplifier and a PMOS pass transistor perform voltage regulation while being supported by shutdown, fault, and the usual Temperature and current protection circuitry

The regulator's topology is the classic type with negative feedback from the output to one of the inputs of the error amplifier. Feedback resistors R_1 and R_2 are either internal or external to the IC, depending on whether it is the fixed voltage version or the adjustable version. The negative feedback and high open loop gain of the error amplifier cause the two inputs of the error amplifier to be virtually equal in voltage. If the output voltage changes due to load changes, the error amplifier provides the appropriate drive to the pass transistor to maintain the error amplifier's inputs as virtually equal. In short, the error amplifier keeps the output voltage constant in order to keep its inputs equal.

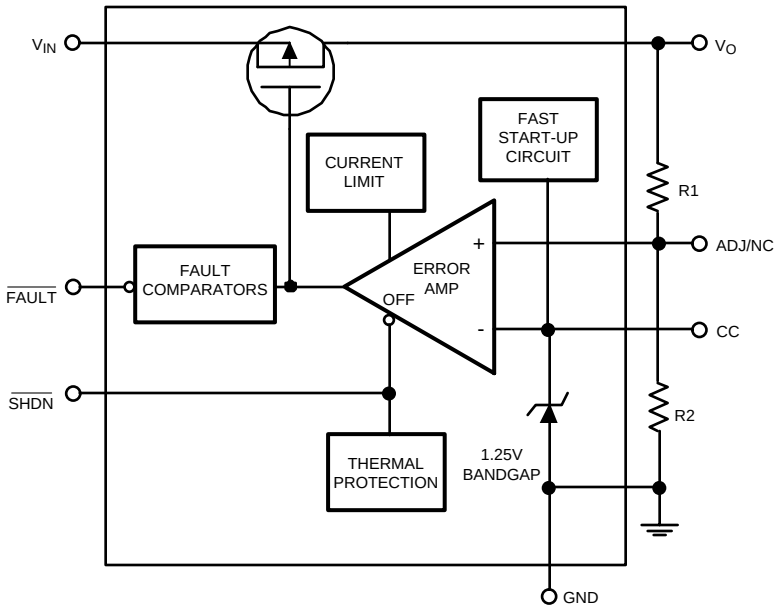


Figure 38. LDO Functional Block Diagram

Output Voltage Setting

The output voltage is set according to the amount of negative feedback (Note that the pass transistor inverts the feedback signal). Figure 39 simplifies the LDO's topology. This type of regulator can be represented as an op amp configured as non-inverting amplifier and a fixed DC Voltage (V_{REF}) for its input signal. The special characteristic of this op amp is its extra-large output transistor that only sources current. In terms of its non-inverting configuration, the output voltage equals V_{REF} times the closed loop gain:

$$V_O = V_{REF}\left[\frac{R_1}{R_2} + 1\right] \quad (18)$$

Utilize Equation (17) for adjusting the output to a particular voltage:

$$R_1 = R_2\left[\frac{V_O}{1.25V} - 1\right] \quad (19)$$

Choose R_2 = 100k to optimize accuracy, power supply rejection, noise and power consumption.

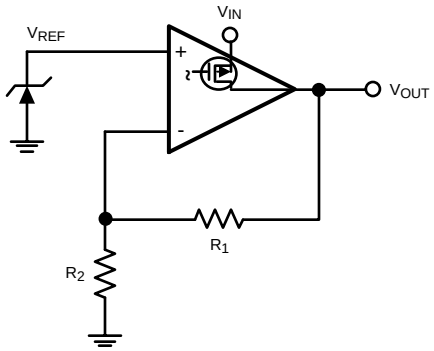


Figure 39. Regulator Topology Simplified

Similarity in the output capabilities exists between op amps and linear regulators. Just as rail-to-rail output op amps allow their output voltage to approach the supply voltage, low dropout regulators (LDOs) allow their output voltage to operate close to the input voltage. Both achieve this by the configuration of their output transistors. Standard op amps and regulator outputs are at the source (or emitter) of the output transistor. Rail-to-rail op amp and LDO regulator outputs are at the drain (or collector) of the output transistor. This replaces the threshold (or diode drop) limitations on the output with the less restrictive source-to-drain (or V_{SAT}) limitations. There is a trade-off, of course. The output impedance become significantly higher, thus providing a critically lower pole when combined with the capacitive load. That's why rail-to-rail op amps are usually poor at driving capacitive loads and recommend a series output resistor when doing so. LDOs require the same series resistance except that the internal resistance of the output capacitor will usually suffice. Refer to Output Capacitance for more information.

Output Capacitance

The LDO is specifically designed to employ ceramic output capacitors as low as 2.2µF. Ceramic capacitors below 10µF offer significant cost and space savings, along with high frequency noise filtering. Higher values and other types and of capacitor may be used, but their equivalent series resistance (ESR) should be maintained below 0.5Ω

Ceramic capacitor of the value required by the LDO are available in the following dielectric types: Z5U, Y5V, X5R and X7R. The Z5U and Y5V types exhibit a 50% or more drop in capacitance value as their temperature increases from 25°C, an important consideration. The X5R generally maintain their capacitance value within ±20%. The X7R type are desirable for their tighter tolerance of 10% over temperature.

Ceramic capacitors pose a challenge because of their relatively low ESR. Like most other LDOs, the LDO relies on a zero in the frequency response to compensate against excessive phase shift in the regulator's feedback loop. If the phase shift reaches 360° (i.e.; becomes positive), the regulator will oscillate. This compensation usually resides in the zero generated by the combination of the output capacitor with its equivalent series resistance (ESR). The zero is intended to cancel the effects of the pole generated by the load capacitance (C_L) combined with the parallel combination of the load resistance (R_L) and the output resistance (R_O) of the regulator. The challenge posed by low ESR capacitors is that the zero it generates can be too high in frequency for the pole that it's intended to compensate. The LM4817 overcomes this challenge by internally generating a strategically placed zero.

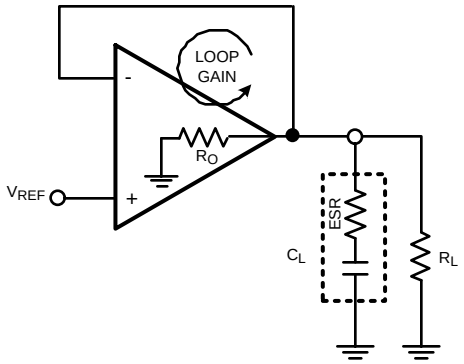


Figure 40. Simplified Model of Regulator Loop Gain Components

Figure 40 shows a basic model for the linear regulator that helps describe what happens to the output signal as it is processed through its feedback loop; that is, describe its loop gain (LG). The LG includes two main transfer functions: the error amplifier and the load. The error amplifier provides voltage gain and a dominant pole, while the load provides a zero and a pole. The LG of the model in Figure 39 is described by Equation (18):

$$LG\ (j\omega) = \frac{A_O}{1 + j\left[\frac{\omega}{\omega_{POLE}}\right]} * \frac{1 + j\omega\ (ESR \times C_L)}{1 + j\omega\ ((ESR + R_O\ //\ R_L)\ C_L)} \tag{20}$$

The first term of Equation (18) expresses the voltage gain (numerator) and a single pole role-off (denominator) of the error amplifier. The second term expresses the zero (numerator) and pole (denominator) of the load in combination with the R_O of the regulator.

Figure 41 shows a Bode plot that represents a case where the zero contributed by the load is too high to cancel the effect of the pole contributed by the load and R_O. The solid line illustrates the loop gain while the dashed line illustrates the corresponding phase shift. Notice that the phase shift at unity gain is a total 360° -the criteria for oscillation.

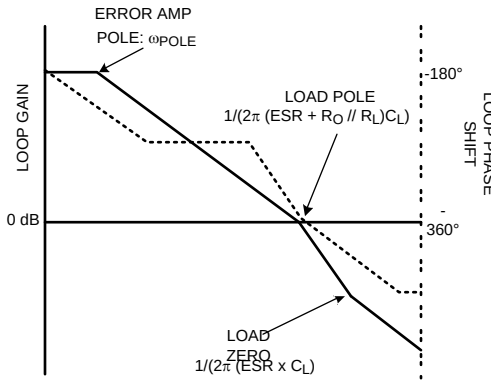


Figure 41. Loop Gain Bode Plot Illustrating Inadequately High Zero for Stability Compensation

The LDO generates an internal zero that makes up for the inadequately high zero of the low ESR ceramic output capacitor. This internally generated zero is strategically placed to provide positive phase shift near unity gain, thus providing a stable phase margin.

No-Load Stability

The LM4817 remains stable during no-load conditions, a necessary feature for CMOS RAM keep-alive applications.

Input Capacitor

The LM4817 requires a minimum input capacitance of about 1µF. The value may be increased indefinitely. The type is not critical to stability. However, instability may occur with bench set-ups where long supply leads are used, particularly at near dropout and high current conditions. This is attributed to the lead inductance coupling to the output through the gate oxide of the pass transistor; thus, forming a pseudo LCR network within the Loop-gain. A 10µF tantalum input capacitor remedies this non-situ condition; its larger ESR acts to dampen the pseudo LCR network. This may only be necessary for some bench setups. 1µF ceramic input capacitor are fine for most end-use applications.

If a tantalum input capacitor is intended for the final application, it is important to consider their tendency to fail in short circuit mode, thus potentially damaging the part.

Noise Bypass Capacitor

The noise bypass capacitor (CC) significantly reduces the LDO'soutput noise. Connect the CC capacitor between pin 6 and ground. The optimum value for CC is 33nF.

Pin 6 directly connects to the high impedance output of the bandgap. The DC leakage of the CC capacitor should be considered; loading down the reference will reduce the output voltage. NPO and COG ceramic capacitors typically offer very low leakage. Polypropylene and polycarbonate film carbonate capacitor offer even lower leakage currents.

CC does not affect the transient response; however, it does affect turn-on time. The smaller the CC value, the quicker the turn-on time.

Power Dissipation

Power dissipation refers to the part's ability to radiate heat away from the silicon, with packaging being a key factor. A reasonable analogy is the packaging a human being might wear, a jacket for example. A jacket keeps a person comfortable on a cold day, but not so comfortable on a hot day. It would be even worse if the person was exerting power (exercising). This is because the jacket has resistance to heat flow to the outside ambient air, like the IC package has a thermal resistance from its junctions to the ambient (θ_{JA}).

θ_{JA} has a unit of temperature per power and can be used to calculate the IC's junction temperature as follows:

$$T_J = \theta_{JA} (PD) + T_A \quad (21)$$

T_J is the junction temperature of the IC. θ_{JA} is the thermal resistance from the junction to the ambient air outside the package. PD is the power exerted by the IC, and T_A is the ambient temperature.

PD is calculated as follows:

$$PD = I_{OUT} (V_{IN} - V_O) \quad (22)$$

θ_{JA} for the LM4817 package (VSSOP-8) is 223°C/W with no forced air flow, 182°C/W with 225 linear feet per minute (LFPM) of air flow, 163°C/W with 500 LFPM of air flow, and 149°C/W with 900 LFPM of air flow.

θ_{JA} can also be decreased (improved) by considering the layout of the PC board: heavy traces (particularly at V_{IN} and the two V_{OUT} pins), large planes, through-holes, etc.

Improvements and absolute measurements of the θ_{JA} can be estimated by utilizing the thermal shutdown circuitry that is internal to the IC. The thermal shutdown turns off the pass transistor of the device when its junction temperature reaches 160°C (Typical). The pass transistor doesn't turn on again until the junction temperature drops about 10°C (hysteresis).

Using the thermal shutdown circuit to estimate , θ_{JA} can be done as follows: With a low input to output voltage differential, set the load current to 300mA. Increase the input voltage until the thermal shutdown begins to cycle on and off. Then slowly decrease V_{IN} (100mV increments) until the part stays on. Record the resulting voltage differential (V_D) and use it in Equation 23:

$$\theta_{JA} = \frac{(160 - T_A)}{(0.300 \times V_D)} \quad (23)$$

Fault Detection

The LDO provides a $\overline{\text{FAULT}}$ pin that goes low during out of regulation conditions like current limit and thermal shutdown, or when it approaches dropout. The latter monitors the input-to-output voltage differential and compares it against a threshold that is slightly above the dropout voltage. This threshold also tracks the dropout voltage as it varies with load current. Refer to Fault Detect vs. Load Current curve in LDO Typical Performance Characteristics.

The $\overline{\text{FAULT}}$ pin requires a pull-up resistor since it is an open-drain output. This resistor should be large in value to reduce energy drain. A 100kΩ pull-up resistor works well for most applications.

Figure 42 shows the LDO's with delay added to the $\overline{\text{FAULT}}$ pin for the reset pin of a microprocessor. The output of the comparator stays low for a preset amount of time after the regulator comes out of a fault condition.

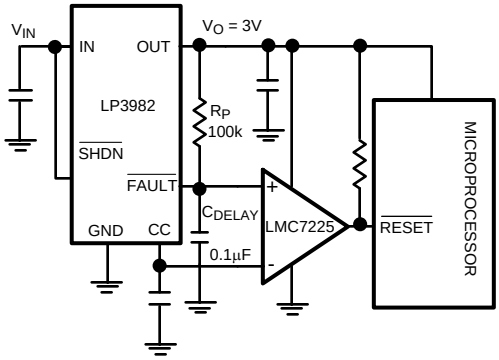


Figure 42. Power on Delayed Reset Application

The delay time for the application of Figure 41 is set as follows:

$$C_{DELAY} = \frac{-t}{R_P \ln\left[1 - \frac{V_{REF}}{V_O}\right]} \quad (24)$$

The application is set for a reset delay time of 8.8ms. Note that the comparator should have high impedance inputs so as to not load down the V_{REF} at the CC pin of the LM4817.

Shutdown

The LM4817's LDO goes into sleep mode when the $\overline{\text{SHDN}}$ pin is in a logic low condition. During this condition, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to 1nA typical. The maximum guaranteed voltage for a logic low at the $\overline{\text{SHDN}}$ pin is 0.4V. A minimum guaranteed voltage of 2V at the $\overline{\text{SHDN}}$ pin will turn the LDO back on. The $\overline{\text{SHDN}}$ pin may be directly tied to V_{IN} to keep the part on. The $\overline{\text{SHDN}}$ pin may exceed V_{IN} but not the ABS MAX of 6.5V.

Figure 42 shows an application that uses the $\overline{\text{SHDN}}$ pin. It detects when the battery is too low and disconnects the load by turning off the regulator. A micropower comparator (LMC7215) and reference (LM385) are combined with resistors to set the minimum battery voltage. At the minimum battery voltage, the comparator output goes low and tuns off the LDO and corresponding load. Hysteresis is added to the minimum battery threshold to prevent the battery's recovery voltage from falsely indicating an above minimum condition. When the load is disconnected from the battery, it automatically increases in terminal voltage because of the reduced IR drop across its internal resistance. The Minimum battery detector of Figure 42 has a low detection threshold (V_{LT}) of 3.6V that corresponds to the minimum battery voltage. The upper threshold (V_{UT}) is set for 4.6V in order to exceed the recovery voltage of the battery.

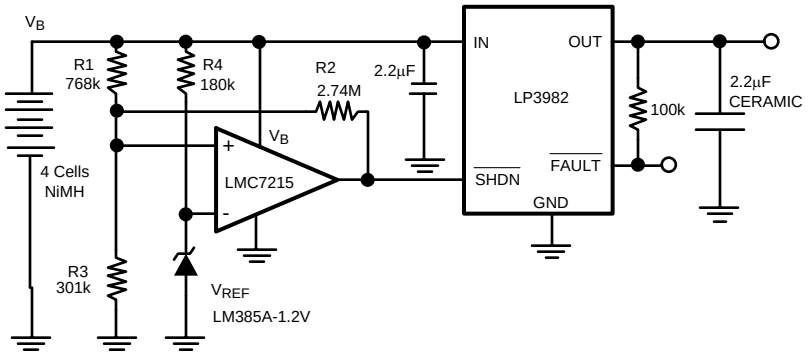


Figure 43. Minimum Battery Detector that Disconnects the Load Via the $\overline{\text{SHDN}}$ Pin of the LM4817

Resistor value for V_{UT} and V_{LT} are determined as follows:

$$G_T = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

$$V_{UT} = R_1 (V_{REF})\, G_T$$

$$V_{LT} = R_1 // R_2 (V_{REF})\, G_T \quad (25)$$

(The application of Figure 42 used a G_T of 5µ mho)

$$R_1 = \frac{V_{UT1}}{V_{REF}(G_T)} \quad (26)$$

$$R_2 = \frac{1}{\frac{V_{REF}(G_T)}{V_{LT}} - \frac{1}{R_1}} \quad (27)$$

$$R_3 = \frac{1}{G_T - \left[\frac{1}{R_1} + \frac{1}{R_2}\right]} \quad (28)$$

The above procedure assumes a rail-to-rail output comparator. Essentially, R_2 is in parallel with R_1 prior to reaching the lower threshold, then R_2 becomes parallel with R_3 for the upper threshold. Note that the application requires rail-to-rail input as well.

The resistor values shown in Figure 43 are the closest practical to calculated values.

Fast Start-Up

The LM4817's LDO provides fast start-up time for better system efficiency. The start-up speed is maintained when using the optional noise bypass capacitor. An internal 500µA current source charges the capacitor until it reaches about 90% of its final value.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 44 through Figure 46 show the recommended two-layer PC board layout that is optimized for the 28-pin PWP-packaged LM4817 and associated components. These circuits are designed for use with an external 5V supply and 8Ω (or greater) speakers.

This circuit board is easy to use. Apply 5V and ground to the board's V_{DD} and GND pads, respectively. Connect speakers between the board's -OUTA and +OUTA and OUTB and +OUTB pads. Apply the stereo input signal to the input pins labeled "-INA" and "-INB." The stereo input signal's ground references are connected to the respective input channel's "GND" pin, adjacent to the input pins.

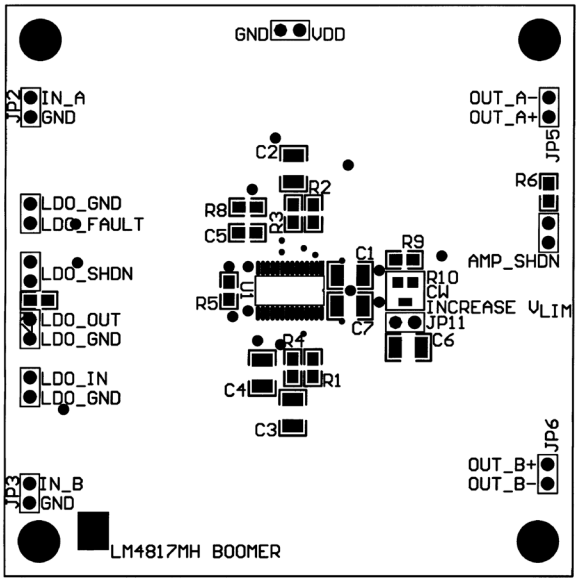


Figure 44. Recommended PWP board layout: component-side silkscreen

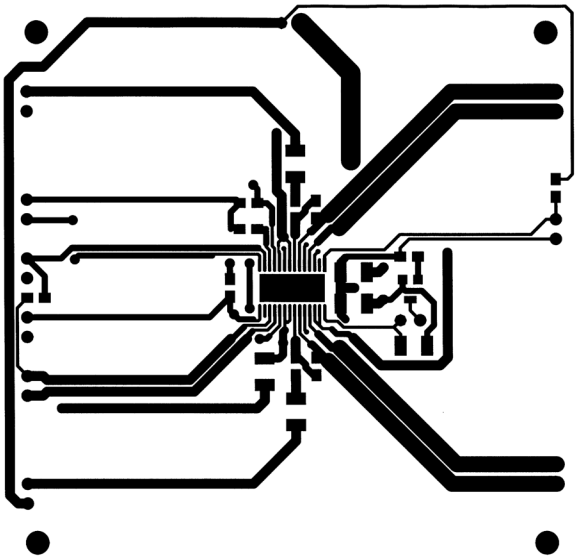


Figure 45. Recommended PWP PC board layout: component-side layout

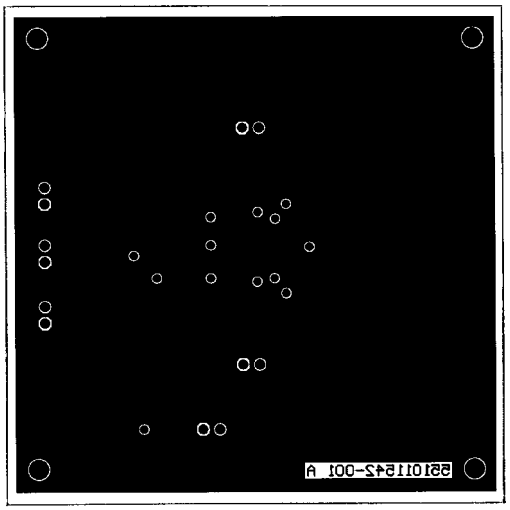


Figure 46. Recommended PWP board layout: bottom-side layout

Revision History

Rev	Date	Description
1.0	2/08/06	Changed the Limit (from 3.0 to 2.7) on V_{IH} (Stereo Amplifier Elect. Char. for Entire IC) table, then re-released D/S to the WEB.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4817MHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LM4817MH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

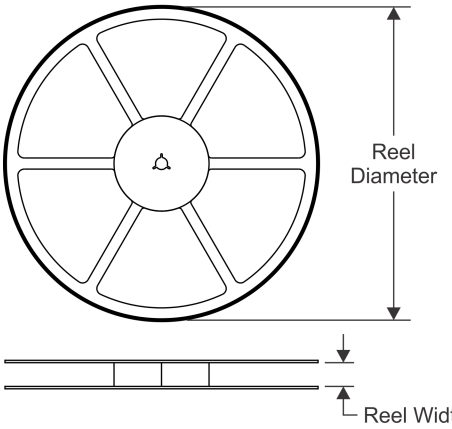
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

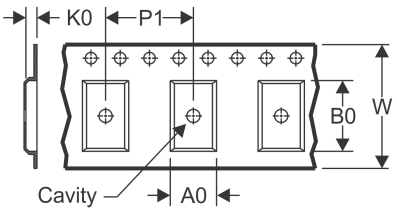
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

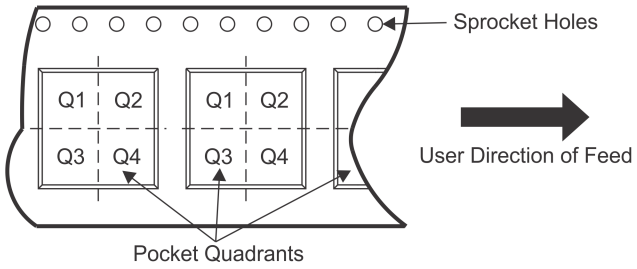


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

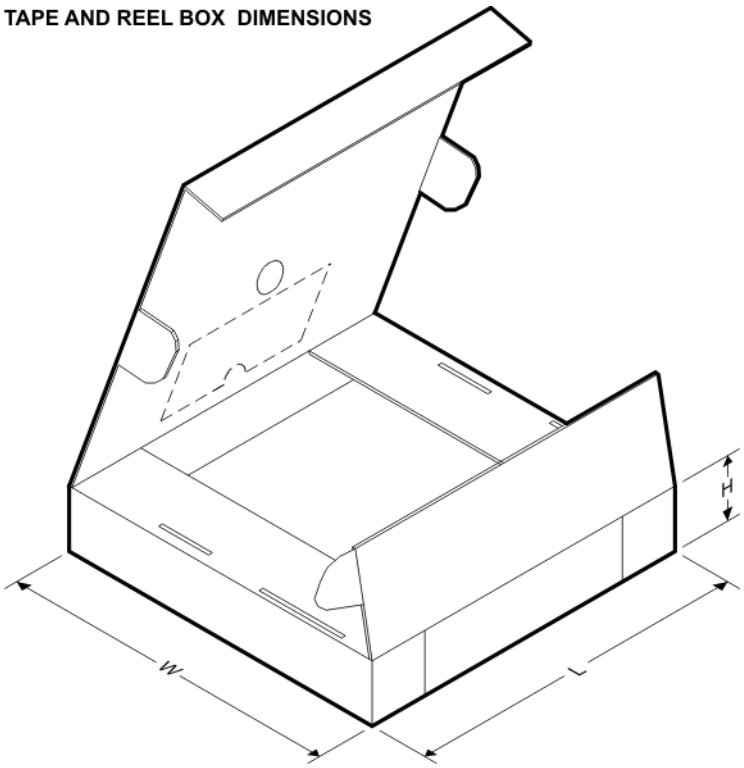
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4817MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

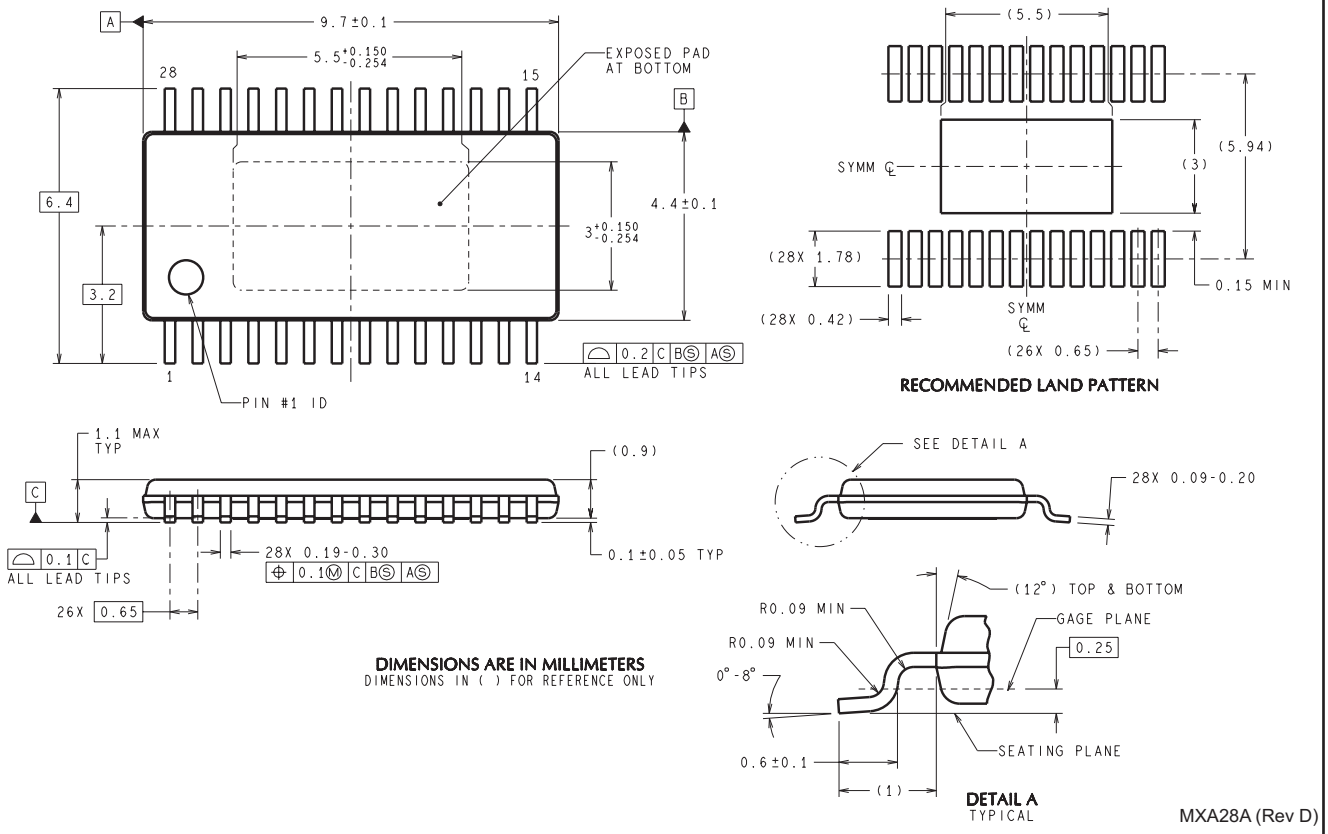
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4817MHX/NOPB	HTSSOP	PWP	28	2500	349.0	337.0	45.0

PWP0028A



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