

# LM4836 Boomer® Audio Power Amplifier Series

## Stereo 2W Audio Power Amplifiers

### with DC Volume Control, Bass Boost, and Input Mux

#### General Description

The LM4836 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω (Note 1) with less than 1.0% THD+N, or 2.2W into 3Ω (Note 2) with less than 1.0% THD+N.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4836 incorporates a DC volume control, stereo bridged audio power amplifiers, selectable gain or bass boost, and an input mux making it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4836 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

**Note 1:** When properly mounted to the circuit board, the LM4836MTE will deliver 2W into 4Ω. The LM4836MT will deliver 1.1W into 8Ω. See the Application Information section for LM4836MTE usage information.

**Note 2:** An LM4836MTE which has been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

#### Key Specifications

- P<sub>O</sub> at 1% THD+N
  - into 3Ω (LM4836MTE) 2.2W (typ)
  - into 4Ω (LM4836MTE) 2.0W (typ)
  - into 8Ω (LM4836) 1.1W (typ)
- Single-ended mode THD+N at 85mW into 32Ω 1.0% (typ)
- Shutdown current 0.2μA (typ)

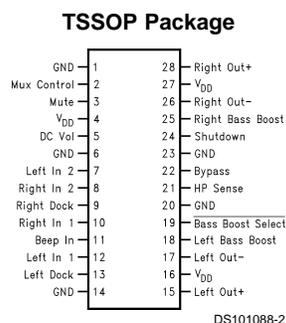
#### Features

- PC98 and PC99 Compliant
- DC Volume Control Interface
- Input mux
- System Beep Detect
- Stereo switchable bridged/single-ended power amplifiers
- Selectable internal/external gain and bass boost configurable
- "Click and pop" suppression circuitry
- Thermal shutdown protection circuitry

#### Applications

- Portable and Desktop Computers
- Multimedia Monitors
- Portable Radios, PDAs, and Portable TVs

#### Connection Diagram



#### Top View

**Order Number LM4836MT**  
**See NS Package Number MTC28 for TSSOP**  
**Order Number LM4836MTE**  
**See NS Package Number MXA28A for Exposed DAP TSSOP**

**Absolute Maximum Ratings** (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to $V_{DD} + 0.3V$
Power Dissipation	Internally limited
ESD Susceptibility (Note 12)	2500V
ESD Susceptibility (Note 13)	250V
Junction Temperature	150°C
Soldering Information	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

$\theta_{JC}$ (typ)—MTC28	20°C/W
$\theta_{JA}$ (typ)—MTC28	80°C/W
$\theta_{JC}$ (typ)—MXA28A	2°C/W
$\theta_{JA}$ (typ)—MXA28A (Note 4)	41°C/W
$\theta_{JA}$ (typ)—MXA28A (Note 3)	54°C/W
$\theta_{JA}$ (typ)—MXA28A (Note 5)	59°C/W
$\theta_{JA}$ (typ)—MXA28A (Note 6)	93°C/W

**Operating Ratings**

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$	-40°C $\leq T_A \leq$ 85°C
Supply Voltage		2.7V $\leq V_{DD} \leq$ 5.5V

**Electrical Characteristics for Entire IC**

(Notes 7, 10)

The following specifications apply for  $V_{DD} = 5V$  and  $T_A = 25^\circ C$  unless otherwise noted.

Symbol	Parameter	Conditions	LM4836		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
$V_{DD}$	Supply Voltage			2.7	V (min)
				5.5	V (max)
$I_{DD}$	Quiescent Power Supply Current	$V_{IN} = 0V, I_O = 0A$	15	30	mA (max)
$I_{SD}$	Shutdown Current	$V_{pin\ 24} = V_{DD}$	0.2	2.0	$\mu A$ (max)
$V_{IH}$	Headphone Sense High Input Voltage			4	V (min)
$V_{IL}$	Headphone Sense Low Input Voltage			0.8	V (max)

**Electrical Characteristics for Volume Attenuators**

(Notes 7, 10)

The following specifications apply for  $V_{DD} = 5V$  and  $T_A = 25^\circ C$  unless otherwise noted.

Symbol	Parameter	Conditions	LM4836		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
$C_{RANGE}$	Attenuator Range	Gain with $V_{pin\ 5} \geq 4.5V$	0	$\pm 0.5$	dB (max)
			0	-1.0	dB (min)
$C_{RANGE}$	Attenuator Range	Attenuation with $V_{pin\ 5} = 0V$	-73	-70	dB (min)
$A_M$	Mute Attenuation	$V_{pin\ 3} = 5V, \text{ Bridged Mode}$	-88	-80	dB (min)
		$V_{pin\ 3} = 5V, \text{ Single-Ended Mode}$	-80	-70	dB (min)

**Electrical Characteristics for Single-Ended Mode Operation**

(Notes 7, 10)

The following specifications apply for  $V_{DD} = 5V$  and  $T_A = 25^\circ C$  unless otherwise noted.

Symbol	Parameter	Conditions	LM4836		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
$P_O$	Output Power	THD+N = 1.0%; f = 1kHz; $R_L = 32\Omega$	85		mW
		THD+N = 10%; f = 1 kHz; $R_L = 32\Omega$	95		mW

## Electrical Characteristics for Single-Ended Mode Operation (Continued)

(Notes 7, 10)

The following specifications apply for  $V_{DD} = 5V$  and  $T_A = 25^\circ C$  unless otherwise noted.

Symbol	Parameter	Conditions	LM4836		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
THD+N	Total Harmonic Distortion+Noise	$V_{OUT} = 1V_{RMS}$ , $f=1kHz$ , $R_L = 10k\Omega$ , $A_{VD} = 1$	0.065		%
PSRR	Power Supply Rejection Ratio	$C_B = 1.0 \mu F$ , $f = 120 Hz$ , $V_{RIPPLE} = 200 mV_{rms}$	58		dB
SNR	Signal to Noise Ratio	$P_{OUT} = 75 mW$ , $R_L = 32\Omega$ , A-Wtd Filter	102		dB
$X_{talk}$	Channel Separation	$f=1kHz$ , $C_B = 1.0 \mu F$	65		dB

## Electrical Characteristics for Bridged Mode Operation

(Notes 7, 10)

The following specifications apply for  $V_{DD} = 5V$  and  $T_A = 25^\circ C$  unless otherwise noted.

Symbol	Parameter	Conditions	LM4836		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
$V_{OS}$	Output Offset Voltage	$V_{IN} = 0V$	10	50	mV (max)
$P_O$	Output Power	THD + N = 1.0%; $f=1kHz$ ; $R_L = 3\Omega$ (Note 8)	2.2		W
		THD + N = 1.0%; $f=1kHz$ ; $R_L = 4\Omega$ (Note 9)(Note 15)	2		W
		THD = 1.5% (max); $f = 1 kHz$ ; $R_L = 8\Omega$	1.1	1.0	W (min)
		THD+N = 10%; $f = 1 kHz$ ; $R_L = 8\Omega$	1.5		W
THD+N	Total Harmonic Distortion+Noise	$P_O = 1W$ , $20 Hz < f < 20 kHz$ , $R_L = 8\Omega$ , $A_{VD} = 2$	0.3		%
		$P_O = 340 mW$ , $R_L = 32\Omega$	1.0		%
PSRR	Power Supply Rejection Ratio	$C_B = 1.0 \mu F$ , $f = 120 Hz$ , $V_{RIPPLE} = 200 mV_{rms}$ ; $R_L = 8\Omega$	74		dB
SNR	Signal to Noise Ratio	$V_{DD} = 5V$ , $P_{OUT} = 1.1W$ , $R_L = 8\Omega$ , A-Wtd Filter	93		dB
$X_{talk}$	Channel Separation	$f=1kHz$ , $C_B = 1.0 \mu F$	70		dB

**Note 3:** The  $\theta_{JA}$  given is for an MXA28A package whose exposed-DAP is soldered to an exposed  $2in^2$  piece of 1 ounce printed circuit board copper.

**Note 4:** The  $\theta_{JA}$  given is for an MXA28A package whose exposed-DAP is soldered to a  $2in^2$  piece of 1 ounce printed circuit board copper on a bottom side layer through 21 8mil vias.

**Note 5:** The  $\theta_{JA}$  given is for an MXA28A package whose exposed-DAP is soldered to an exposed  $1in^2$  piece of 1 ounce printed circuit board copper.

**Note 6:** The  $\theta_{JA}$  given is for an MXA28A package whose exposed-DAP is not soldered to any copper.

**Note 7:** All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 2.

**Note 8:** When driving  $3\Omega$  loads from a 5V supply the LM4836MTE exposed DAP must be soldered to the circuit board and forced-air cooled.

**Note 9:** When driving  $4\Omega$  loads from a 5V supply the LM4836MTE exposed DAP must be soldered to the circuit board.

**Note 10:** *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

**Note 11:** The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable power dissipation is  $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ . For the LM4836MT,  $T_{JMAX} = 150^\circ C$ , and the typical junction-to-ambient thermal resistance, when board mounted, is  $80^\circ C/W$  assuming the MTC28 package.

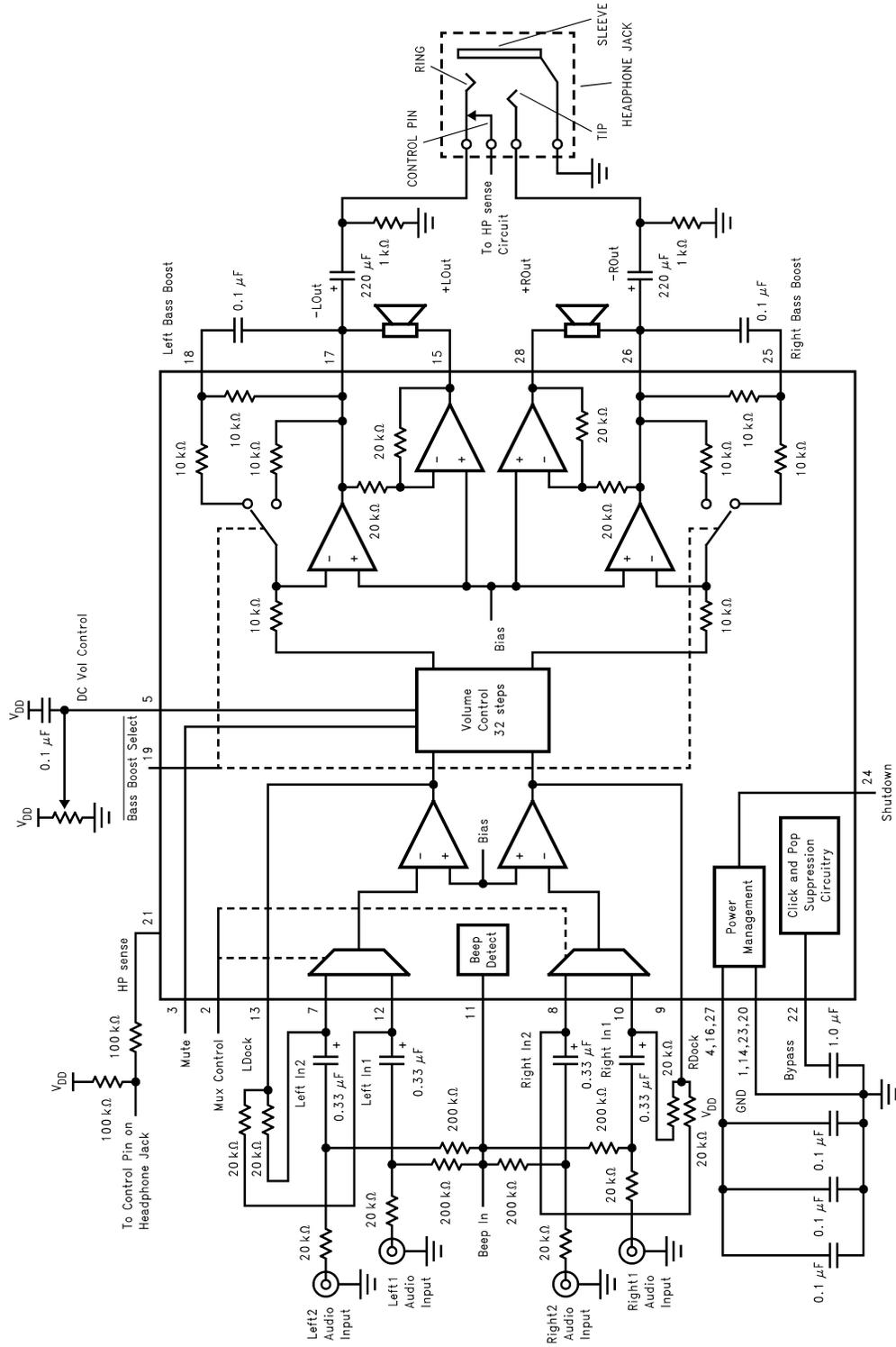
**Note 12:** Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

**Note 13:** Machine Model, 220 pF–240 pF discharged through all pins.

**Note 14:** Typicals are measured at  $25^\circ C$  and represent the parametric norm.

**Note 15:** Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

# Typical Application



DS101089-3

FIGURE 1. Typical Application Circuit

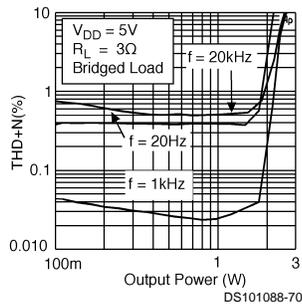
## Truth Table for Logic Inputs (Note 16)

Mute	Mux Control	HP Sense	Inputs Selected	Bridged Output	Single-Ended Output
0	0	0	Left In 1, Right In 1	Vol. Adjustable	-
0	0	1	Left In 1, Right In 1	Muted	Vol. Adjustable
0	1	0	Left In 2, Right In 2	Vol. Adjustable	-
0	1	1	Left In 2, Right In 2	Muted	Vol. Adjustable
1	X	X	-	Muted	Muted

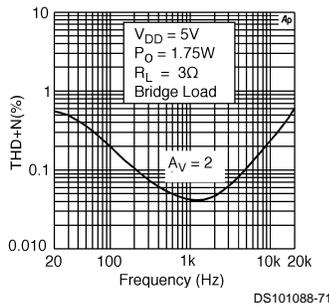
**Note 16:** If system beep is detected on the Beep in pin (pin 11) and beep is fed to inputs, the system beep will be passed through the bridged amplifier regardless of the logic of the Mute, HP sense, or DC Volume Control pins.

## Typical Performance Characteristics MTE Specific Characteristics

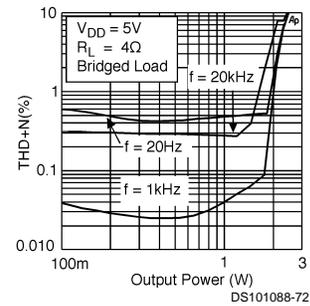
**LM4836MTE**  
THD+N vs Output Power



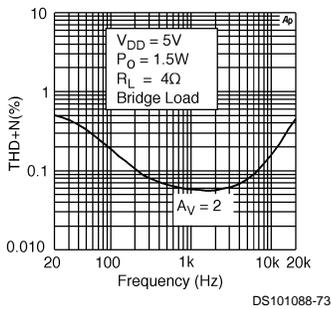
**LM4836MTE**  
THD+N vs Frequency



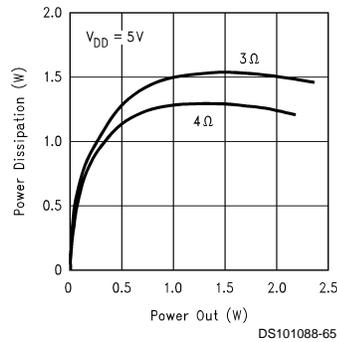
**LM4836MTE**  
THD+N vs Output Power



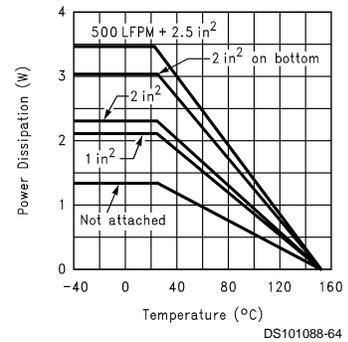
**LM4836MTE**  
THD+N vs Frequency



**LM4836MTE**  
Power Dissipation vs Output Power



**LM4836MTE (Note 17)**  
Power Derating Curve



**Note 17:** These curves show the thermal dissipation ability of the LM4836MTE at different ambient temperatures given these conditions:

**500LFPM + 2in<sup>2</sup>:** The part is soldered to a 2in<sup>2</sup>, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it.

**2in<sup>2</sup> on bottom:** The part is soldered to a 2in<sup>2</sup>, 1oz. copper plane that is on the bottom side of the PC board through 21 8 mil vias.

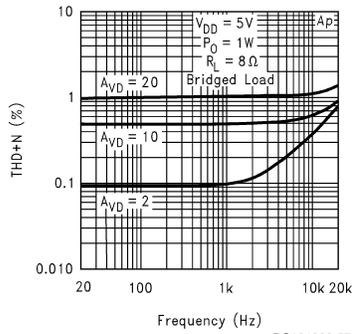
**2in<sup>2</sup>:** The part is soldered to a 2in<sup>2</sup>, 1oz. copper plane.

**1in<sup>2</sup>:** The part is soldered to a 1in<sup>2</sup>, 1oz. copper plane.

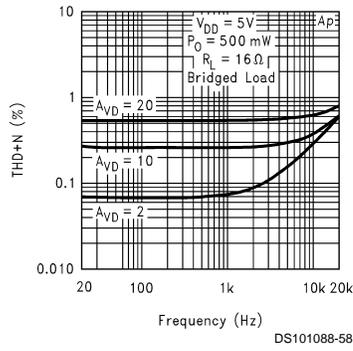
**Not Attached:** The part is not soldered down and is not forced-air cooled.

# Non-MTE Specific Characteristics

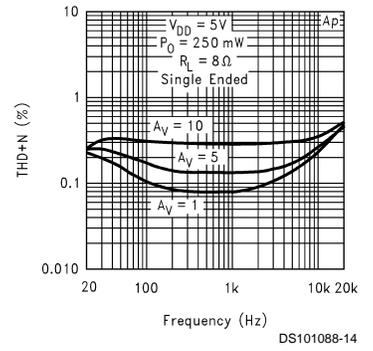
THD+N vs Frequency



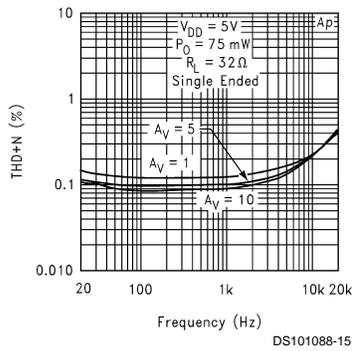
THD+N vs Frequency



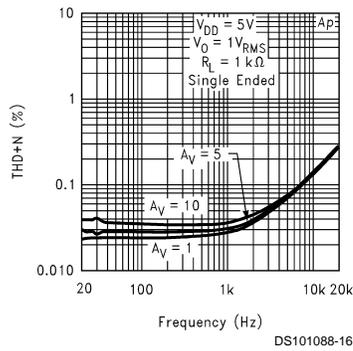
THD+N vs Frequency



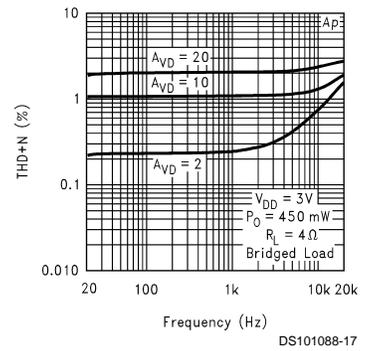
THD+N vs Frequency



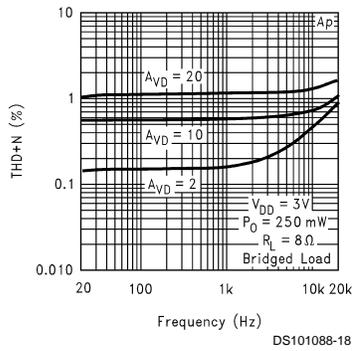
THD+N vs Frequency



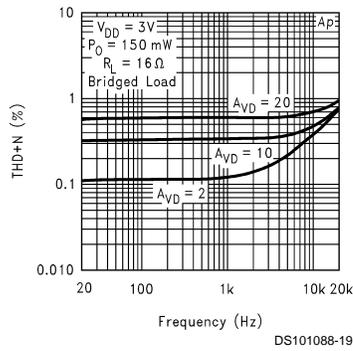
THD+N vs Frequency



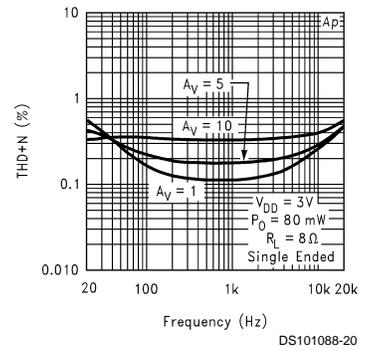
THD+N vs Frequency



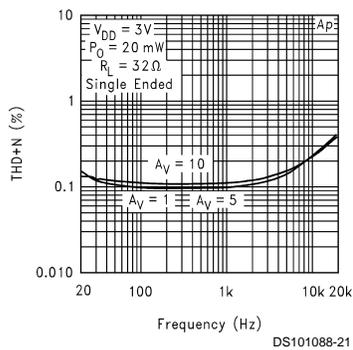
THD+N vs Frequency



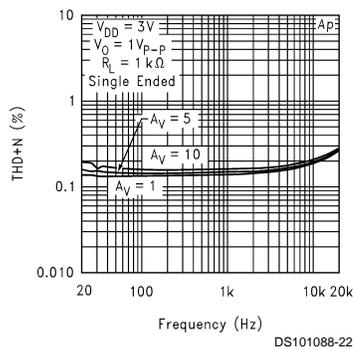
THD+N vs Frequency



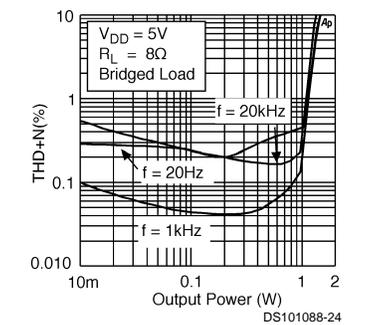
THD+N vs Frequency



THD+N vs Frequency

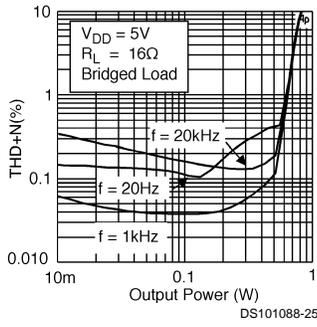


THD+N vs Output Power

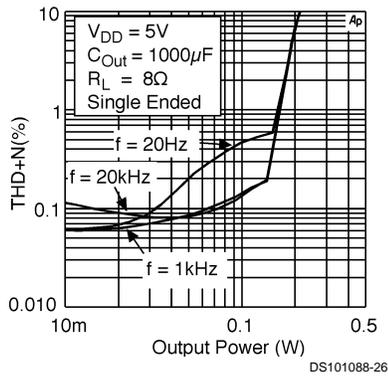


# Non-MTE Specific Characteristics (Continued)

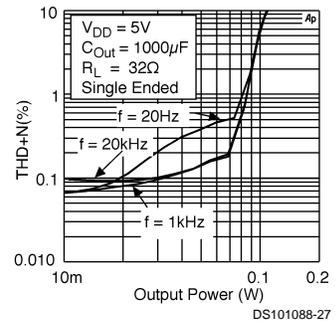
**THD+N vs Output Power**



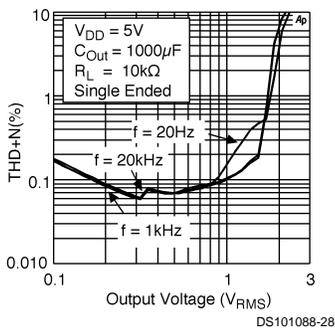
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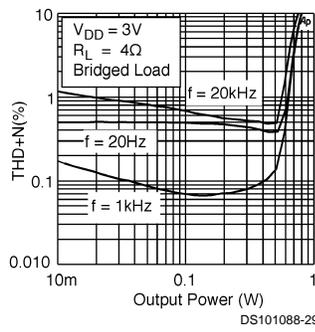
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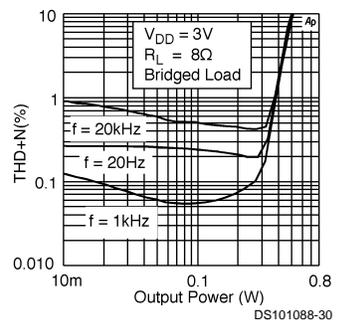
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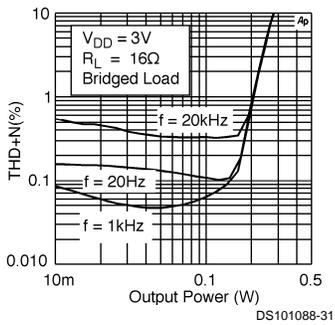
**THD+N vs Output Power**



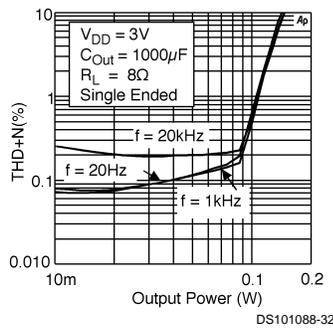
**THD+N vs Output Power**



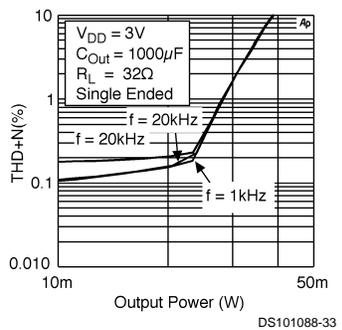
**THD+N vs Output Power**



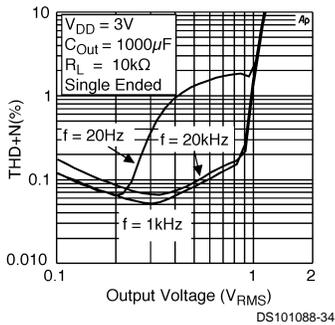
**THD+N vs Output Power**



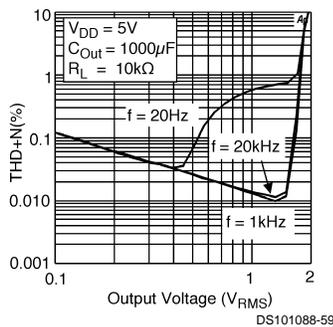
**THD+N vs Output Power**



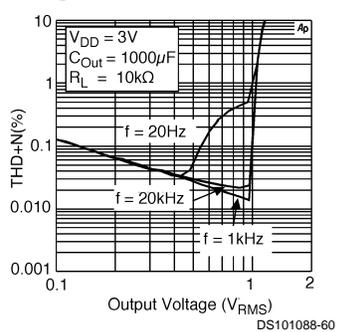
**THD+N vs Output Power**



**THD+N vs Output Voltage  
Docking Station Pins**

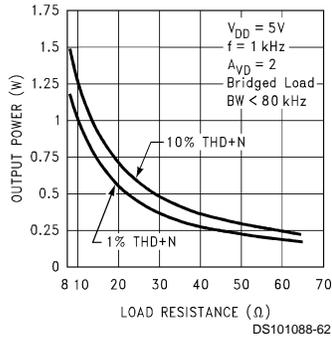


**THD+N vs Output Voltage  
Docking Station Pins**

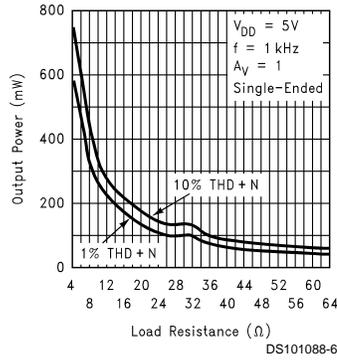


# Non-MTE Specific Characteristics (Continued)

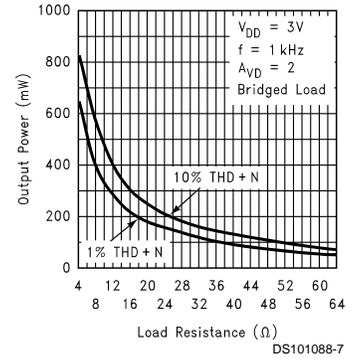
**Output Power vs Load Resistance**



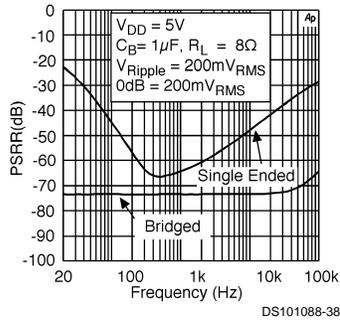
**Output Power vs Load Resistance**



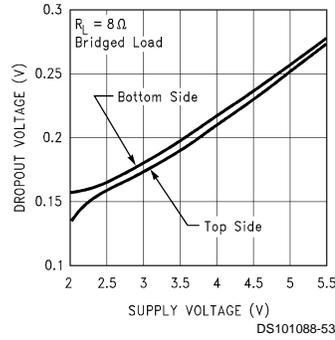
**Output Power vs Load Resistance**



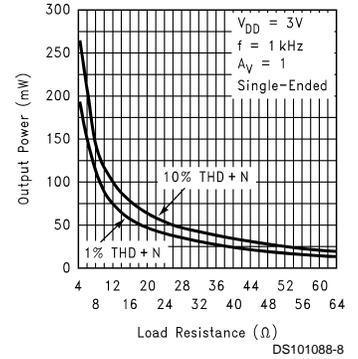
**Power Supply Rejection Ratio**



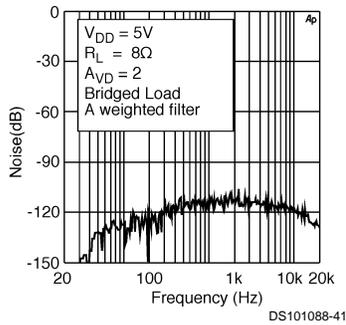
**Dropout Voltage**



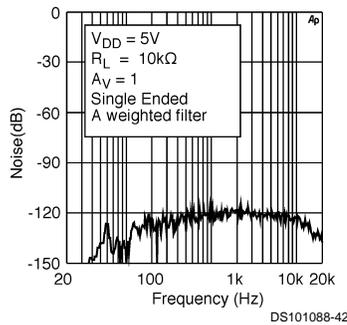
**Output Power vs Load Resistance**



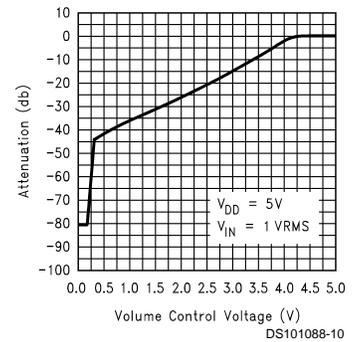
**Noise Floor**



**Noise Floor**

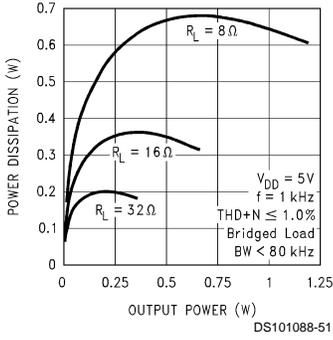


**Volume Control Characteristics**

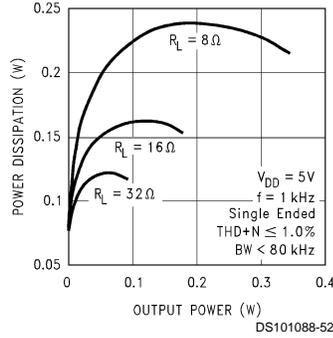


# Non-MTE Specific Characteristics (Continued)

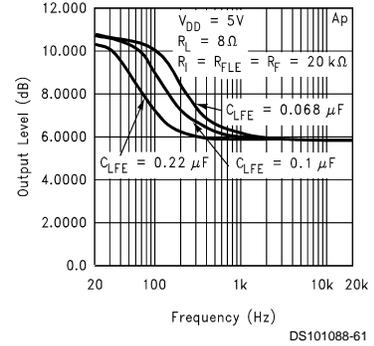
**Power Dissipation vs Output Power**



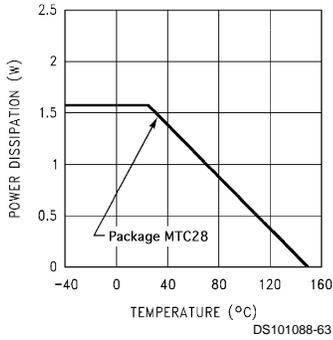
**Power Dissipation vs Output Power**



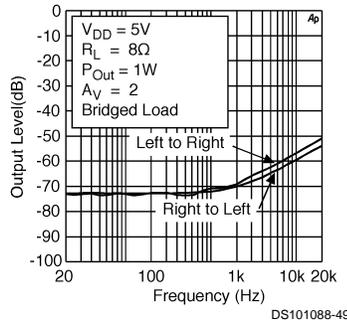
**External Gain/ Bass Boost Characteristics**



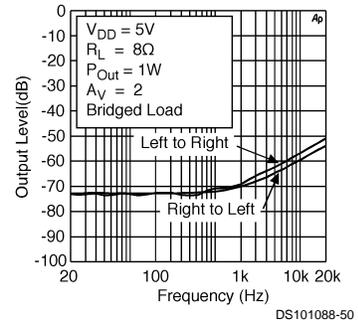
**Power Derating Curve**



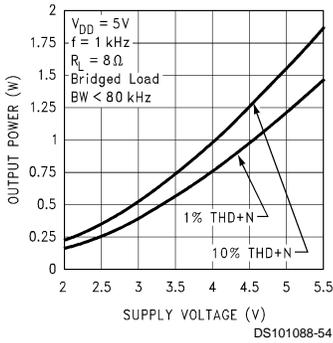
**Crosstalk**



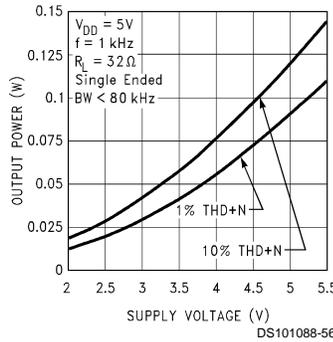
**Crosstalk**



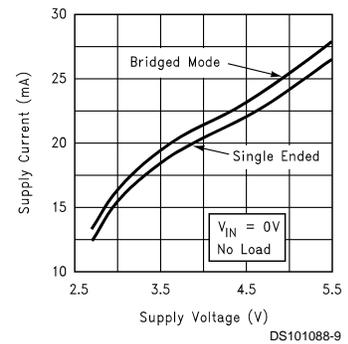
**Output Power vs Supply Voltage**



**Output Power vs Supply Voltage**



**Supply Current vs Supply Voltage**



## Application Information

### EXPOSED-DAP MOUNTING CONSIDERATIONS

The exposed-DAP (die attach pad) must be tied to ground. The exposed-DAP of the LM4836MTE requires special attention to thermal design. If thermal design issues are not properly addressed, an LM4836MTE driving 4Ω will go into thermal shutdown.

The exposed-DAP on the bottom of the LM4836MTE should be soldered down to a copper plane on the circuit board. The copper plane will conduct heat away from the exposed-DAP. If the copper plane is not on the top surface of the circuit board, 20 to 30 vias of 0.010 inches or smaller in diameter should be used to thermally couple the exposed-DAP to the plane. For good thermal conduction, the vias must be plated-through and solder-filled.

The copper plane used to conduct heat away from the exposed-DAP should be as large as practical. If the plane is on the same side of the circuit board as the exposed-DAP, 2 in<sup>2</sup> is the minimum for 5V operation into 4Ω. If the heat sink plane is buried or not on the same side as the exposed-DAP, 5in<sup>2</sup> is the minimum for 5V operation into 4Ω. If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling may be required to keep the LM4836MTE junction temperature below the thermal shutdown temperature (150°C). See the power derating curve for the LM4836MTE for derating information.

The LM4836MTE requires forced-air cooling when operating into 3Ω.

### POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified load.

$$P_{\text{DMAX}} = (V_{\text{DD}})^2 / (2\pi^2 R_L) \quad (1)$$

However, a direct consequence of the increased power delivered to the load by a bridged amplifier is an increase in internal power dissipation. Equation 2 states the maximum power dissipation point for a bridged amplifier operating at a given supply voltage and driving a specified load.

$$P_{\text{DMAX}} = 4(V_{\text{DD}})^2 / (2\pi^2 R_L) \quad (2)$$

Since the LM4836 is a stereo power amplifier, the maximum internal power dissipation is two times that of Equation 1 or Equation 2 depending on the mode of operation. Even with the power dissipation of the stereo amplifiers, the LM4836 does not require heatsinking. The power dissipation from the amplifiers, must not be greater than the package power dissipation that results from Equation 3:

$$P_{\text{DMAX}} = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}} \quad (3)$$

For the LM4836 TSSOP package,  $\theta_{\text{JA}} = 80^\circ\text{C}/\text{W}$  and  $T_{\text{JMAX}} = 150^\circ\text{C}$ . Depending on the ambient temperature,  $T_A$ , of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 and 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased, or the ambient temperature reduced. For the typical application of a 5V power supply, with an 8Ω bridged loads, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 48°C provided that device operation is around the maximum power dissipation points. Power dissipation is a function of output power and

thus, if typical operation is not around the maximum power dissipation point, the ambient temperature can be increased. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers.

### LAYOUT

As stated in the Grounding section, placement of ground return lines is imperative in maintaining the highest level of system performance. It is not only important to route the correct ground return lines together, but also to be aware of where the ground return lines are routed with respect to each other. The output load ground returns should be physically located as far as possible from low signal level lines and their ground return lines.

### 3Ω and 4Ω Layout Considerations

With low impedance loads, the output power at the loads is heavily dependent on trace resistance from the output pins of the LM4836. Traces from the output of the LM4836MTE to the load or load connectors should be as wide as practical. Any resistance in the output traces will reduce the power delivered to the load. For example, with a 4Ω load and 0.1Ω of trace resistance in each output, output power at the load drops from 2W to 1.8W.

Output power is also dependent on supply regulation. To keep the supply voltage from sagging under full output conditions, the supply traces should be as wide as practical.

### Grounding

In order to achieve the best possible performance, there are certain grounding techniques to be followed. All input reference grounds should be tied with their respective source grounds and brought back to the power supply ground separately from the output load ground returns. Bringing the ground returns for the output loads back to the supply separately will keep large signal currents from interfering with the stable AC input ground references. The exposed-DAP of the LM4836MTE package must be tied to ground.

### POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor is improved PSRR due to increased half-supply stability. Typical applications employ a 5 volt regulator with 10 μF and a 0.1 μF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the LM4836. The selection of bypass capacitors, especially  $C_{\text{B}}$ , is thus dependent upon desired PSRR requirements, desired turn on time, click and pop performance as explained in the section, **Proper Selection of External Components**, system cost, and size constraints. It is also recommended to decouple each of the  $V_{\text{DD}}$  pins with a 0.1μF capacitor to ground.

### PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4836 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4836's bridged amplifier should be used in low gain configurations to minimize THD+N values, and maximize the

## Application Information (Continued)

signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1V<sub>rms</sub> are available from sources such as audio codecs.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 1*. Both the input coupling capacitor,  $C_i$ , and the output coupling capacitor form first order high pass filters which limit low frequency response given in Equations 4 and 5.

$$f_{iC} = 1/(2\pi R_i C_i) \quad (4)$$

$$f_{oC} = 1/(2\pi R_L C_o) \quad (5)$$

These values should be chosen based on required frequency response.

### Selection of Input and Output Capacitor Size

Large input and output capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. In many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100 Hz–150 Hz. In this case, using a large input or output capacitor may not increase system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor,  $C_i$ . A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally  $1/2 V_{DD}$ .) This charge comes from the output through the feedback and is apt to create pops once the device is enabled. By minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

### CLICK AND POP CIRCUITRY

The LM4836 contains circuitry to minimize turn-on transients or “click and pops”. In this case, turn-on refers to either power supply turn-on or the device coming out of shutdown mode. When the device is turning on, the amplifiers are internally muted. An internal current source ramps up the voltage of the bypass pin. Both the inputs and outputs ideally track the voltage at the bypass pin. The device will remain in mute mode until the bypass pin has reached its half supply voltage,  $1/2 V_{DD}$ . As soon as the bypass node is stable, the device will become fully operational.

Although the bypass pin current source cannot be modified, the size of the bypass capacitor,  $C_B$ , can be changed to alter the device turn-on time and the amount of “click and pop”. By increasing  $C_B$ , the amount of turn-on pop can be reduced. However, the trade-off for using a larger bypass capacitor is an increase in the turn-on time for the device. Reducing  $C_B$  will decrease turn-on time and increase “click and pop”.

There is a linear relationship between the size of  $C_B$  and the turn-on time. Here are some typical turn-on times for different values of  $C_B$ :

$C_B$	$T_{ON}$
0.01 $\mu\text{F}$	2 ms
0.1 $\mu\text{F}$	20 ms
0.22 $\mu\text{F}$	42 ms
0.47 $\mu\text{F}$	84 ms
1.0 $\mu\text{F}$	200 ms
4.7 $\mu\text{F}$	1sec

In order to eliminate “click and pop”, all capacitors must be discharged before turn-on. Rapid on/off switching of the device or shutdown function may cause the “click and pop” circuitry to not operate fully, resulting in increased “click and pop” noise.

In systems where the line out and headphone jack are the same, the output coupling cap,  $C_o$ , is of particular concern.  $C_o$  is chosen for a desired cutoff frequency with a headphone load. This desired cutoff frequency will change when the headphone load is replaced by a high impedance line out load (powered speakers). The input impedance of headphones are typically between 32 $\Omega$  and 64 $\Omega$ . Whereas, the input impedance of powered speakers can vary from 1k $\Omega$  to 100k $\Omega$ . As the RC time constant of the load and the output coupling capacitor increases, the turn off transients are increased.

To improve click and pop performance in this situation, external resistor R7 should be added as shown in *Figure 3*. The recommended value for R7 is between 150 $\Omega$  to 1k $\Omega$ . To achieve virtually clickless and popless performance  $R7 = 150\Omega$ ,  $C_o = 220\mu\text{F}$ , and  $C_B = 1.0\mu\text{F}$  should be used. Lower values of R7 will result in better click and pop performance. However, it should be understood that lower resistance values of R7 will increase current consumption.

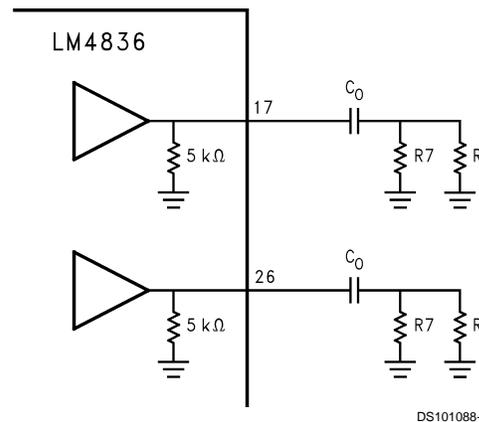


FIGURE 2. Resistor for Varying Output Loads

### DOCKING STATION

In an application such as a notebook computer, docking station or line level outputs may be required. Pin 9 and Pin 13 can drive loads greater than 1k $\Omega$  rail to rail. These pins are tied to the output of the input op-amp to drive powered speakers and other high impedance loads. Output coupling capacitors need to be placed in series with the load. The recommended values of the capacitors are between 0.33 $\mu\text{F}$  to 1.0 $\mu\text{F}$  with the positive side of the capacitors toward the IC. The outputs of the docking station pins cannot be attenu-



## Application Information (Continued)

### BASS BOOST FUNCTION

The Bass Boost Function can be toggled by changing the logic at pin 19. A logic low will switch the power amplifiers to bass boost mode. In bass boost mode the low frequency gain of the amplifier is set by the external capacitor. Whereas a logic high sets the amplifiers to unity gain.

In some cases a designer may want to improve the low frequency response of the bridged amplifier or incorporate a bass boost feature. This bass boost can be useful in systems where speakers are housed in small enclosures. If the designer wishes to disable the bass boost feature, pin 19 can be tied to  $V_{DD}$ .

When bass boost is enabled, the output amplifiers will be internally set at a gain of 2 at low frequencies (gain of 4 in bridged mode). As shown in Figure 2,  $C_{BASS}$  sets the cutoff frequency for the bass boost. At low frequencies the capacitor will be virtually an open circuit. At high frequencies the capacitor will be virtually a short circuit. As a result of this, the gain of the bridge amplifier is increased at low frequencies. A first order pole is formed with a corner frequency at:

$$f_c = 1/(2\pi 10k\Omega C_{BASS})$$

The resulting low frequency differential gain of this bridged amplifier becomes:

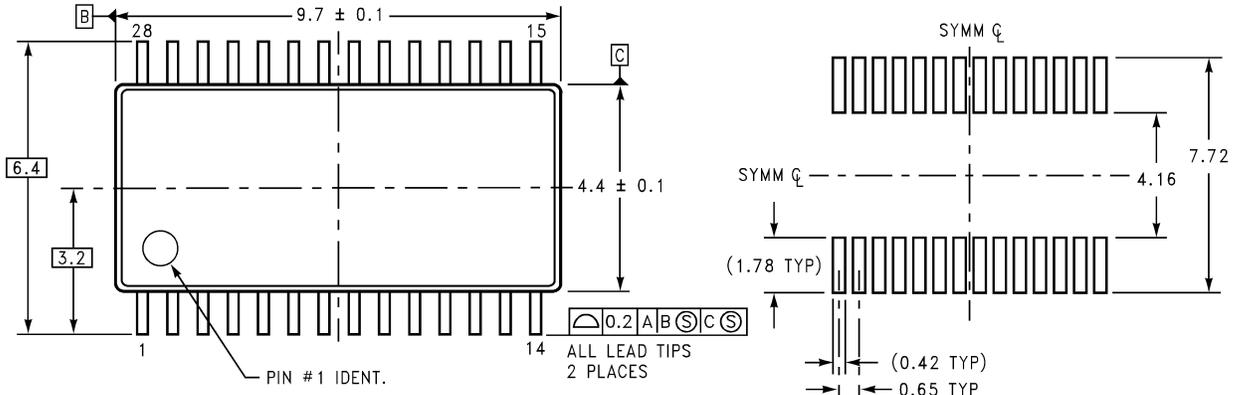
$$2(10k\Omega + 10k\Omega) / 10k\Omega = 4$$

With  $C_{BASS} = 0.1 \mu\text{F}$ , a first order pole is formed with a corner frequency of 160 Hz. The low frequency boost formulas assume that  $C_O$ ,  $C_I$ ,  $f_{IC}$ ,  $f_{OC}$  allow the appropriate low frequency response as explained in the **Proper Selection of External Components** section. See the **Typical Performance Characteristics** section for a graph that includes bass boost performance with various values of  $C_{BASS}$ .

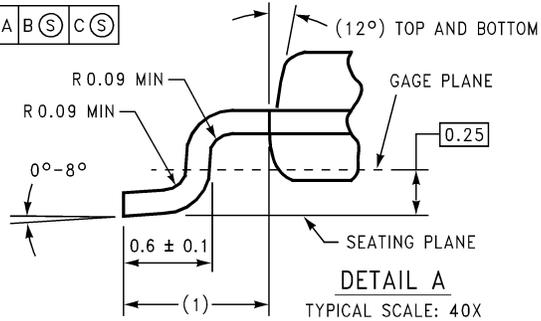
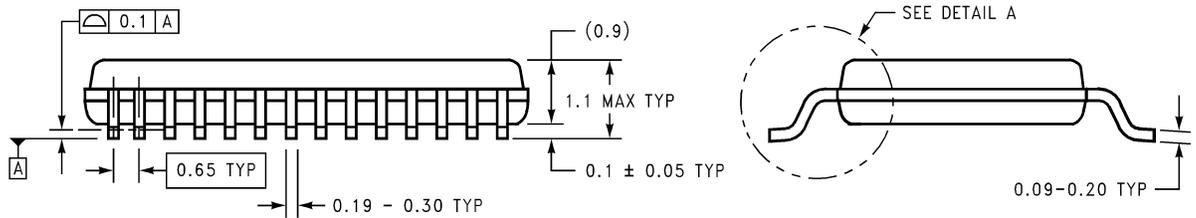
### DC VOLUME CONTROL

The DC voltage at the DC Volume Control pin (pin 5) determines the attenuation of output of the amplifiers. If the DC potential of pin 5 is above 4V (typical 80%  $V_{DD}$ ) the internal amplifiers are set at unity gain. The attenuator range is from 0 dB (pin 5 = 80%  $V_{DD}$ ) to -81 dB (pin 5 = 0V). Any DC voltage greater than 4V (or 80%  $V_{DD}$ ) will result in a gain of unity. Refer to the **Typical Performance Characteristics** for detailed information of the attenuation characteristics of the DC Volume Control pin.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**LAND PATTERN RECOMMENDATION**



MTC28 (REV A)

**TSSOP Package**  
**Order Number LM4836MT**  
**NS Package Number MTC28 for TSSOP**



## Notes

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