LM49100 Boomer® Audio Power Amplifier Series Mono Class AB Audio Sub-System with a True-Ground Headphone Amplifier

Check for Samples: LM49100

FEATURES

- Mono and Stereo Inputs
- Thermal Overload Protection
- True-Ground Headphone Drivers
- I^2C Control Interface
- Input Mute Attenuation
- 2nd Stage Headphone Attenuator
- 32-Step Digital Volume Control
- 10 Operating Modes
- Minimum External Components
- Click and Pop Suppression
- Micro-Power Shutdown
- Available in Space-Saving 3mm x 3mm 25-Bump csBGA Package
- RF Suppression

APPLICATIONS

- Mobile Phones
- PDAs
- Laptops
- Portable Electronics

DESCRIPTION

The LM49100 is a fully integrated audio subsystem capable of delivering 1.275W of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N and with a 5V power supply. The LM49100 also has a stereo true-ground headphone amplifier capable of 50mW per channel of continuous average power into a 32Ω single-ended (SE) loads with 1% THD+N.

The LM49100 has three input channels. One pair of SE inputs can be used with a stereo signal. The other input channel is fully differential and may be used with a mono input signal. The LM49100 features a 32-step digital volume control and ten distinct output modes. The mixer, volume control, and device mode select are controlled through an I^2C compatible interface.

Thermal overload protection prevent the device from being damaged during fault conditions. Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown.

Table 1. Key Specifications

	VALUE	UNIT
Power Output at V_{DD} = 5V: Loudspeaker (LS): R_L = 8Ω, THD+N ≤ 1%	1.275	W
Headphone (V_{DD}HP = 2.8V): R_L = 32Ω, THD+N ≤ 1%	50	mW
Shutdown current	0.01	µA

Typical Application

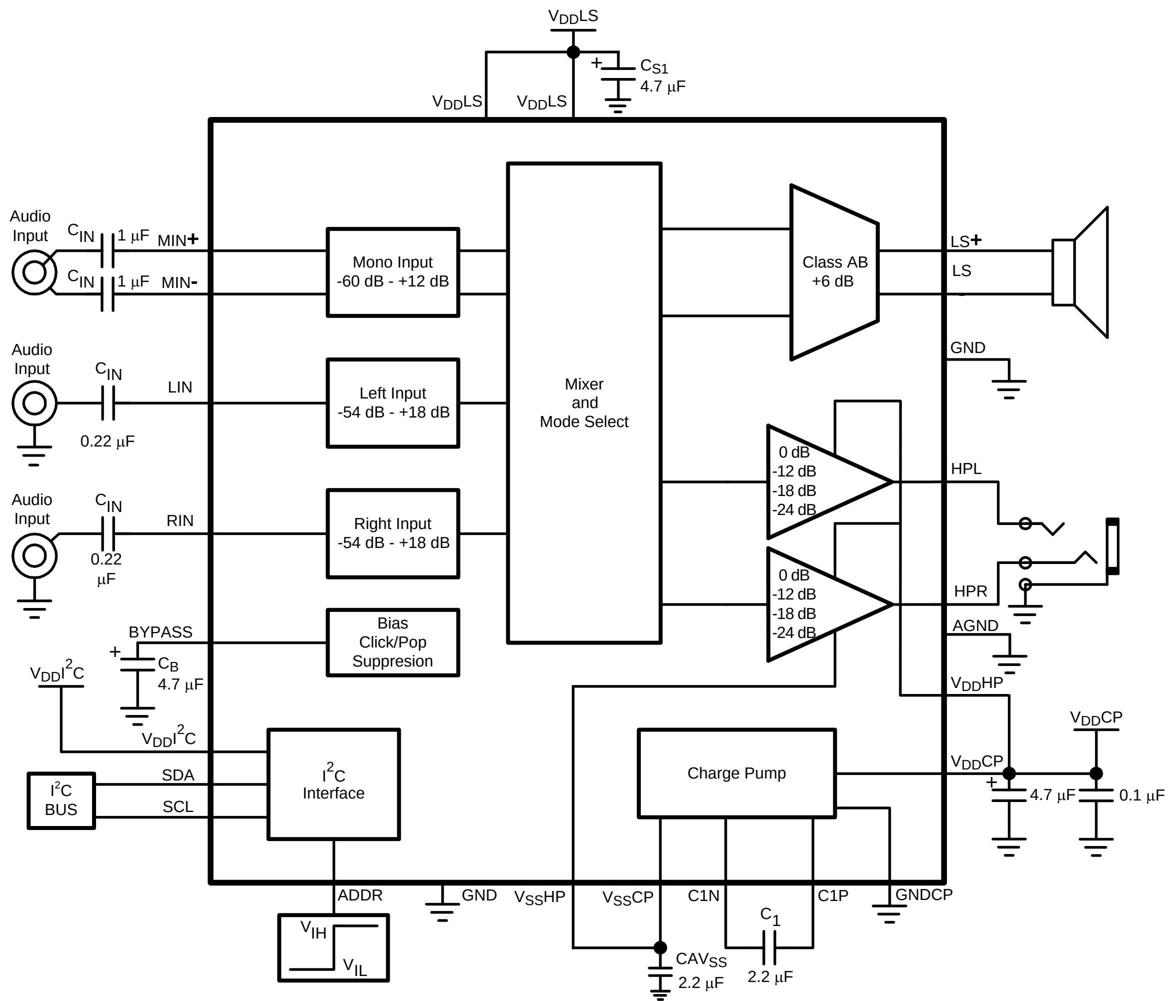


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

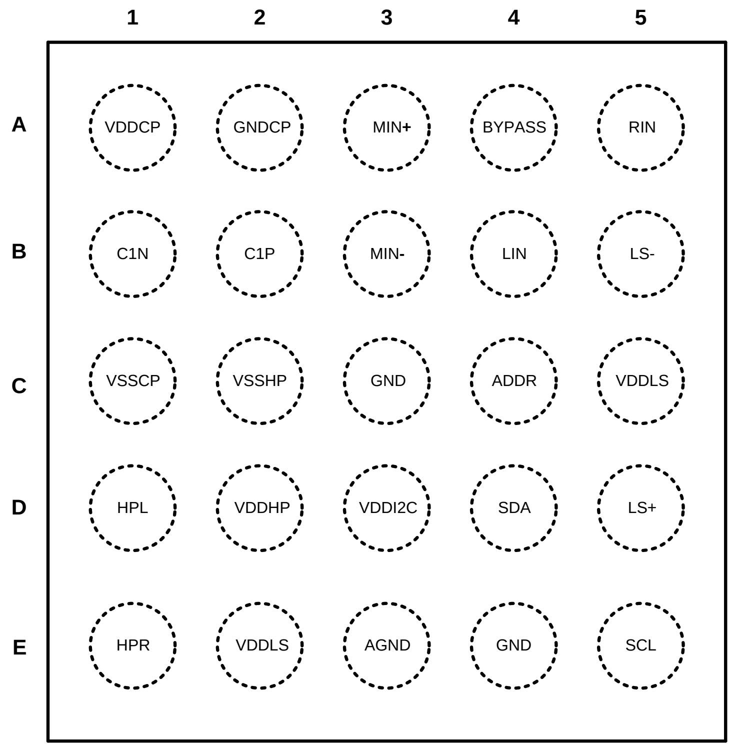


Figure 2. Top View
25-Bump csBGA
3mm × 3mm × 1mm
See NYA0025A Package

BUMP DESCRIPTIONS

Bump	Name	Description
A1	V_{DD}CP	Positive Charge Pump Power Supply
A2	GNDCP	Charge Pump Ground
A3	MIN+	Positive Mono Input
A4	BYPASS	Half-Supply Bypass
A5	RIN	Right Input
B1	C1N	Negative Terminal – Charge Pump Flying Capacitor
B2	C1P	Positive Terminal – Charge Pump Flying Capacitor
B3	MIN-	Negative Mono Input
B4	LIN	Left Input
B5	LS−	Negative Loudspeaker Output
C1	V_{SS}CP	Negative Charge Pump Power Supply
C2	V_{SS}HP	Negative Headphone Power Supply
C3	GND	Ground
C4	ADDR	I^2C Address Identification
C5	V_{DD}LS	Loudspeaker Power Supply
D1	HPL	Left Headphone Output
D2	V_{DD}HP	Positive Headphone Power Supply
D3	$V_{DD}I^2$C	I^2C Power Supply

BUMP DESCRIPTIONS (continued)

Bump	Name	Description
D4	SDA	I^2C Data
D5	LS+	Loudspeaker Output Positive
E1	HPR	Right Headphone Output
E2	$V_{DD}LS$	Loudspeaker Power Supply
E3	AGND	Headphone Signal Ground (See Application Information section).
E4	GND	Ground
E5	SCL	I^2C Clock

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

Supply Voltage (Loudspeaker)	6V
Supply Voltage (Headphone)	3V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (4)	Internally Limited
ESD Susceptibility (5)	2000V
ESD Susceptibility (6)	200V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (GR)	50.2°C/W

(1) All voltages are measured with respect to the GND pin unless other wise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which specify performance limits. This assumes that the device is within the Operating Ratings. Specifications are not for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM49100, see power derating currents for more information.
(5) Human body model, 100 pF discharged through a 1.5kΩ resistor.
(6) Machine Model, 220pF - 240pF discharged through all pins.

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage $V_{DD}LS$	$2.7V \le V_{DD}LS \le 5.5V$
Supply Voltage $V_{DD}HP$	$2.4\ V \le V_{DD}HP \le 2.9V$
I^2C Voltage ($V_{DD}I^2C$)	$1.7V \le V_{DD}I^2C \le 5.5V$ $V_{DD}HP \le V_{DD}LS$ $V_{DD}I^2C \le V_{DD}LS$

Electrical Characteristics $V_{DD}LS = 3.6V$, $V_{DD}HP = 2.8V$ [1][2]

The following specifications apply for all programmable gain set to 0 dB, $C_B = 4.7\mu F$, $R_{L\ (SP)} = 8\Omega$, $R_{L(HP)} = 32\Omega$, f = 1 kHz unless otherwise specified. Limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions			LM49100 Typical [3]	LM49100 Limit [4]	Units (Limits)
I_{DD}	Supply Current	$V_{DD}LS = 3.0V$ $V_{DD}HP = 2.8V$	Modes 1, 3, 5 $V_{IN} = 0V$, No Load		2.9		mA
			Modes 2, 4, 6 $V_{IN} = 0V$, No Load		3.4		mA
			Modes 7, 10, 14 $V_{IN} = 0V$, No Load		4.8		mA
		$V_{DD}LS = 3.6V$ $V_{DD}HP = 2.8V$	Modes 1, 3, 5 $V_{IN} = 0V$, No Load		2.9	4.3	mA (max)
			Modes 2, 4, 6 $V_{IN} = 0V$, No Load		3.5	5.4	mA (max)
			Modes 7, 10, 14 $V_{IN} = 0V$, No Load		4.8	7.4	mA (max)
		$V_{DD}LS = 5.0V$ $V_{DD}HP = 2.8V$	Modes 1, 3, 5 $V_{IN} = 0V$, No Load		3.1		mA
			Modes 2, 4, 6 $V_{IN} = 0V$, No Load		3.6		mA
			Modes 7, 10, 14 $V_{IN} = 0V$, No Load		5.0		mA
I_{SD}	Shutdown Supply Current	Mode 0			0.01	1	µA (max)
V_{OS}	Output Offset Voltage	$V_{IN} = 0V$, Mode 7, Mono			6.0	25	mV (max)
		$V_{IN} = 0V$, Mode 7, Headphone Gain = –24dB			2.2	5.5	mV
		$V_{IN} = 0V$, Mode 7, Headphone Gain = –18dB			2.4		mV (max)
		$V_{IN} = 0V$, Mode 7, Headphone Gain = –12dB			3.2		mV
		$V_{IN} = 0V$, Mode 7, Headphone Gain = 0dB			7	15	mV (max)
P_{OUT}	Output Power	$V_{DD}LS = 3.0V$	LS f = 1kHz	$R_L = 8\Omega$ 1% 10%	425 525		mW mW
			HP f = 1kHz	$R_L = 16\Omega$ 1% 10%	49 69		mW mW
				$R_L = 32\Omega$ 1% 10%	35 44		mW mW
P_{OUT}	Output Power	$V_{DD}LS = 3.6V$	LS f = 1kHz	$R_L = 8\Omega$ 1% 10%	640 790	600	mW (min) mW
			HP f = 1kHz	$R_L = 16\Omega$ 1% 10%	49 72		mW mW
				$R_L = 32\Omega$ 1% 10%	50 62	46	mW (min) mW

(1) All voltages are measured with respect to the GND pin unless other wise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which specify performance limits. This assumes that the device is within the Operating Ratings. Specifications are not for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).

Electrical Characteristics $V_{DD}LS = 3.6V$, $V_{DD}HP = 2.8V$ [(1)(2)] (continued)

The following specifications apply for all programmable gain set to 0 dB, C_B = 4.7µF, $R_{L\ (SP)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1 kHz unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions			LM49100 Typical [(3)]	LM49100 Limit [(4)]	Units (Limits)
P_{OUT}	Output Power	$V_{DD}LS$ = 5.0V	LS f = 1kHz	R_L = 8Ω 1% 10%	1275 1575		mW mW
			HP f = 1kHz	R_L = 16Ω 1% 10%	49 72		mW mW
				R_L = 32Ω 1% 10%	53 62		mW mW
THD+N	Total Harmonic Distortion + Noise	$V_{DD}LS$ = 3.0V	f = 1kHz	Loudspeaker; Mode 1, R_L = 8Ω, P_{OUT} = 215mW	0.05		%
				Headphone; Mode 4, R_L = 32Ω, P_{OUT} = 25mW	0.02		%
THD+N	Total Harmonic Distortion + Noise	$V_{DD}LS$ = 3.6V	f = 1kHz	Loudspeaker; Mode 1, R_L = 8Ω, P_{OUT} = 320mW	0.05		%
				Headphone; Mode 4, R_L = 32Ω, P_{OUT} = 25mW	0.02		%
THD+N	Total Harmonic Distortion + Noise	$V_{DD}LS$ = 5.0V	f = 1kHz	Loudspeaker; Mode 1, R_L = 8Ω, P_{OUT} = 630mW	0.035		%
				Headphone; Mode 4, R_L = 32Ω, P_{OUT} = 25mW	0.02		%
e_N	Noise	A-weighted, 0 dB, inputs terminated to GND, output referred		Headphone			
				Mode 2, 10	12		µV
				Mode 4, 7	13		µV
				Mode 6, 14	16		µV
				Loudspeaker			
				Mode 1	14		µV
				Mode 3, 7, 10, 14	23		µV
				Mode 5	27		µV
T_{ON}	Turn-on Time				26		ms
T_{OFF}	Turn-off Time				1		ms
Z_{IN}	Input Impedance	Maximum gain setting			12.5	10 15	kΩ (min) kΩ (max)
		Maximum attenuation setting			110	90 130	kΩ (min) kΩ (max)

Electrical Characteristics $V_{DD}LS = 3.6V$, $V_{DD}HP = 2.8V$ (1)(2) (continued)

The following specifications apply for all programmable gain set to 0 dB, $C_B = 4.7\mu F$, $R_{L\ (SP)} = 8\Omega$, $R_{L(HP)} = 32\Omega$, f = 1 kHz unless otherwise specified. Limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions		LM49100 Typical (3)	LM49100 Limit (4)	Units (Limits)
A_V	Volume Control	Stereo (Left and Right Channels)	Input referred maximum attenuation	−54	–52 –56	dB (min) dB (max)
			Input referred maximum gain	18	17.5 18.5	dB (min) dB (max)
		Mono	Input referred maximum attenuation	−60	–58 –62	dB (min) dB (max)
			Input referred maximum gain	12	11.5 12.5	dB (min) dB (max)
CMRR	Common Mode Rejection Ratio	Headphone Mode 2, f = 217 Hz, $V_{CM} = 1\ V_{PP}$, $R_L = 32\Omega$		64		dB
		Loudspeaker Mode 1, f = 217 Hz, $V_{CM} = 1\ V_{PP}$, $R_L = 8\Omega$		58		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVpp on V_{DD} LS, output referred, inputs terminated to GND, f = 217Hz				
		LS, Mode 1		90		dB
		LS, Mode 3, 7, 10, 14		78		dB
		LS, Mode 5		77		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVpp on V_{DD} HP, output referred, inputs terminated to GND, f = 217Hz				
		LS, Mode 7, 10, 14		83		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVpp on V_{DD} LS, output referred, inputs terminated to GND, f = 217Hz				
		HP, Mode 2, 10		90		dB
		HP, Mode 4, 7		88		dB
		HP, Mode 6, 14		87		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVpp on V_{DD} HP, output referred, inputs terminated to GND, f = 217Hz				
		HP, Mode 2, 10		83		dB
		HP, Mode 4, 7		83		dB
		HP, Mode 6, 14		80		dB

I^2C (1)(2)

The following specifications apply for V_{DD} = 5.0V and 3.3V, $T_A = 25°C$, $2.2V \le V_{DD}I^2C \le 5.5V$, unless otherwise specified.

Symbol	Parameter	Conditions (3)	LM49100 Typical (4)	LM49100 Limits (2)	Units (Limits)
t_1	I^2C Clock Period			2.5	µs (min)
t_2	I^2C Data Setup Time			100	ns (min)
t_3	I^2C Data Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
t_6	I^2C Data Hold Time			100	ns (min)
V_{IH}	I^2C Input Voltage High			$0.7xV_{DD}I^2C$	V (min)
V_{IL}	I^2C Input Voltage Low			$0.3xV_{DD}I^2C$	V (max)

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which specify performance limits. This assumes that the device is within the Operating Ratings. Specifications are not for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) Limits are specified to AOQL (Average Outgoing Quality Level).
(3) Please refer to Figure 32 (I^2C Timing Diagram).
(4) Typicals are measured at 25°C and represent the parametric norm.

I^2C (1)(2)

The following specifications apply for V_{DD} = 5.0V and 3.3V, T_A = 25°C, 1.7V ≤ $V_{DD}I^2C$ ≤ 2.2V, unless otherwise specified.

Symbol	Parameter	Conditions (3)	LM49100		Units (Limits)
			Typical (4)	Limits (2)	
t_1	I^2C Clock Period			2.5	µs (min)
t_2	I^2C Data Setup Time			250	ns (min)
t_3	I^2C Data Stable Time			0	ns (min)
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition Time			250	ns (min)
t_6	I^2C Data Hold Time			250	ns (min)
V_{IH}	I^2C Input Voltage High			$0.7xV_{DD}I^2C$	V (min)
V_{IL}	I^2C Input Voltage Low			$0.3xV_{DD}I^2C$	V (max)

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which specify performance limits. This assumes that the device is within the Operating Ratings. Specifications are not for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) Limits are specified to AOQL (Average Outgoing Quality Level).
(3) Please refer to Figure 32 (I^2C Timing Diagram).
(4) Typicals are measured at 25°C and represent the parametric norm.

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 3.6V, R_L = 8Ω, P_O = 320mW
BW = 22kHz, LS, Mode 1

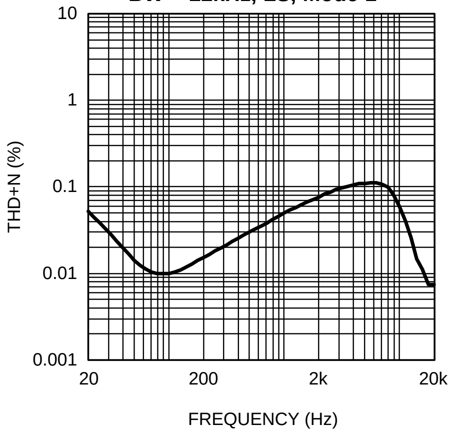


Figure 3.

THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω, P_O = 25mW
HP, BW = 22kHz, Mode 4,7

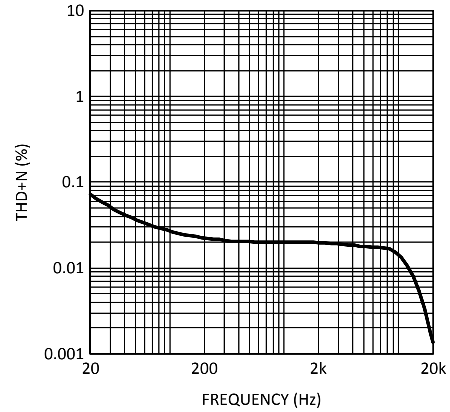


Figure 4.

THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, P_O = 215mW
BW = 22kHz, LS, Mode 1

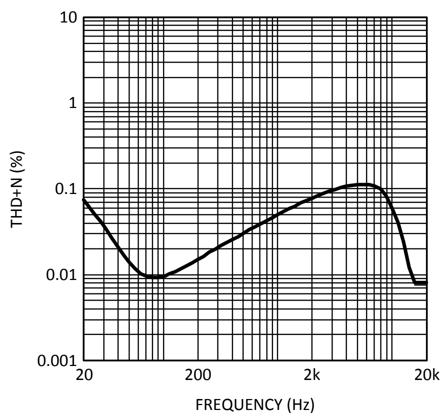


Figure 5.

THD+N vs Frequency
V_{DD} = 3V, R_L = 32Ω, P_O = 25mW
BW = 22kHz, HP, Mode 4, 7

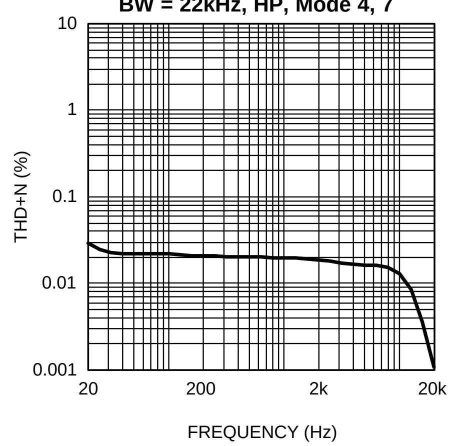


Figure 6.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 630mW
BW = 22kHz, Loudspeaker, Mode 1

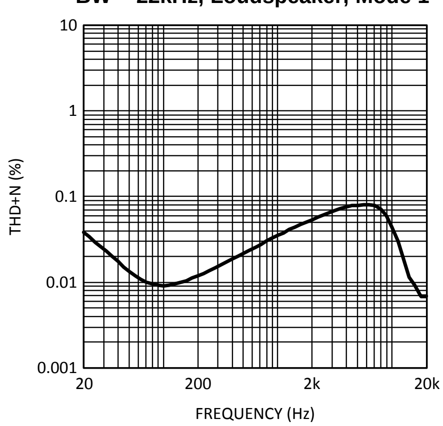


Figure 7.

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 25mW
BW = 22kHz, Headphone, Mode 4,7

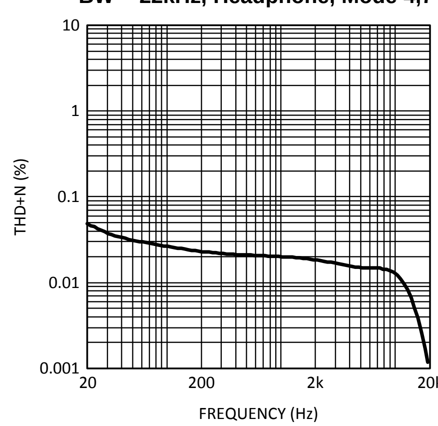


Figure 8.

Typical Performance Characteristics (continued)

THD+N vs Output Power
R_L = 32Ω, f = 1kHz
BW = 22kHz, HP, Mode 4

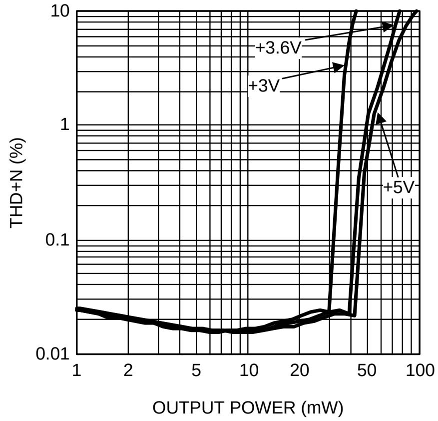


Figure 9.

THD+N vs Output Power
R_L = 8Ω, f = 1kHz
BW = 22kHz, LS, Mode 1

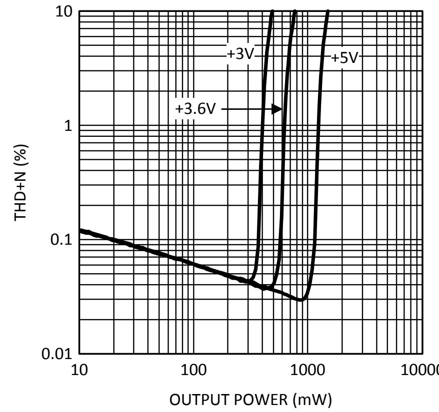


Figure 10.

Output Power vs Supply Voltage
V_{DD}HP = 2.8V, R_L = 8Ω,
f = 1kHz, LS

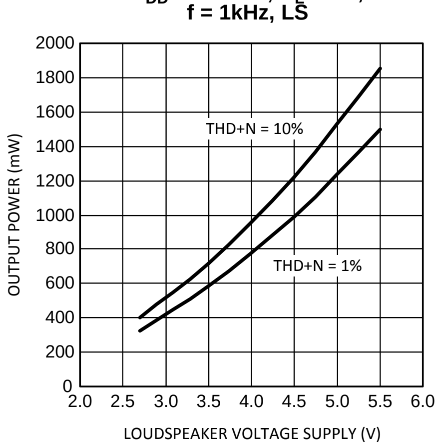


Figure 11.

Output Power vs Supply Voltage
V_{DD}HP = 2.8V, R_L = 32Ω,
f = 1kHz, HP

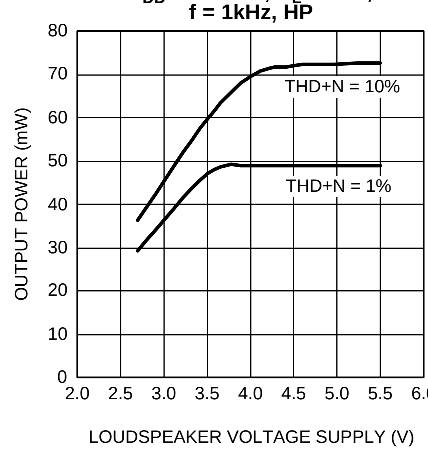


Figure 12.

Power Dissipation vs Output Power
V_{DD} = 3.6V, R_L = 8Ω,
f = 1kHz, Mode 1

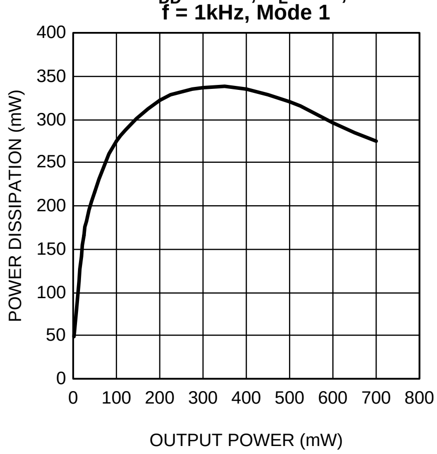


Figure 13.

Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 8Ω,
f = 1kHz, Mode 1

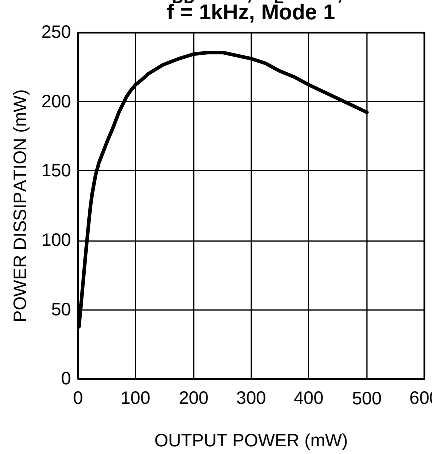


Figure 14.

Typical Performance Characteristics (continued)

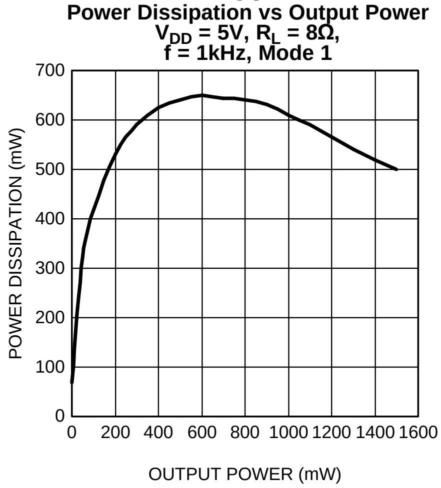


Figure 15.

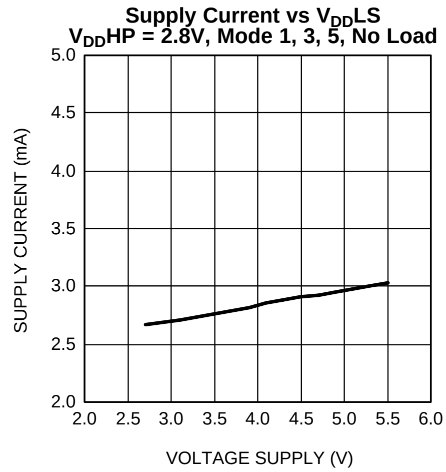


Figure 16.

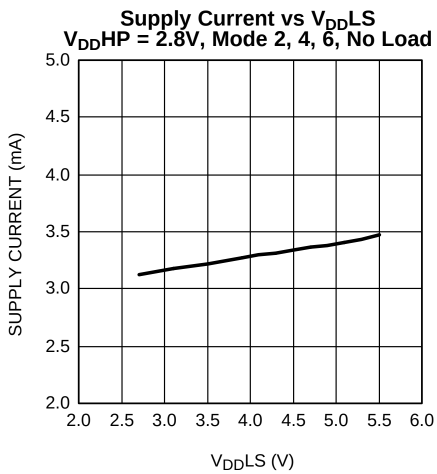


Figure 17.

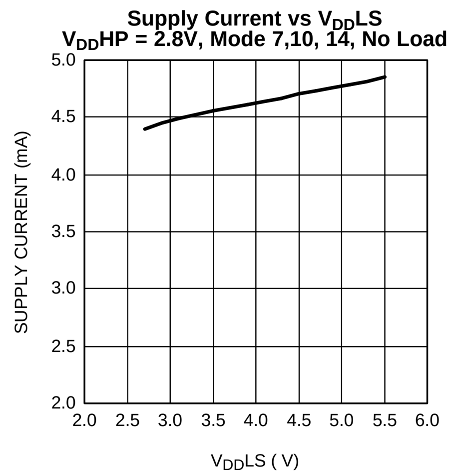


Figure 18.

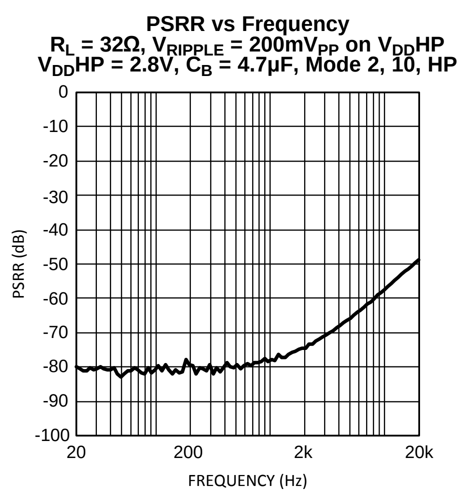


Figure 19.

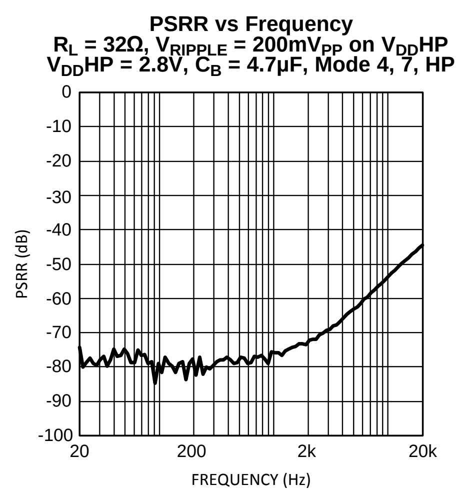


Figure 20.

Typical Performance Characteristics (continued)

PSRR vs Frequency
R_L = 32Ω, V_{RIPPLE} = 200mV_{PP} on V_{DD}HP
V_{DD}HP = 2.8V, C_B = 4.7µF, Mode 6, HP

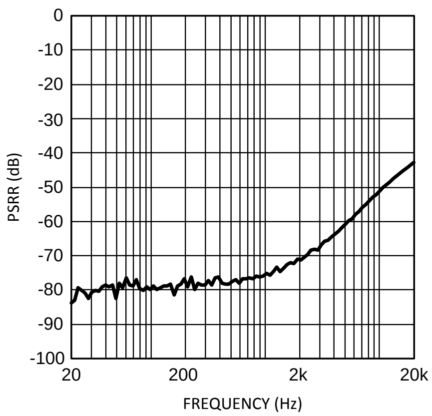


Figure 21.

PSRR vs Frequency
R_L = 32Ω, V_{RIPPLE} = 200mV_{PP} on V_{DD}LS
V_{DD}LS = 3.6V, C_B = 4.7µF, Mode 2, 10, HP

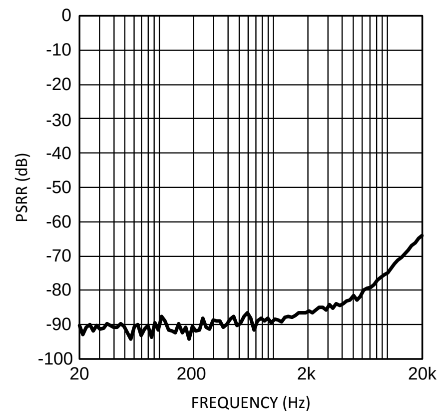


Figure 22.

PSRR vs Frequency
R_L = 32Ω, V_{RIPPLE} = 200mV_{PP} on V_{DD}LS
V_{DD}LS = 3.6V, C_B = 4.7µF, Mode 4, 7, HP

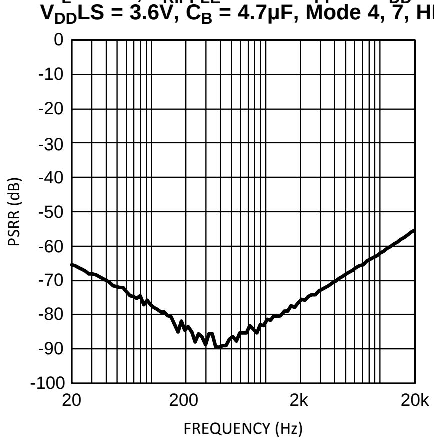


Figure 23.

PSRR vs Frequency
R_L = 32Ω, V_{RIPPLE} = 200mV_{PP} on V_{DD}LS
V_{DD}LS = 3.6V, C_B = 4.7µF, Mode 6, 14, HP

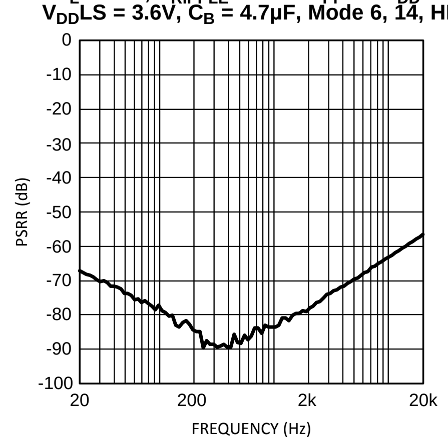


Figure 24.

PSRR vs Frequency
R_L = 8Ω, V_{RIPPLE} = 200mV_{PP} on V_{DD}HP
V_{DD}HP = 2.8V, C_B = 4.7µF, Mode 7, 10, 14, LS+HP

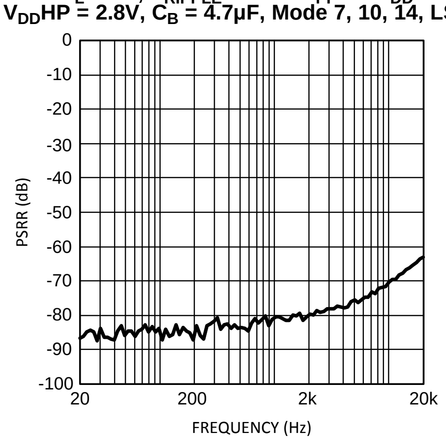


Figure 25.

PSRR vs Frequency
R_L = 8Ω, V_{RIPPLE} = 200mV_{PP} on V_{DD}LS
V_{DD}LS = 3.6V, C_B = 4.7µF, Mode 1, LS

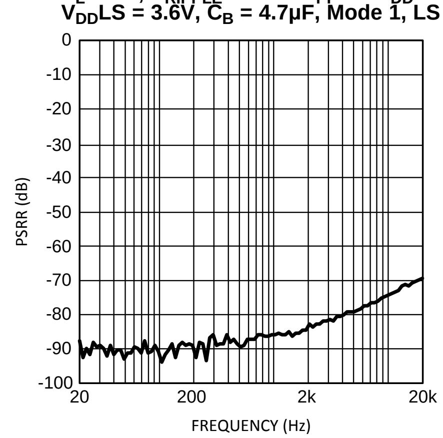


Figure 26.

Typical Performance Characteristics (continued)

PSRR vs Frequency
R_L = 8Ω, V_{RIPPLE} = 200mV_{PP} on V_{DD}LS
V_{DD}LS = 3.6V, C_B = 4.7µF, Mode 7, 10, 14, LS+HP

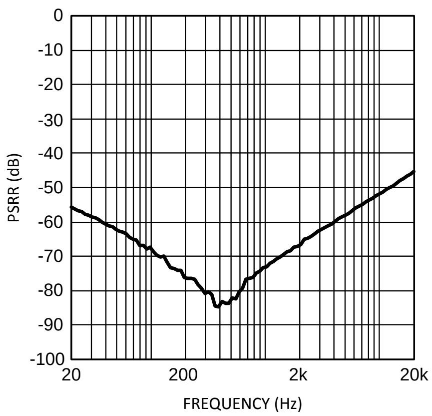


Figure 27.

PSRR vs Frequency
R_L = 8Ω, V_{RIPPLE} = 200mV_{PP} on V_{DD}LS
V_{DD}LS = 3.6V, C_B = 4.7µF, Mode 3, LS

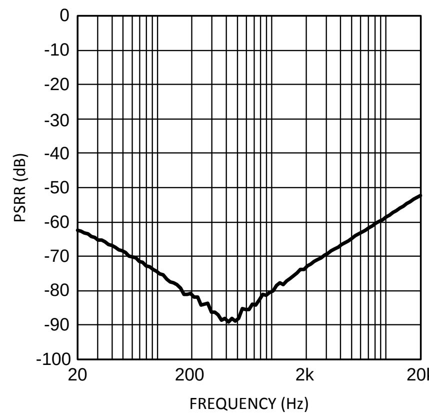


Figure 28.

PSRR vs Frequency
R_L = 8Ω, V_{RIPPLE} = 200mV_{PP} on V_{DD}LS
V_{DD}LS = 3.6V, C_B = 4.7µF, Mode 5, LS

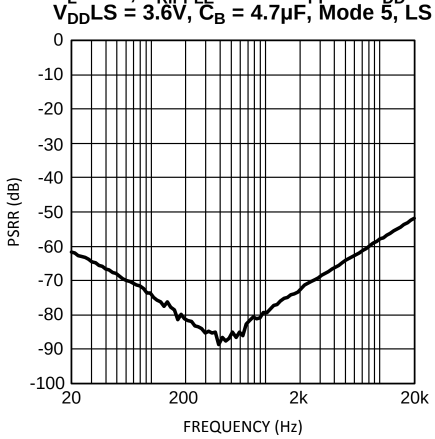


Figure 29.

Crosstalk vs Frequency
P_O = 12mW, f = 1kHz, Mode 4, HP

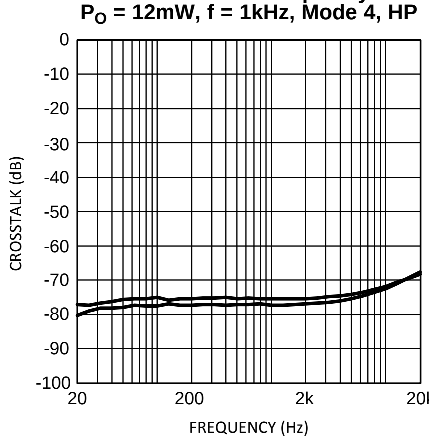


Figure 30.

LM49100 Control Tables

Table 2. I^2C Control Register Table(1)

	D7	D6	D5	D4	D3	D2	D1	D0
Modes Control	0	0	1	1	MC3	MC2	MC1	MC0
HP Volume (Gain) Control	0	1	INPUT_MUTE	0	0	HPR_SD	HPVC1	HPVC0
Mono Volume Control	1	0	0	MV4	MV3	MV2	MV1	MV0
Left Volume (Gain) Control	1	1	0	LV4	LV3	LV2	LV1	LV0
Right Volume (Gain) Control	1	1	1	RV4	RV3	RV2	RV1	RV0

(1) The LM49100 is controlled through an I^2C compatible interface. The I^2C chip address is 0xF8 (ADR pin = 0) or 0xFAh (ADDR pin = 1).

Table 3. Headphone Attenuation Control(1)

Gain Select	HPVC1	HPVC0	Gain, dB
0	0	0	0
1	0	1	−12
2	1	0	−18
3	1	1	−24

(1) The following bits have added for extra headphone output attenuation:

Table 4. Output Mode Selection(1)

Output Mode Number	MC3	MC2	MC1	MC0	Handsfree Mono Output	Right HP Output	Left HP Output
0	0	0	0	0	SD	SD	SD
1	0	0	0	1	$2 \times G_M \times M$	SD	SD
2	0	0	1	0	SD	$G_{HP} \times (G_M \times M)$	$G_{HP} \times (G_M \times M)$
3	0	0	1	1	$2 \times (G_L \times L + G_R \times R)$	SD	SD
4	0	1	0	0	SD	$G_{HP} \times (G_R \times R)$	$G_{HP} \times (G_L \times L)$
5	0	1	0	1	$2 \times (G_L \times L + G_R \times R + G_M \times M)$	SD	SD
6	0	1	1	0	SD	$G_{HP} \times (G_R \times R + G_M \times M)$	$G_{HP} \times (G_L \times L + G_M \times M)$
7	0	1	1	1	$2 \times (G_L \times L + G_R \times R)$	$G_{HP} \times (G_R \times R)$	$G_{HP} \times (G_L \times L)$
10	1	0	1	0	$2 \times (G_L \times L + G_R \times R)$	$G_{HP} \times (G_M \times M)$	$G_{HP} \times (G_M \times M)$
14	1	1	1	0	$2 \times (G_L \times L + G_R \times R)$	$G_{HP} \times (G_R \times R + G_M \times M)$	$G_{HP} \times (G_L \times L + G_M \times M)$

(1) G_L — Left channel gain
G_R — Right channel gain
G_M — Mono channel gain
G_{HP} — Headphone Amplifier gain
R — Right input signal
L — Left input signal
SD — Shutdown
M — Mono input signal

Table 5. Mono/Stereo Left/Stereo Right Input Gain Control

Volume Step	MV4/LV4/RV4	MV3/LV3/RV3	MV2/LV2/RV2	MV1/LV1/RV1	MV0/LV0/RV0	R/L Gain, dB	MonoGain, dB
1	0	0	0	0	0	−54	−60
2	0	0	0	0	1	−47	−53
3	0	0	0	1	0	−40.5	−46.5
4	0	0	0	1	1	−34.5	−40.5
5	0	0	1	0	0	−30.0	−36

Table 5. Mono/Stereo Left/Stereo Right Input Gain Control (continued)

Volume Step	MV4/LV4/RV4	MV3/LV3/RV3	MV2/LV2/RV2	MV1/LV1/RV1	MV0/LV0/RV0	R/L Gain, dB	MonoGain, dB
6	0	0	1	0	1	−27	−33
7	0	0	1	1	0	−24	−30
8	0	0	1	1	1	−21	−27
9	0	1	0	0	0	−18	−24
10	0	1	0	0	1	−15	−21
11	0	1	0	1	0	−13.5	−19.5
12	0	1	0	1	1	−12	−18
13	0	1	1	0	0	−10.5	−16.5
14	0	1	1	0	1	−9	−15
15	0	1	1	1	0	−7.5	−13.5
16	0	1	1	1	1	−6	−12
17	1	0	0	0	0	−4.5	−10.5
18	1	0	0	0	1	−3	−9
19	1	0	0	1	0	−1.5	−7.5
20	1	0	0	1	1	0	−6
21	1	0	1	0	0	1.5	−4.5
22	1	0	1	0	1	3	−3
23	1	0	1	1	0	4.5	−1.5
24	1	0	1	1	1	6	0
25	1	1	0	0	0	7.5	1.5
26	1	1	0	0	1	9	3
27	1	1	0	1	0	10.5	4.5
28	1	1	0	1	1	12	6
29	1	1	1	0	0	13.5	7.5
30	1	1	1	0	1	15	9
31	1	1	1	1	0	16.5	10.5
32	1	1	1	1	1	18	12

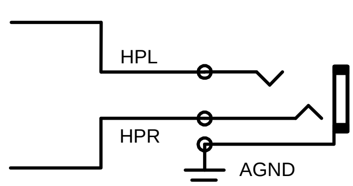
APPLICATION INFORMATION

MINIMIZING CLICK AND POP

To minimize the audible click and pop heard through a headphone, maximize the input signal through the corresponding volume (gain) control registers and adjust the output amplifier gain accordingly to achieve the user's desired signal gain. For example, setting the output of the headphone amplifier to -24dB and setting the input volume control gain to 24dB will reduce the output offset from 7mV (typical) to 2.2mV (typical). This will reduce the audible click and pop noise significantly while maintaining a 0dB signal gain.

SIGNAL GROUND NOISE

The LM49100 has proprietary suppression circuitry, which provides an additional -50dB (typical) attenuation of the headphone ground noise and its incursion into the headphone. For optimum utilization of this feature the headphone jack ground should connect to the AGND (E3) bump.



I^2C PIN DESCRIPTION

SDA: This is the serial data input pin.

SCL: This is the clock input pin.

ADDR: This is the address select input pin.

I^2C COMPATIBLE INTERFACE

The LM49100 uses a serial bus which conforms to the I^2C protocol to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The LM49100's I^2C compatible interface supports standard (100kHz) and fast (400kHz) I^2C modes. In this discussion, the master is the controlling microcontroller and the slave is the LM49100.

The I^2C address for the LM49100 is determined using the ADDR pin. The LM49100's two possible I^2C chip addresses are of the form $111110X_10$ (binary), where $X_1 = 0$, if ADDR pin is logic LOW; and $X_1 = 1$, if ADDR pin is logic HIGH. If the I^2C interface is used to address a number of chips in a system, the LM49100's chip address can be changed to avoid any possible address conflicts.

The bus format for the I^2C interface is shown in Figure 31. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is HIGH. The start signal will alert all devices attached to the I^2C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is HIGH.

After the last bit of the address bit is sent, the master releases the data line HIGH (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM49100 has received the address correctly, then it holds the data line LOW during the clock pulse. If the data line is not held LOW during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM49100.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable HIGH.

After the data byte is sent, the master must check for another acknowledge to see if the LM49100 received the data.

If the master has more data bytes to send to the LM49100, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes HIGH while the clock signal is HIGH. The data line should be held HIGH when not in use.

I^2C INTERFACE POWER SUPPLY PIN ($V_{DD}I^2C$)

The LM49100's I^2C interface is powered up through theV_{DD} I^2C pin. The LM49100's I^2C interface operates at a voltage level set by the V_{DD} I^2C pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I^2C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

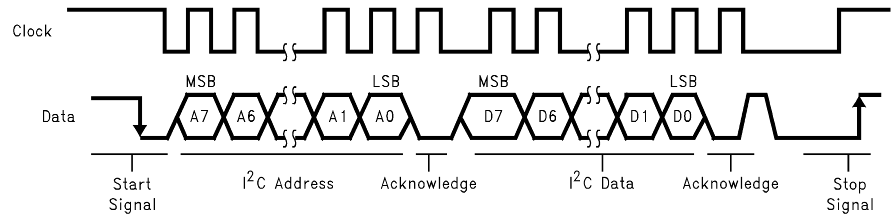


Figure 31. I^2C Bus Format

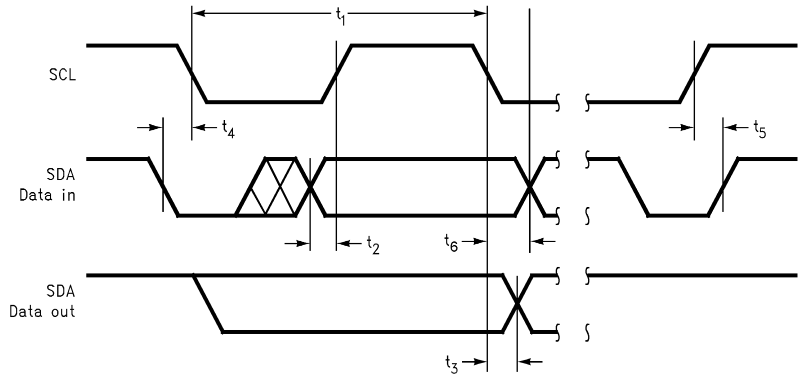


Figure 32. I²C Timing Diagram

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 8Ω LOAD

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by an 8Ω load from 158.3mW to 156.4mW. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

The LM49100 drives a load, such as a loudspeaker, connected between outputs, LS+ and LS-.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between LS- and LS+ and driven differentially (commonly referred to as ”bridge mode”).

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing LS- and LS+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as loudspeakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM49100 has a pair of bridged-tied amplifiers driving a handsfree loudspeaker, LS. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation 1, assuming a 5V power supply and an 8Ω load, the maximum MONO power dissipation is 634mW.

$$P_{DMAX\text{-}LS} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridge Mode} \quad (1)$$

The LM49100 also has a pair of single-ended amplifiers driving stereo headphones, HPR and HPL. The maximum internal power dissipation for HPR and HPL is given by Equation 2. Assuming a 2.8V power supply and a 32Ω load, the maximum power dissipation for L_{OUT} and R_{OUT} is 49mW, or 99mW total.

$$P_{DMAX\text{-}HPL} = 4(V_{DD}HP)^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (2)$$

The maximum internal power dissipation of the LM49100 occurs when all three amplifiers pairs are simultaneously on; and is given by Equation 3.

$$P_{DMAX\text{-}TOTAL} = P_{DMAX\text{-}LS} + P_{DMAX\text{-}HPL} + P_{DMAX\text{-}HPR} \quad (3)$$

The maximum power dissipation point given by Equation 3 must not exceed the power dissipation given by Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (4)$$

The LM49100's T_{JMAX} = 150°C. In the csBGA package, the LM49100's θ_{JA} is 50.2°C/W. At any given ambient temperature T_A, use Equation 4 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 4 and substituting $P_{DMAX\text{-}TOTAL}$ for P_{DMAX} results in Equation 5. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM49100's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX\text{-}TOTAL}\, \theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum mono power dissipation without exceeding the maximum junction temperature is approximately 114°C for the csBGA package.

$$T_{JMAX} = P_{DMAX\text{-}TOTAL}\, \theta_{JA} + T_A \quad (6)$$

Equation 6 gives the maximum junction temperature T_{JMAX}. If the result violates the LM49100's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation 3 is greater than that of Equation 4, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 1µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 4.7µF tantalum bypass capacitor and a parallel 0.1µF ceramic capacitor connected between the LM49100's supply pin and ground. Keep the length of leads and traces that connect capacitors between the LM49100's power supply pin and ground as short as possible.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_{IN} in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the loudspeakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using loudspeakers and headphones with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor (R_i), typical 12.5kΩ, and the input capacitor (C_{IN}) produce a high pass filter cutoff frequency that is found using Equation 7.

$$f_c = 1 / (2\pi R_i C_{IN}) \quad (7)$$

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM49100 settles to quiescent operation, its value is critical when minimizing turn-on pops. Choosing C_B equal to 2.2µF along with a small value of C_i (in the range of 0.1µF to 0.33µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_{IN} no larger than necessary for the desired bandwidth helps minimize clicks and pops. C_B's value should be in the range of 4 to 5 times the value of C_{IN} . This ensures that output transients are eliminated when power is first applied or the LM49100 resumes operation after shutdown.

Demo Board Schematic

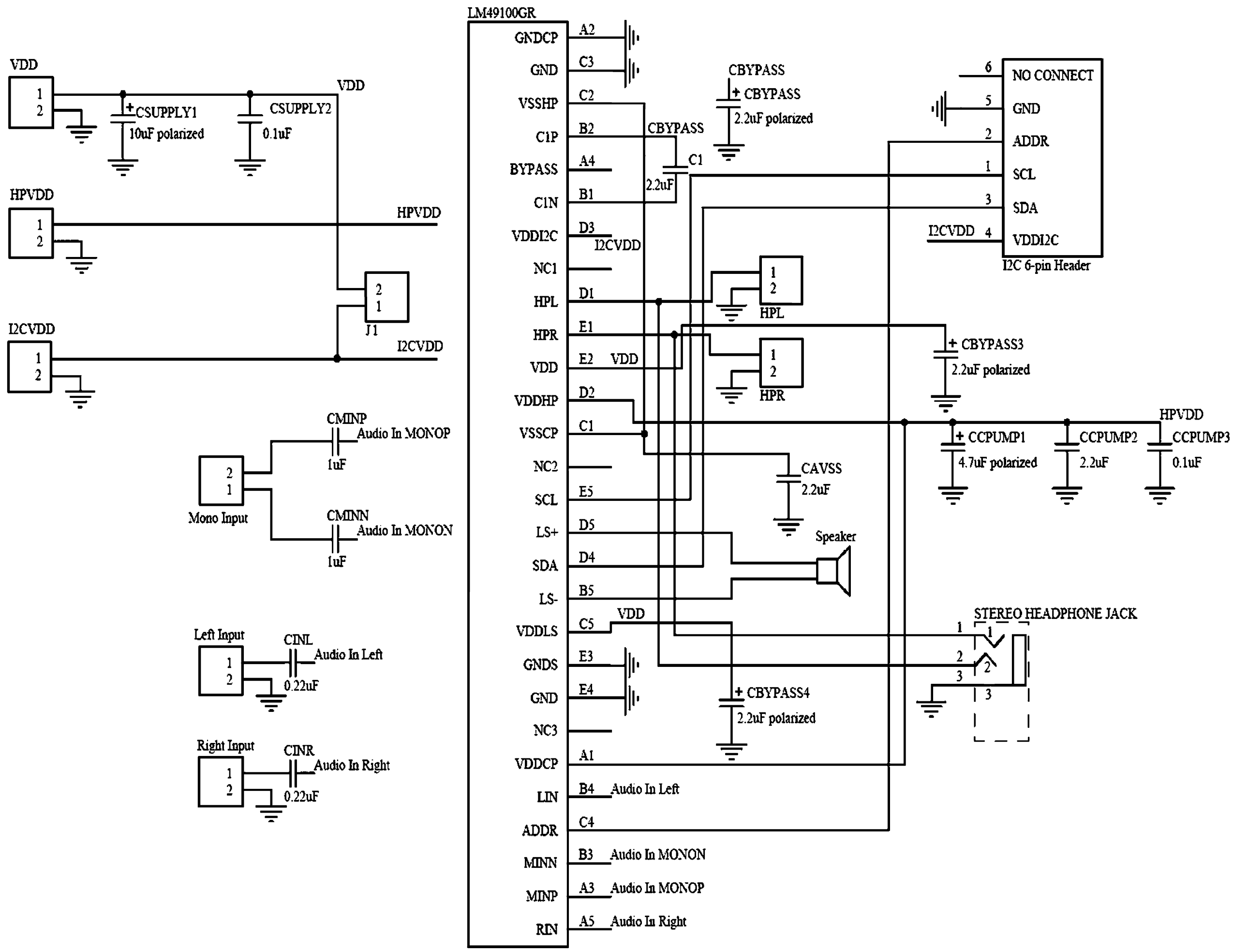


Figure 33. Demo Board Schematic

Demonstration Board Layout

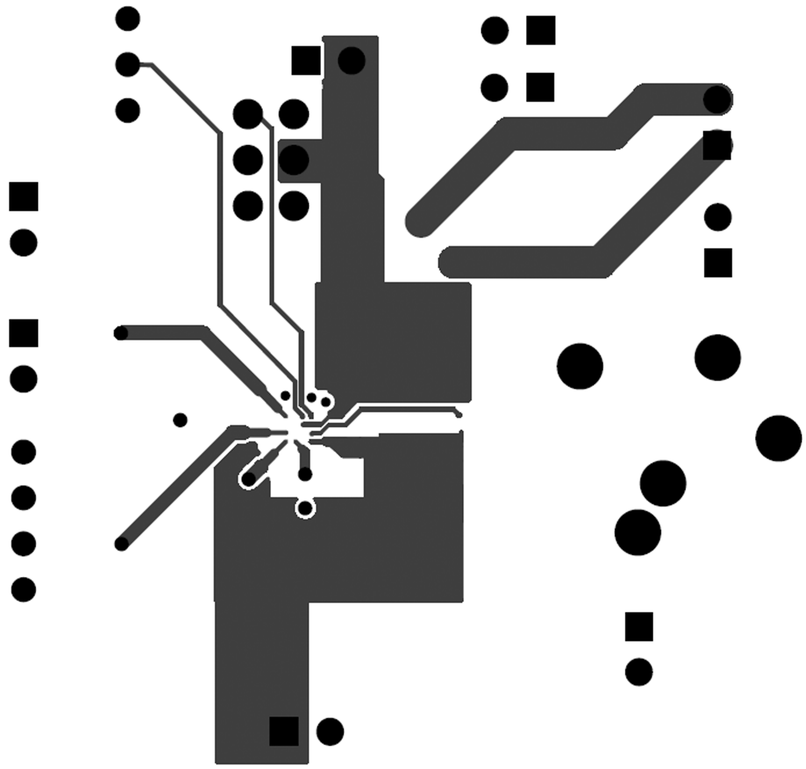


Figure 34. Signal 1 Layer

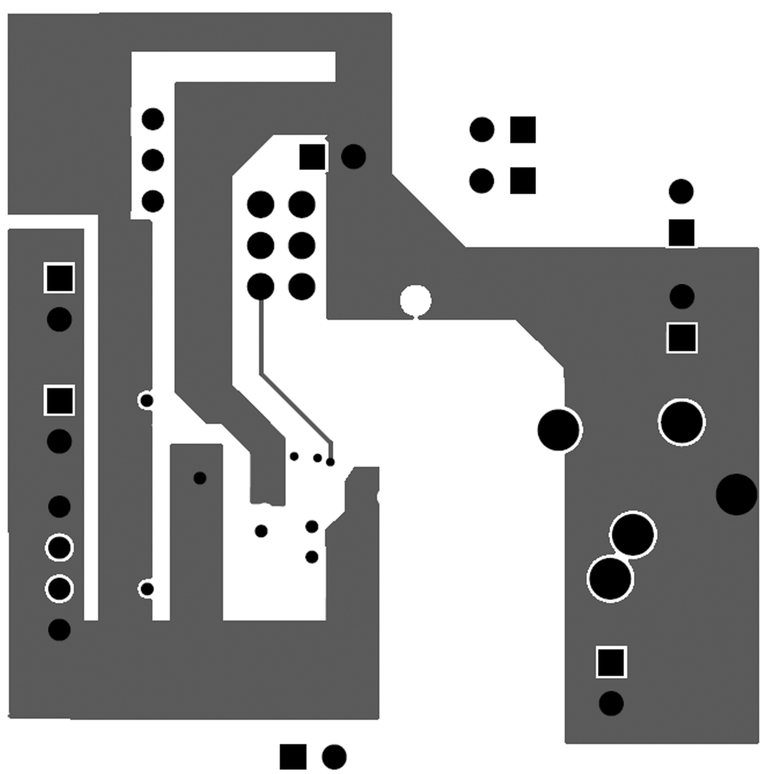


Figure 35. Signal 2 Layer

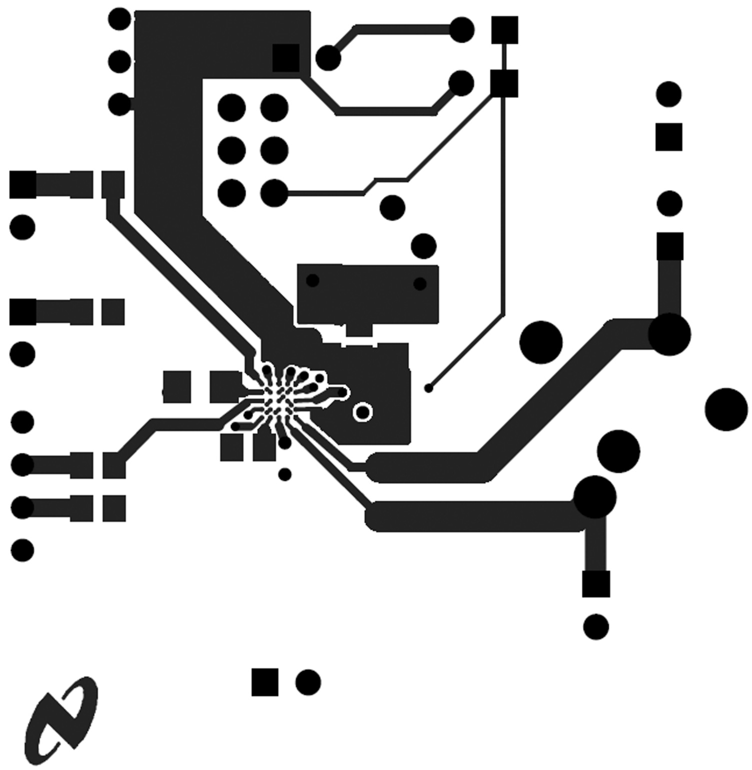


Figure 36. Top Layer

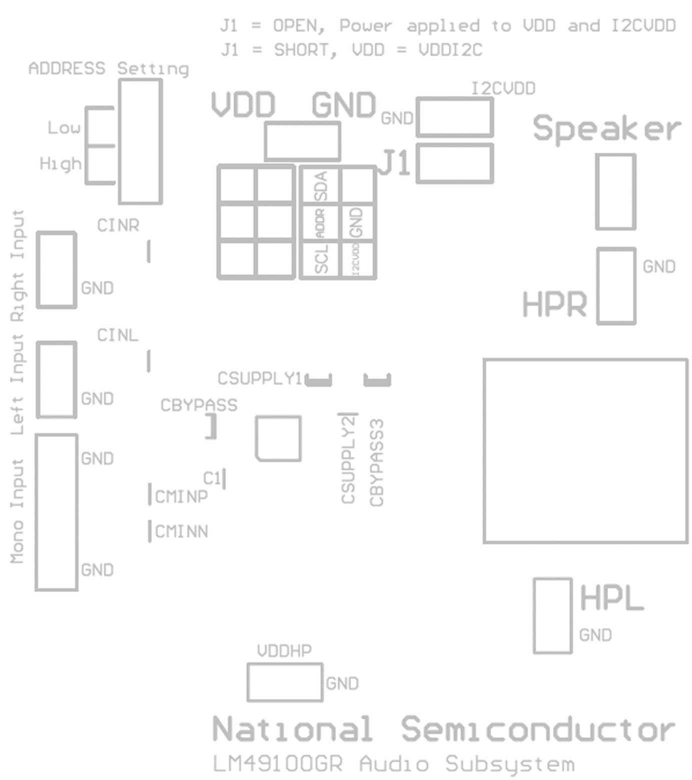


Figure 37. Top Overlay

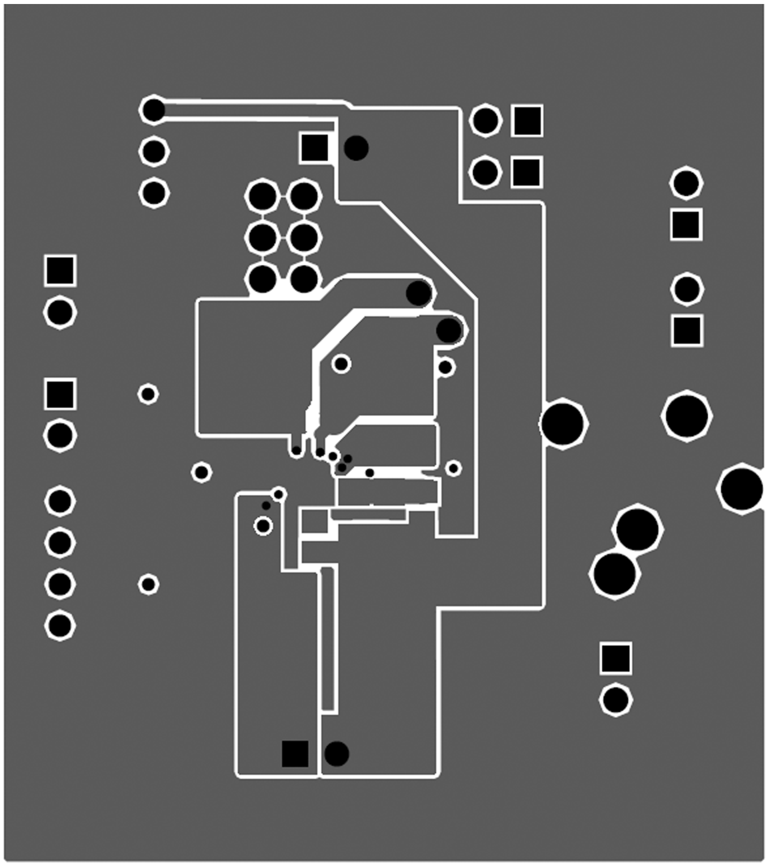


Figure 38. Bottom Layer

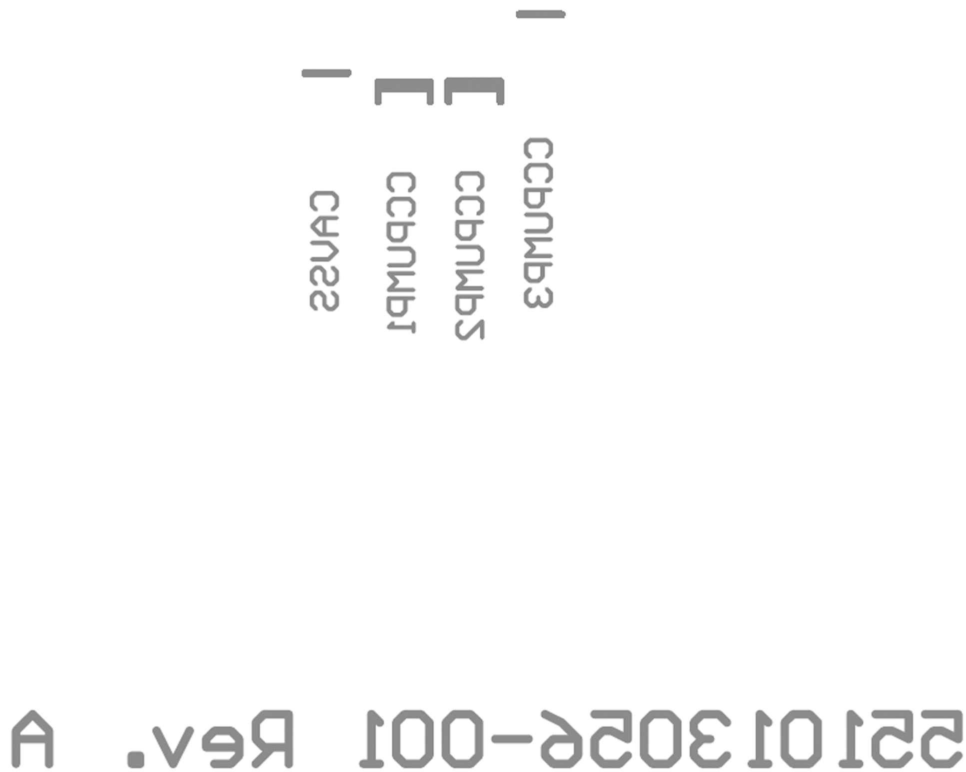


Figure 39. Bottom Overlay

REVISION HISTORY

Rev	Date	Description
1.0	06/21/07	Initial release.
1.1	06/28/07	Changed the mktg outline from TLA25XXX to GRA25A.
1.2	08/09/07	Replaced some curves.
1.3	08/13/07	Changed the f = 1kHz into f = 217Hz (PSRR) in the Electrical Characteristics table.
1.4	08/14/07	Edited Table 2.
1.5	09/18/07	Edited the Schematic Diagram.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM49100GR/NOPB	ACTIVE	csBGA	NYA	25	1000	Green (RoHS & no Sb/Br)	CU SNAGCU	Level-1-260C-UNLIM	-40 to 85	GC9	Samples
LM49100GRX/NOPB	ACTIVE	csBGA	NYA	25	3500	Green (RoHS & no Sb/Br)	CU SNAGCU	Level-1-260C-UNLIM	-40 to 85	GC9	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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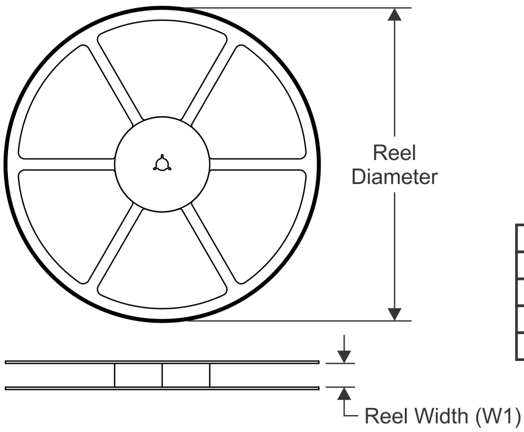
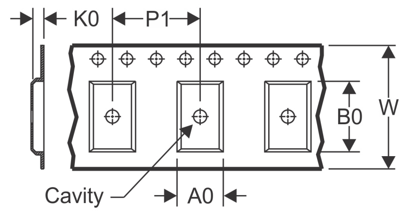
TAPE AND REEL INFORMATION

REEL DIMENSIONS

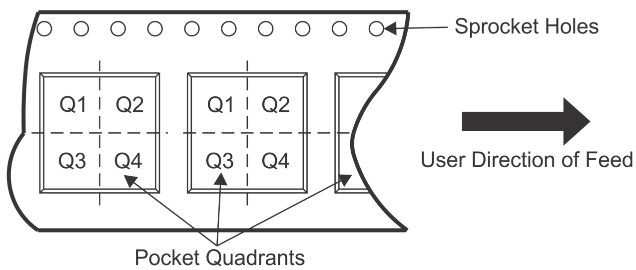


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

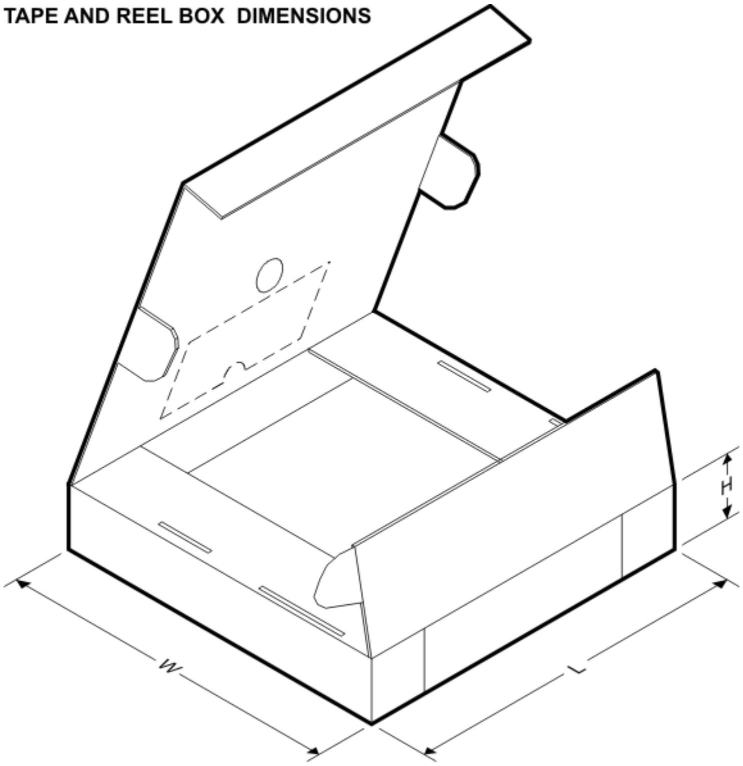
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49100GR/NOPB	csBGA	NYA	25	1000	178.0	12.4	3.3	3.3	1.6	8.0	12.0	Q1
LM49100GRX/NOPB	csBGA	NYA	25	3500	330.0	12.4	3.3	3.3	1.6	8.0	12.0	Q1

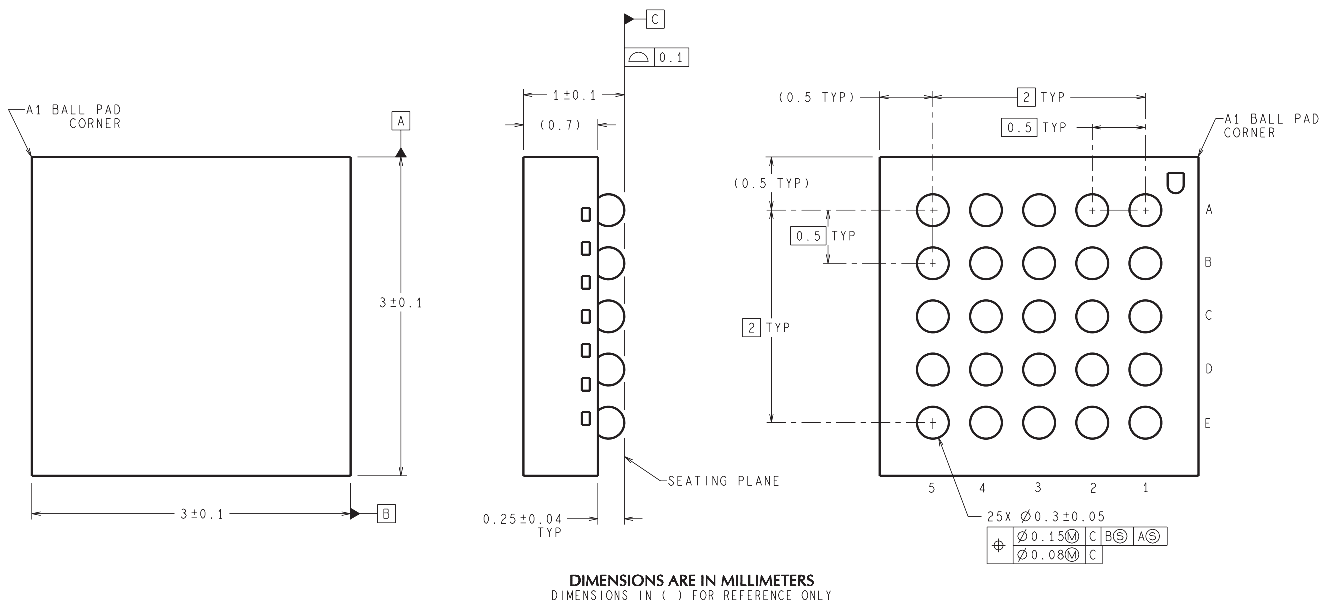
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM49100GR/NOPB	csBGA	NYA	25	1000	203.0	190.0	41.0
LM49100GRX/NOPB	csBGA	NYA	25	3500	349.0	337.0	45.0

NYA0025A



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