LM5100 /LM5101 High Voltage High Side and Low Side Gate Driver

Check for Samples: LM5100, LM5101

FEATURES

- **Drives both a high side and low side N-Channel MOSFET**
- **Independent high and low driver logic inputs (TTL for LM5101 or CMOS for LM5100)**
- **Bootstrap supply voltage range up to 118V DC**
- **Fast propagation times (25 ns typical)**
- **Drives 1000 pF load with 15 ns rise and fall times**
- **Excellent propagation delay matching (3 ns typical)**
- **Supply rail under-voltage lockouts**
- **Low power consumption**
- **Pin compatible with HIP2100/HIP2101**

TYPICAL APPLICATIONS

- **Current Fed push-pull converters**
- **Half and Full Bridge power converters**
- **Synchronous buck converters**
- **Two switch forward power converters**
- **Forward with Active Clamp converters**

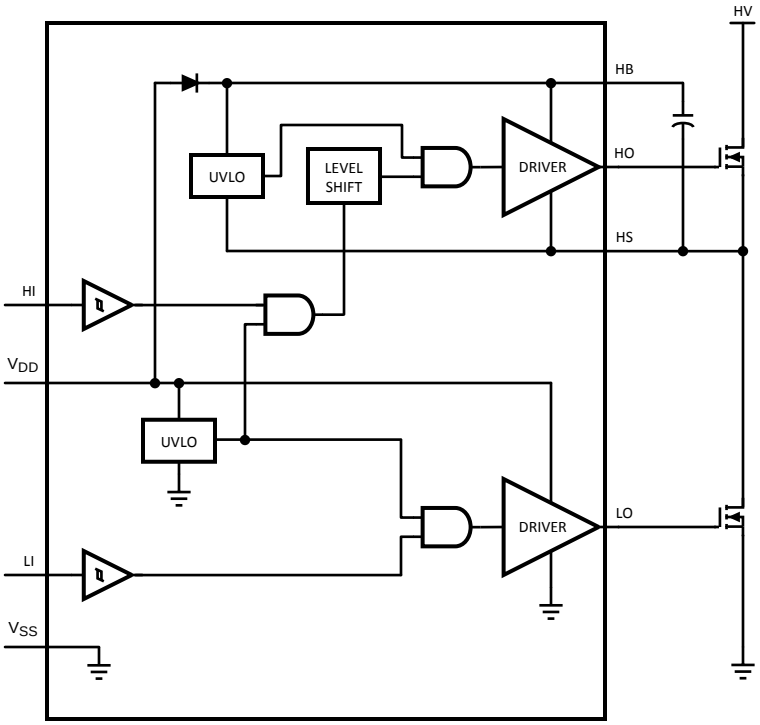
DESCRIPTION

The LM5100/LM5101 High Voltage Gate Drivers are designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The outputs are independently controlled with CMOS input thresholds (LM5100) or TTL input thresholds (LM5101). An integrated high voltage diode is provided to charge the high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails. This device is available in the standard SOIC-8 pin and the LLP-10 pin packages.

Package

- SOIC-8
- LLP-10 (4 mm x 4 mm)

Simplified Block Diagram



Connection Diagrams

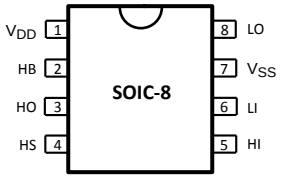


Figure 1. Top View

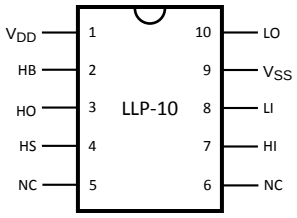


Figure 2. Top View

Table 1. Pin Description

Pin #		Name	Description	Application Information
SO-8	LLP-10			
1	1	V_{DD}	Positive gate drive supply	Locally decouple to V_{SS} using low ESR/ESL capacitor located as close to IC as possible.
2	2	HB	High side gate driver bootstrap rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The Bootstrap capacitor should be place as close to IC as possible.

Table 1. Pin Description (continued)

Pin #		Name	Description	Application Information
SO-8	LLP-10			
3	3	HO	High side gate driver output	Connect to gate of high side MOSFET with a short low inductance path.
4	4	HS	High side MOSFET source connection	Connect to bootstrap capacitor negative terminal and the source of the high side MOSFET.
5	7	HI	High side driver control input	The LM5100 inputs have CMOS type thresholds. The LM5101 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
6	8	LI	Low side driver control input	The LM5100 inputs have CMOS type thresholds. The LM5101 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7	9	V_{SS}	Ground return	All signals are referenced to this ground.
8	10	LO	Low side gate driver output	Connect to the gate of the low side MOSFET with a short low inductance path.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

V_{DD} to V_{SS}	−0.3V to +18V
V_{HB} to V_{HS}	−0.3V to +18V
LI or HI Inputs	−0.3V to V_{DD} +0.3V
LO Output	−0.3V to V_{DD} +0.3V
HO Output	V_{HS} −0.3V to V_{HB} +0.3V
V_{HS} to V_{SS}	−1V to +100V
V_{HB} to V_{SS}	118V
Junction Temperature	+150°C
Storage Temperature Range	−55°C to +150°C
ESD Rating HBM (2)	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

(2) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 500V.

Recommended Operating Conditions

V_{DD}	+9V to +14V
HS	−1V to 100V
HB	V_{HS} +8V to V_{HS} +14V
HS Slew Rate	< 50 V/ns
Junction Temperature	−40°C to +125°C

Electrical Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0V (LM5100)		0.1	**0.2**	mA
		LI = HI = 0V (LM5101)		0.25	**0.4**	
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		1.5	**3**	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.3	**3**	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	V_{HS} = V_{HB} = 100V		0.05	**10**	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.08		mA
INPUT PINS						
V_{IL}	Low Level Input Voltage Threshold (LM5100)		**3**	5.0		V
V_{IL}	Low Level Input Voltage Threshold (LM5101)		**0.8**	1.8		V
V_{IH}	High Level Input Voltage Threshold (LM5100)			5.5	**8**	V
V_{IH}	High Level Input Voltage Threshold (LM5101)			1.8	**2.2**	V
V_{IHYS}	Input Voltage Hysteresis (LM5100)			0.5		V
R_I	Input Pulldown Resistance		**100**	200	**500**	kΩ
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold		**6.0**	6.9	**7.4**	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.6	**0.9**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.85	**1.1**	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.8	**1.5**	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.23	**0.4**	V
V_{OHL}	High-Level Output Voltage	I_{LO} = −100 mA, V_{OHL} = V_{DD}–V_{LO}		0.35	**0.55**	V
I_{OHL}	Peak Pullup Current	V_{LO} = 0V		1.6		A
I_{OLL}	Peak Pulldown Current	V_{LO} = 12V		1.8		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.23	**0.4**	V
V_{OHH}	High-Level Output Voltage	I_{HO} = −100 mA V_{OHH} = V_{HB}–V_{HO}		0.35	**0.55**	V
I_{OHH}	Peak Pullup Current	V_{HO} = 0V		1.6		A
I_{OLH}	Peak Pulldown Current	V_{HO} = 12V		1.8		A
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	SOIC-8		170		°C/W
		LLP-10 (1)		40		

(1) 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

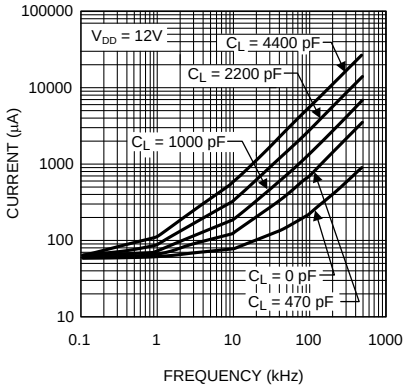
Switching Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO.

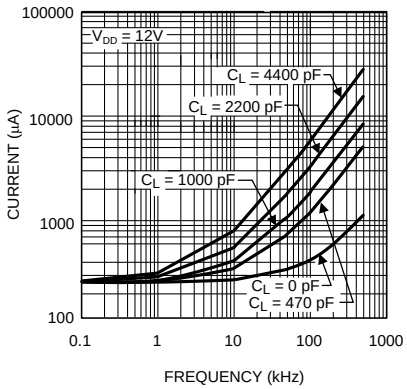
Symbol	Parameter	Conditions	Min	Typ	Max	Units
LM5100						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			24	**45**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			24	**45**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			24	**45**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			24	**45**	ns
t_{MON}	Delay Matching: Lower Turn-On and Upper Turn-Off			2	**10**	ns
t_{MOFF}	Delay Matching: Lower Turn-Off and Upper Turn-On			2	**10**	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15		ns
t_R, t_F	Either Output Rise/Fall Time (3V to 9V)	C_L = 0.1 µF		0.6		µs
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns
LM5101						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			25	**56**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			25	**56**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			25	**56**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			25	**56**	ns
t_{MON}	Delay Matching: Lower Turn-On and Upper Turn-Off			2	**10**	ns
t_{MOFF}	Delay Matching: Lower Turn-Off and Upper Turn-On			2	**10**	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15		ns
t_R, t_F	Either Output Rise/Fall Time (3V to 9V)	C_L = 0.1 µF		0.6		µs
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns

Typical performance Characteristics

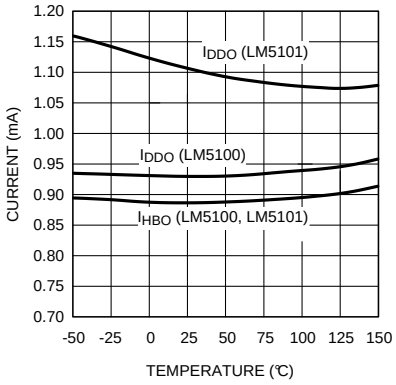
LM5100 I_{DD} vs Frequency



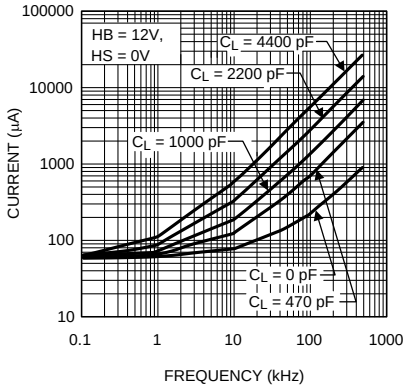
LM5101 I_{DD} vs Frequency



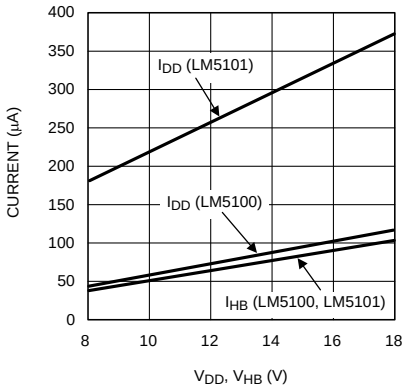
LM5100/LM5101 Operating Current vs Temperature



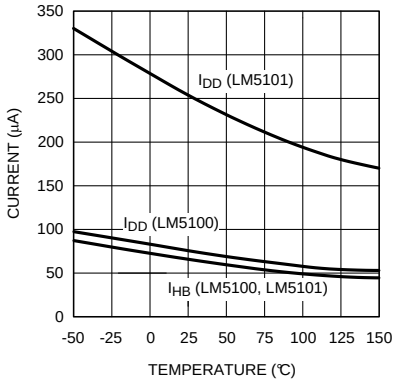
IHB vs Frequency



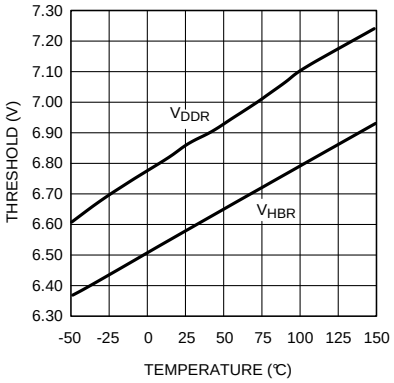
Quiescent Current vs Supply Voltage



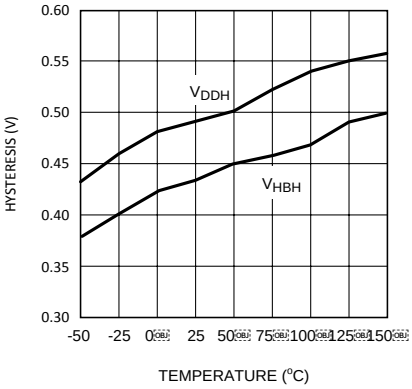
LM5100/LM5101 Quiescent Current vs Temperature



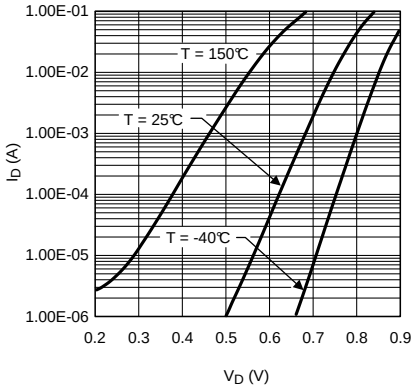
Undervoltage Rising Thresholds vs Temperature



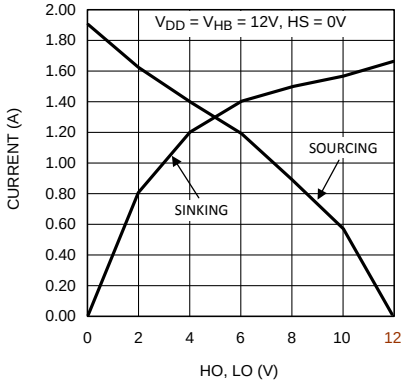
LM5100 Undervoltage Threshold Hysteresis vs Temperature



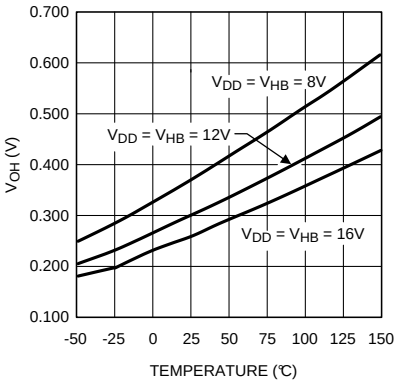
Bootstrap Diode Forward Voltage



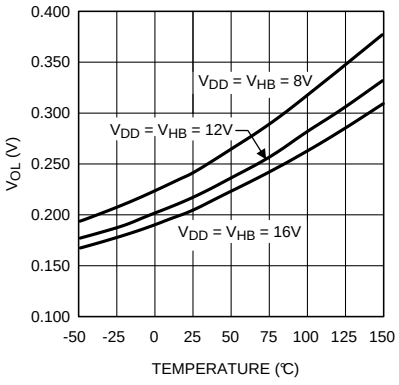
HO and LO Peak Output Current vs Output Voltage



LO and HO Gate Drive—High Level Output Voltage vs Temperature



LO and HO Gate Drive—Low Level Output Voltage vs Temperature



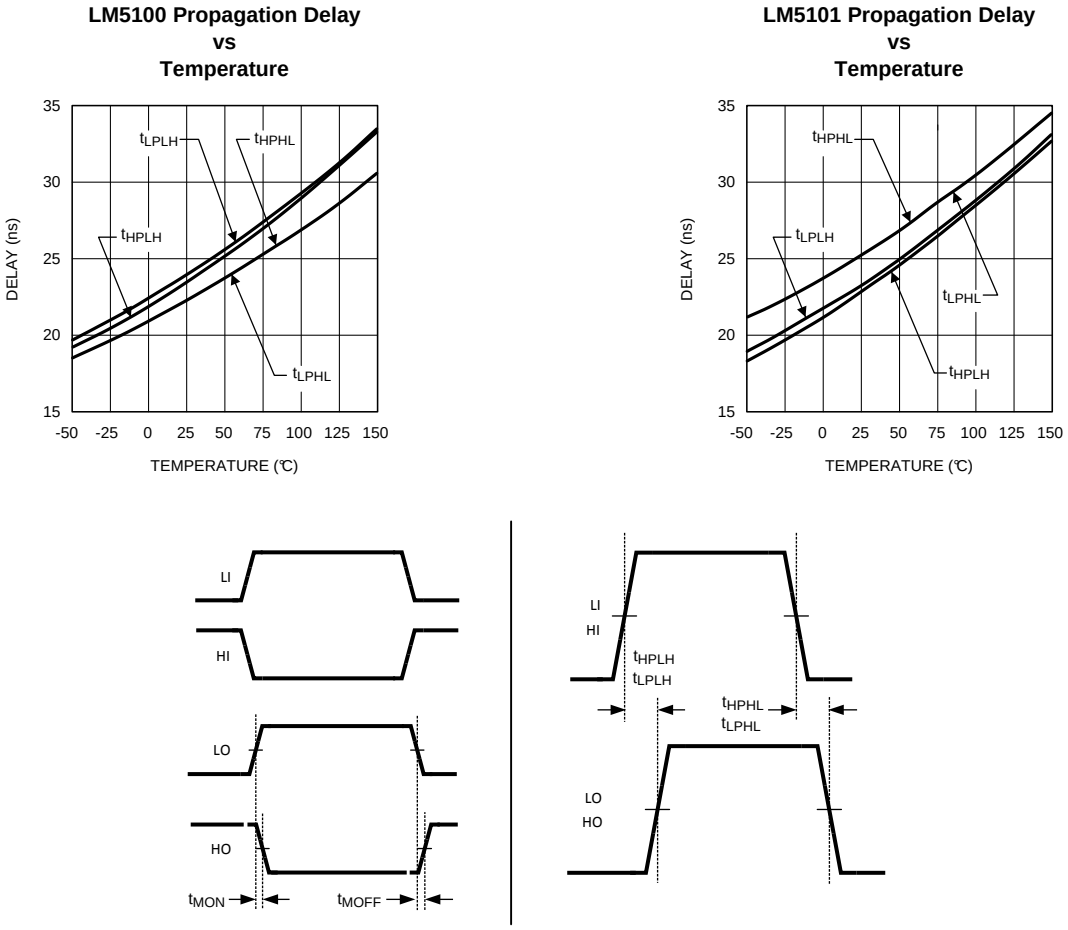


Figure 3. Timing Diagram

Layout Considerations

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR / ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
   - a) The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   - b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2 \quad (1)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

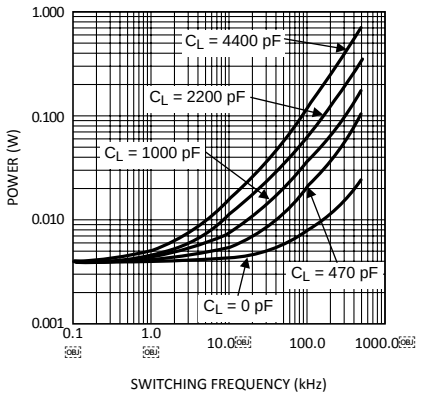


Figure 4. Gate Driver Power Dissipation (LO + HO)
V_{CC} = 12V, Neglecting Diode Losses

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

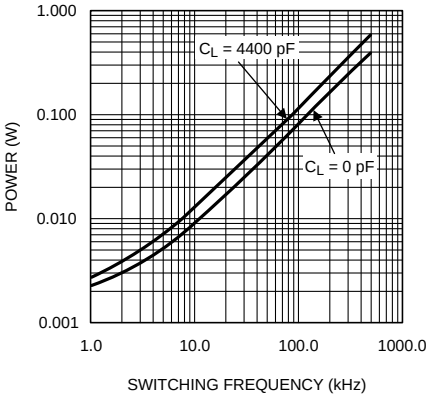


Figure 5. Diode Power Dissipation V_{IN} = 80V

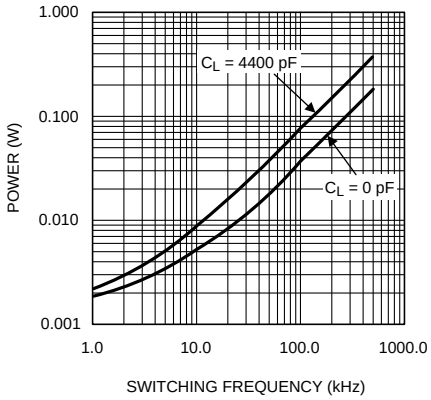


Figure 6. Diode Power Dissipation V_{IN} = 40V

The total IC power dissipation can be estimated from the previous plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel (refer to Figure 7) with the internal bootstrap diode can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.

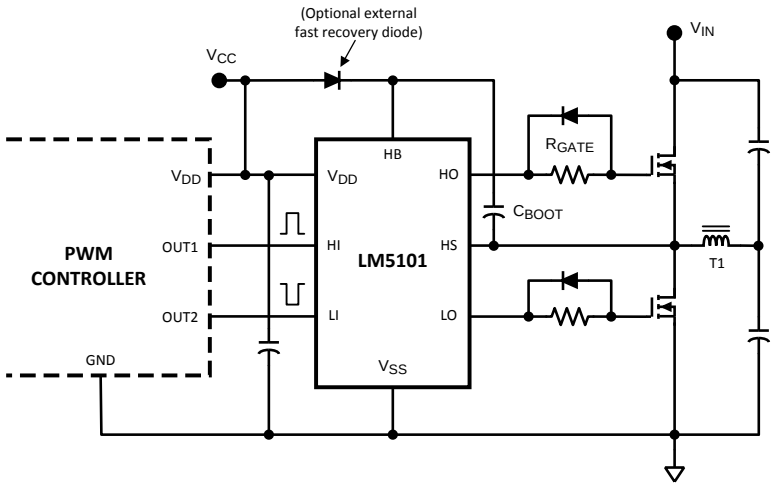


Figure 7. LM5101 Driving MOSFETs Connected in Half-Bridge Configuration

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5100MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI		5100 M	
LM5100MX/NOPB	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5100 M	
LM5101M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI		5101 M	
LM5101M/NOPB	NRND	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5101 M	
LM5101MX/NOPB	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5101 M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

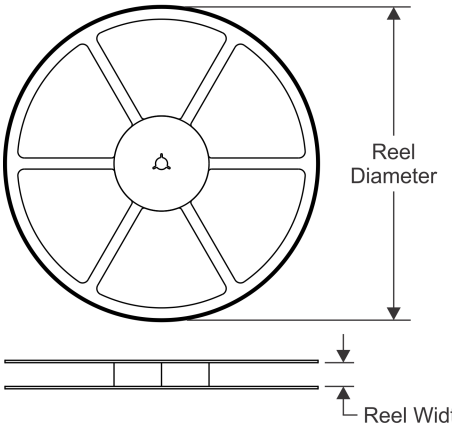
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

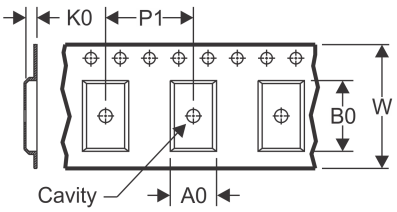
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

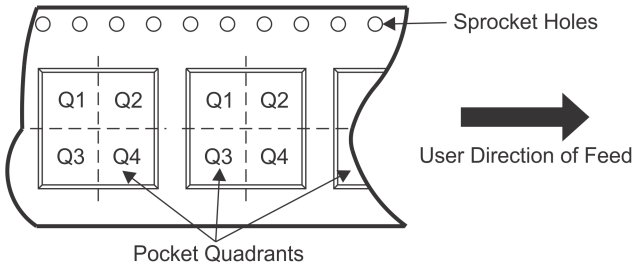


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

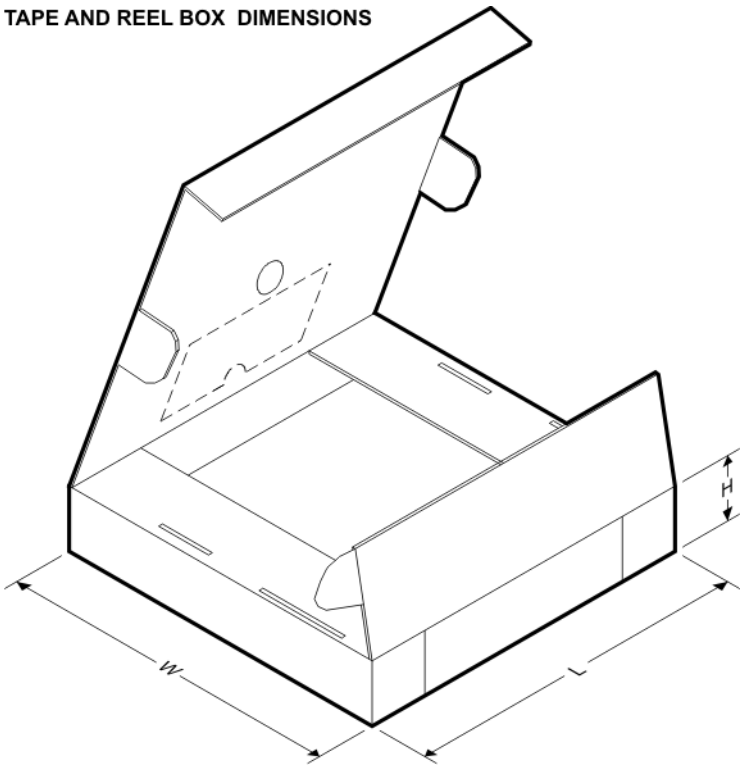
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5100MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

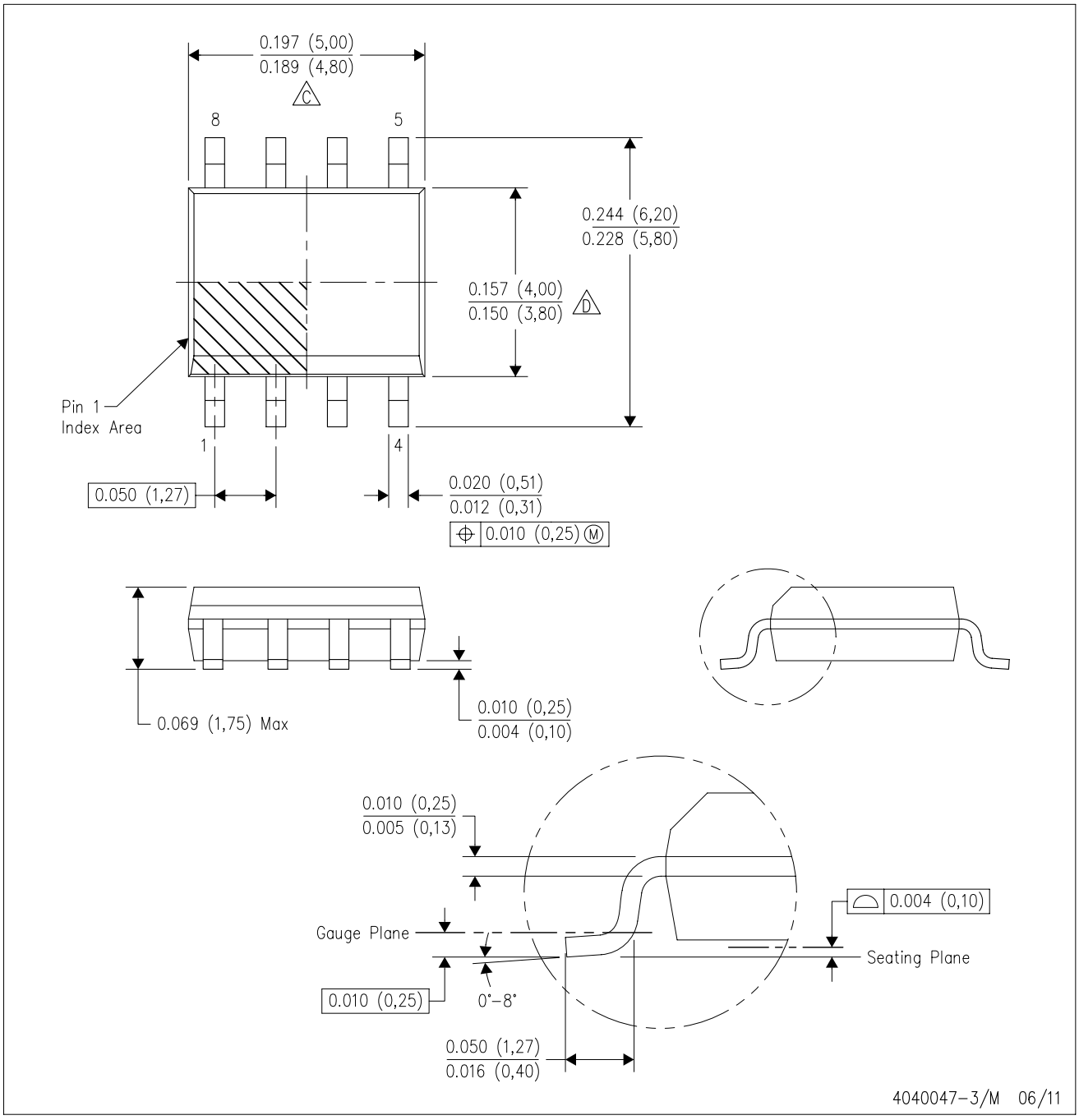
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5100MX	SOIC	D	8	2500	349.0	337.0	45.0
LM5100MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM5101MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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