Sense Amplifiers

LM5520/LM7520 series dual core memory sense amplifiers general description

The devices in this series of dual core sense amplifiers convert bipolar millivolt-level memory sense signals to saturated logic levels. The design employs a common reference input which allows the input threshold voltage level of both amplifiers to be adjusted. Separate strobe inputs provide time discrimination for each channel. Logic inputs and outputs are DTL/TTL compatible. All devices of the series have identical preamplifier configurations, while various logic connections are provided to suit the specific application.

The LM5520/LM7520 has output latch capability and provides sense, strobe, and memory function for two sense lines. The LM5522/LM7522 contains a single open collector output which may be used to expand the number of inputs of the LM5520/LM7520, or to drive an external Memory Data Register (MDR). Intended for small memories, the two channels of the LM5524/LM7524 are independent with two separate outputs. The LM5534/LM7534 is similar to the LM5524/LM7524 but has uncommitted, wire-ORable outputs. The LM5528/LM7528 has the same logic configuration of the LM5524/LM7524 and in addition provides separate low impedance Test Points at each preamplifier output. A similar device having uncommitted, wire-ORable outputs is the LM5538/LM7538.

All critical characteristics are guaranteed for operation within normal system parameter variations of temperature, supply voltages, and output loading.

Features of the series include:

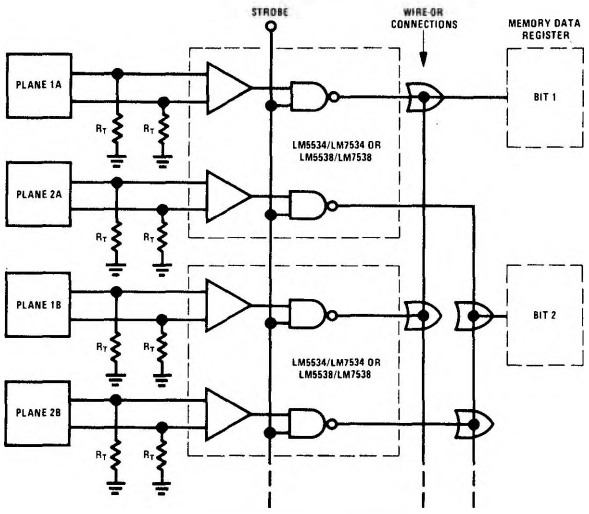
- High speed
- Guaranteed narrow threshold uncertainty including temperature and supply voltage variation
- Adjustable input threshold voltage
- Fast overload recovery times
- Two amplifiers per package
- Molded or cavity dual-in-line package
- Six logic configurations

The part number ending with an even number (e.g., LM5520) designates a tighter guaranteed input threshold uncertainty than the subsequent odd number ending (e.g., LM5521). The remaining specifications for the two are identical. All devices meet or exceed the specifications for the corresponding device (where applicable) in the SN5520/SN7520 series and are pin-for-pin replacements.

absolute maximum ratings

Supply Voltage	±7V
Differential or Reference Input Voltage	±5V
Logic Input Voltage	+5.5V
Operating Temperature Range	
LM55XX	−55°C to +125°C
LM75XX	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

typical application



Expanded Small Memory System

LM5520/LM7520 and LM5521/LM7521 electrical characteristics

LM5520/LM5521: The following apply for $-55°C \leq T_A \leq 125°C$, $V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$. (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF. INPUT	STROBE INPUT	GATE Q INPUT	GATE $\bar{Q}$ INPUT	LOGIC OUTPUT (NOTE 3)	SUPPLY VOLT.	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V		+16 mA(Q)	±5V ±5%	Logic Output <0.4V
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V		−400 μA(Q)	±5V ±5%	Logic Output >2.4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V		+16 mA(Q)	±5V ±5%	Logic Output <0.4V
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V		−400 μA(Q)	±5V ±5%	Logic Output >2.4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5.25V	+5.25V	+5.25V		±5.25V	
LM7520/LM7521: The following apply for $0°C \leq T_A \leq 70°C$, $V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$												
Differential Input Threshold Voltage (V_{TH}) (Note 4)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V		+16 mA(Q)	±5V ±5%	Logic Output <0.4V
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V		−400 μA(Q)	±5V ±5%	Logic Output >2.4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V		+16 mA(Q)	±5V ±5%	Logic Output <0.4V
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V		−400 μA(Q)	±5V ±5%	Logic Output >2.4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5.25V	+5.25V	+5.25V		±5.25V	
LM5520/LM5521: The following apply for $-55°C \leq T_A \leq 125°C$, $V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$ LM7520/LM7521: The following apply for $0°C \leq T_A \leq 70°C$, $V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$												
Differential Input Offset Current		0.5		μA	0V	0V	+5.25V	+5.25V	+5.25V		±5.25V	
Logic "1" Input Voltage												
(Strobes)	2			V	40 mV	20 mV	+2V	+4.75V		−400 μA(Q)	±4.75V	Logic Output >2.4V
(Gate Q)	2			V	40 mV	20 mV	0V	+2V		+16 mA(Q)	±4.75V	Logic Output <0.4V
(Gate $\bar{Q}$)	2			V	40 mV	20 mV	0V	0V	+2V	+16 mA($\bar{Q}$)	±4.75V	Logic Output <0.4V
Logic "0" Input Voltage												
(Strobes)			0.8	V	40 mV	20 mV	+0.8V	+4.75V		+16 mA(Q)	±4.75V	Logic Output <0.4V
(Gate Q)			0.8	V	40 mV	20 mV	0V	+0.8V		−400 μA(Q)	±4.75V	Logic Output >2.4V
(Gate $\bar{Q}$)			0.8	V	40 mV	20 mV	0V	0V	+0.8V	−400 μA($\bar{Q}$)	±4.75V	Logic Output >2.4V
Logic "0" Input Current		−1	−1.6	mA	40 mV	20 mV	+0.4V	+0.4V	+0.4V		±5.25V	Each Input
Logic "1" Input Current		5	40	μA	0V	20 mV	+2.4V	+5.25V	+2.4V		±5.25V	Each Input
(Strobe & Gate $\bar{Q}$)		.02	1	mA	0V	20 mV	+5.25V	+5.25V	+5.25V		±5.25V	Each Input
(Gate Q)		5	40	μA	40 mV	20 mV	+5.25V	+2.4V			±5.25V	
		.02	1	mA	40 mV	20 mV	+5.25V	+5.25V			±5.25V	
Logic "1" Output Voltage												
(Strobe)	2.4	3.9		V	40 mV	20 mV	+2.0V	+5.25V		−400 μA(Q)	±4.75V	
(Gate Q)	2.4	3.9		V	40 mV	20 mV	0V	+0.8V		−400 μA(Q)	±4.75V	
(Gate $\bar{Q}$)	2.4	3.9		V	40 mV	20 mV	+4.75V	0V	+0.8V	−400 μA($\bar{Q}$)	±4.75V	
Logic "0" Output Voltage												
(Strobe)		0.25	0.40	V	40 mV	20 mV	+0.8V	+4.75V		+16 mA(Q)	±4.75V	
(Gate Q)		0.25	0.40	V	0V	20 mV	0V	+2V		+16 mA(Q)	±4.75V	
(Gate $\bar{Q}$)		0.25	0.40	V	0V	20 mV	0V	0V	+2V	+16 mA($\bar{Q}$)	±4.75V	
Q Output Short Circuit Current	−3	−4	−5	mA	0V	20 mV	0V	0V		0 V(Q)	±5.25V	
$\bar{Q}$ Output Short Circuit Current	−2.1	−2.8	−3.5	mA	0V	20 mV	0V	0V	0V	0 V($\bar{Q}$)	±5.25V	
V+ Supply Current		21	35	mA	0V	20 mV	0V	0V	0V		±5.25V	
V− Supply Current		−13	−18	mA	0V	20 mV	0V	0V	0V		±5.25V	

Note 1: For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5520 and LM5521 are guaranteed the same as LM7520 and LM7521, respectively.

Note 2: Limits in parentheses pertain to LM5521, other limits pertain to LM5520.

Note 3: Q or $\bar{Q}$ in parentheses indicate Q or $\bar{Q}$ logic output, respectively.

Note 4: Limits in parentheses pertain to LM7521, other limits pertain to LM7520.

Note 5: Positive current is defined as current into the referenced pin.

Note 6: Pin 1 to have ≥100 pF capacitor connected to ground.

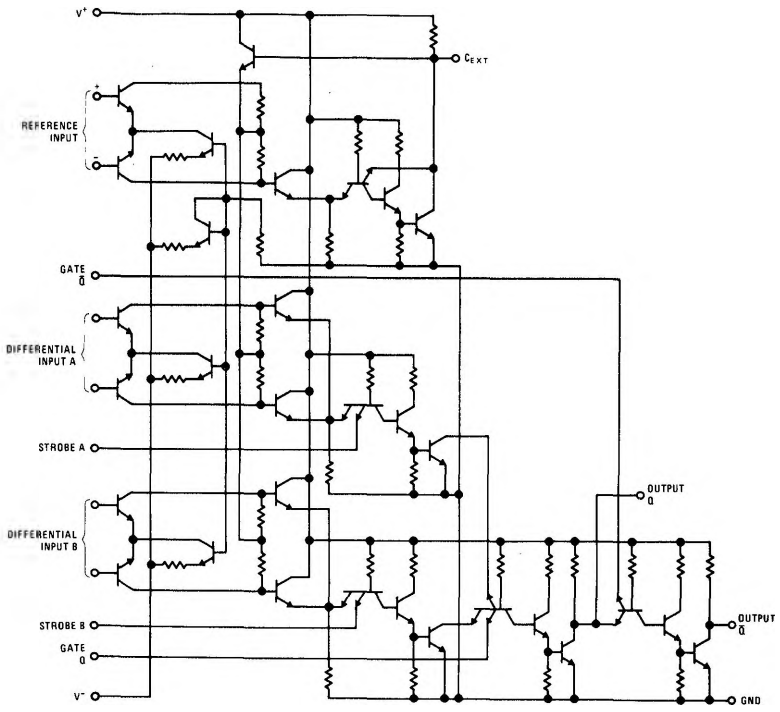
LM5520/LM7520 and LM5521/LM7521
electrical characteristics

LM5520/LM5521 and LM7520/LM7521: The following apply for $T_A = 25^\circ C$, $V^+ = 5V$, $V^- = -5V$

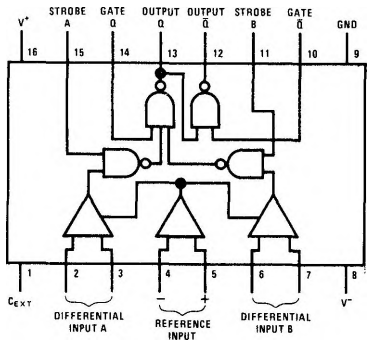
PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS				
					DIFF. INPUT	REF. INPUT	STROBE AND GATE INPUTS	Q LOGIC OUTPUT	AC TEST CIRCUIT
AC Common-Mode Input Firing Voltage		±2.5		V	PULSE	20 mV	+5V	SCOPE	
Propagation Delays									
Differential Input to Logical "1" Q Output		20	40	ns		20 mV			1
Differential Input to Logical "0" Q Output		28		ns		20 mV			1
Differential Input to Logical "1" $\bar{Q}$ Output		36		ns		20 mV			1
Differential Input to Logical "0" $\bar{Q}$ Output		28	55	ns		20 mV			1
Strobe Input to Logical "1" Q Output		10	30	ns		20 mV			1
Strobe Input to Logical "0" Q Output		20		ns		20 mV			1
Strobe Input to Logical "1" $\bar{Q}$ Output		33		ns		20 mV			1
Strobe Input to Logical "0" $\bar{Q}$ Output		16	55	ns		20 mV			1
Gate Q Input to Logical "1" Q Output		12	20	ns		20 mV			2
Gate Q Input to Logical "0" Q Output		6		ns		20 mV			2
Gate Q Input to Logical "1" $\bar{Q}$ Output		17		ns		20 mV			2
Gate Q Input to Logical "0" $\bar{Q}$ Output		19	30	ns		20 mV			2
Gate $\bar{Q}$ Input to Logical "1" $\bar{Q}$ Output		12		ns		20 mV			2
Gate $\bar{Q}$ Input to Logical "0" $\bar{Q}$ Output		6	20	ns		20 mV			2
Diff. Input Overload Recovery Time		10		ns					
Common-Mode Input Overload Recovery Time		5		ns					
Min. Cycle Time		200		ns					

LM5520/LM7520 and LM5521/LM7521

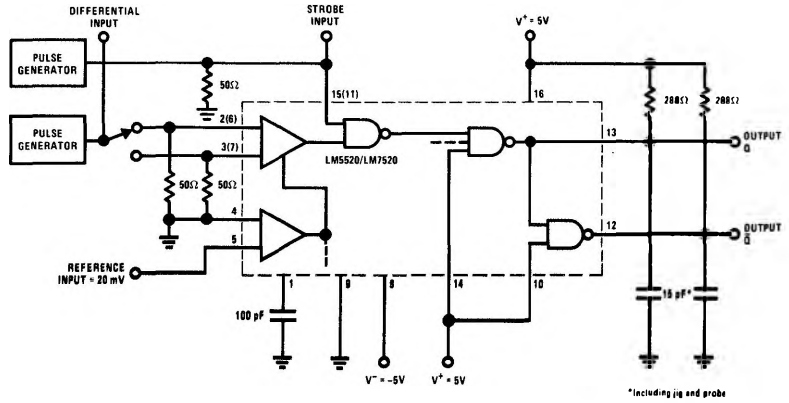
schematic diagram



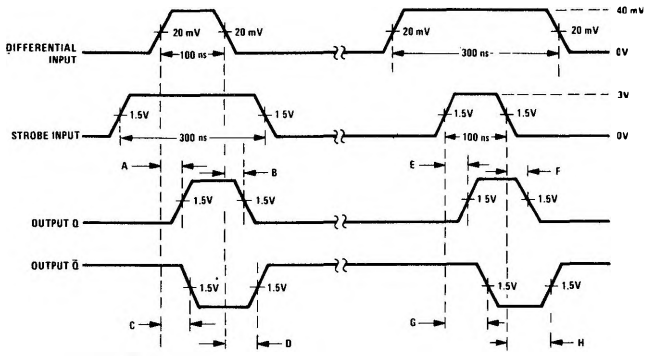
connection diagram



LM5520/LM7520 and LM5521/LM7521
AC test circuit (1)

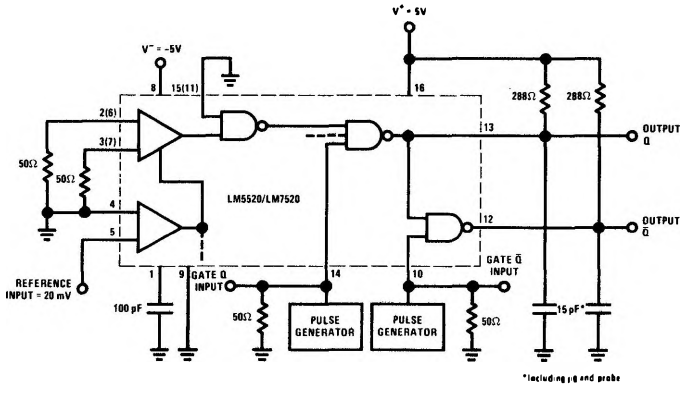


voltage waveforms (1)

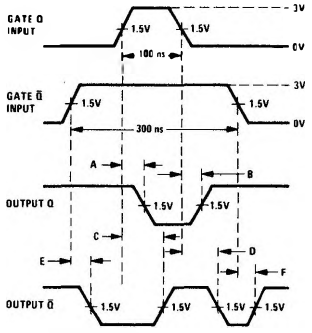


1. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ± 5 ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "1" output Q
   B = Differential input to logical "0" output Q
   C = Differential input to logical "0" output Q̄
   D = Differential input to logical "1" output Q̄
   E = Strobe input to logical "1" output Q
   F = Strobe input to logical "0" output Q
   G = Strobe input to logical "0" output Q̄
   H = Strobe input to logical "1" output Q

AC test circuit (2)



voltage waveforms (2)



1. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ± 5 ns, PRR = 1 MHz
2. Propagation delays:
   A = Gate Q input to logical "0" output Q
   B = Gate Q input to logical "1" output Q
   C = Gate Q input to logical "1" output Q̄
   D = Gate Q input to logical "0" output Q̄
   E = Gate Q̄ input to logical "0" output Q̄
   F = Gate Q̄ input to logical "1" output Q̄